

Thermal Challenges in Enabling Validation & Test of 3D Package on Package

**Ying-feng Pang, Arunima Panigrahy, Jack Mumbo,
Michael Apodaca, Victor Polyanko**

Intel Corporation



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Contents

- Trend of 3D Packaging
- Thermal Challenges in Validation and Test
- Proposed Solution
- Case Study
- Summary



Thermal Challenges in Enabling Validation & Test of 3D Package on Package

2

2020

Trend of 3D Packaging

- Benefits
 - Demand for higher performance
 - Small form factor (small footprint)
 - Improved interconnect performance (shorter length)
- Challenges
 - Thermal issues
 - Reliability issues

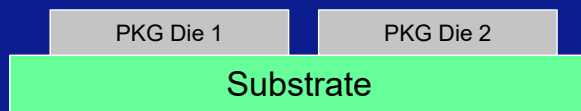


Thermal Challenges in Enabling Validation & Test of 3D Package on Package

3

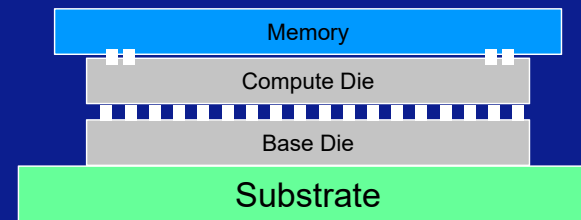
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2D vs 3D Packaging



2D Multi-chip Package

- Multiple dies on a substrate
- No stacking of dies on dies



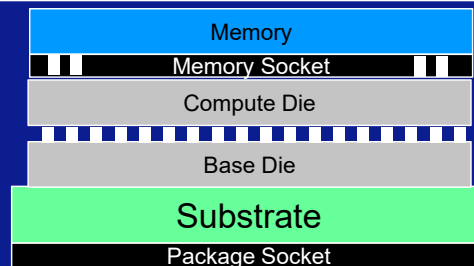
3D High Density Package

- Lateral die to die interconnect (RDL, EMIB, silicon interposer, etc.)
- Through Silicon Via (TSV) between the top package and bottom package
- Good electrical performance due to short interconnects
- Smaller form factor

RDL – redistribution layer
EMIB – embedded multi-die interconnect bridge

3D Package – Thermal Challenges in Test & Validation

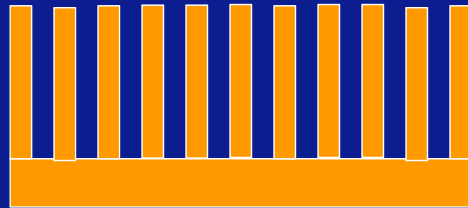
Thermal Solution



Socketed package required
in test & validation

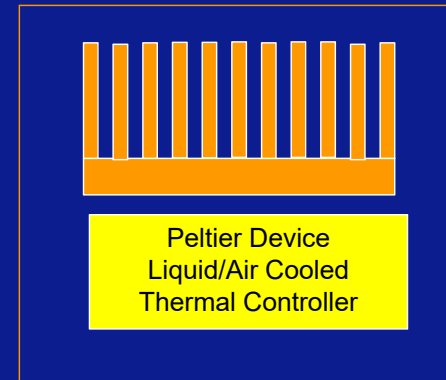
- Large thermal resistance through package stack-up
- Thermal conductive of the sockets
 - soldered-down package has better thermal conduction path
- Operating temperature of the sockets
- Limited memory operating temperature range: -25°C to 85°C
- Wide temperature margining range required for test and validation: -25°C to 125°C
- Limited space for thermal solution

Cooling Solution vs. Temperature Margining Solution



Typical Cooling Solution

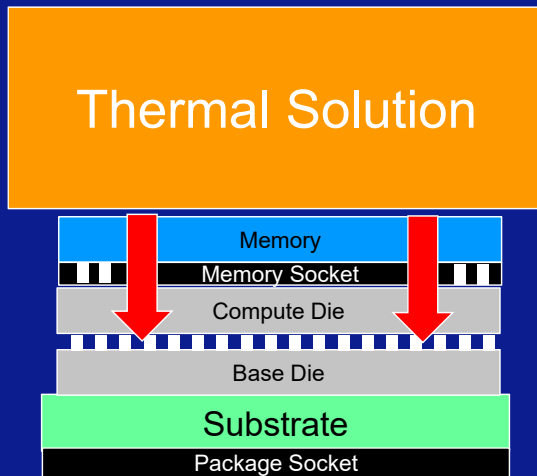
- Prevent package overheating
- Can be air-cooled or liquid-cooled



Temperature Margining Solution

- Has temperature control capability
- Able to provide desired set temperature to the package

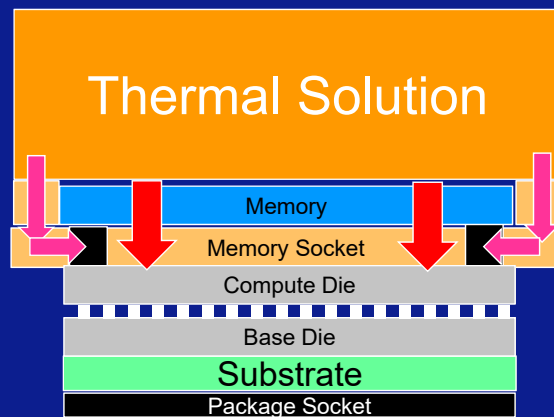
Thermal Conduction Path



- Thermal solution is typically designed to make contact on the top of the package
- Memory package limits the effectiveness of thermal conductive path through the 3D package
- Large temperature gradient from thermal solution to the compute/base die

Not an effective way of enabling temperature control to the package through the package stack

New Concept: Split Conductive Memory Socket

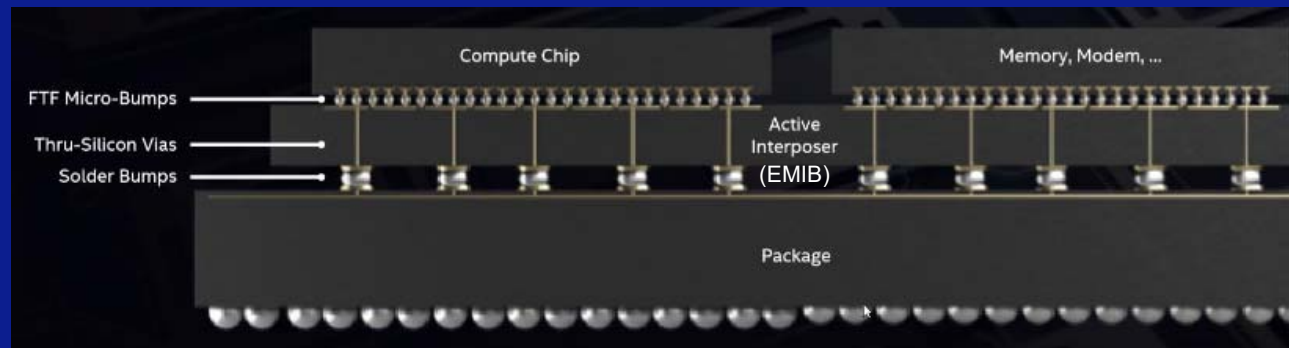


- Enhanced thermal conductivity of the memory socket
- By-passes the memory and provides a conductive path directly to the Compute Die
- Avoids reaching memory package temperature limitation

→ Conduction through memory socket wing

→ Conduction through package top

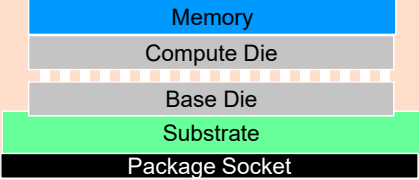
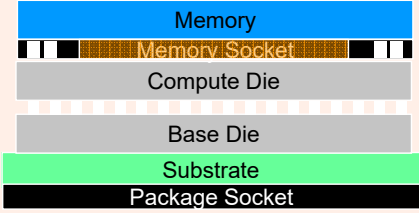
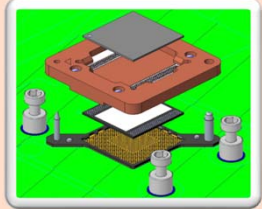
Case Study: 12x12mm 3D Co-PoP



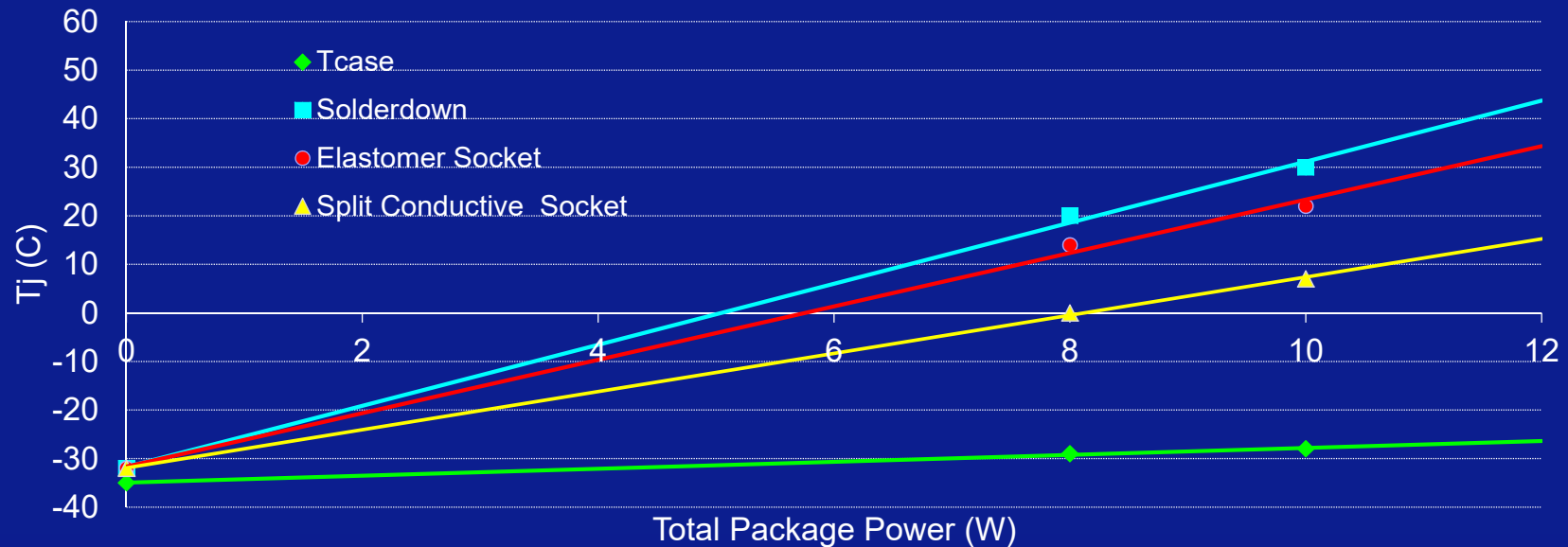
Source: <https://arstechnica.com/gadgets/2018/12/intel-introduces-foveros-3d-die-stacking-for-more-than-just-memory/>

- 12mmx12mm 3D package on package
- Total package power distribution
 - DRAM: 0.05X TDP
 - Compute die: 0.92X TDP
 - Base die: 0.03X TDP
- Test & validation temperature margining requirements:
 - DRAM: T_j -25°C to 85°C
 - SoC: T_j -25°C to 95°C

Case Study: Socket Configurations

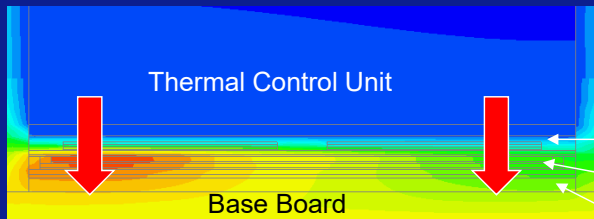
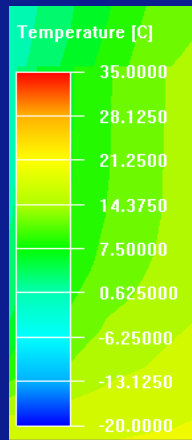
Study	Description	
Solder-down memory	<ul style="list-style-type: none"> No memory socket Epoxy between memory and bottom package 	
Elastomer memory socket	<ul style="list-style-type: none"> With metal insert between memory and bottom package 	
Split conductive memory socket	<ul style="list-style-type: none"> Extended wing around memory package and between memory and bottom package 	

Thermal Simulation Studies

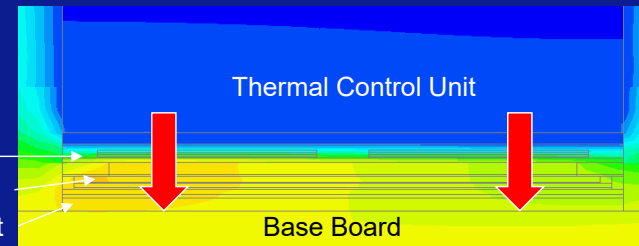


- Elastomer socket with metal insert at the center of the socket provides better thermal conduction path than solder-down memory
- Split conductive socket provides better thermal conduction path among the cases studied

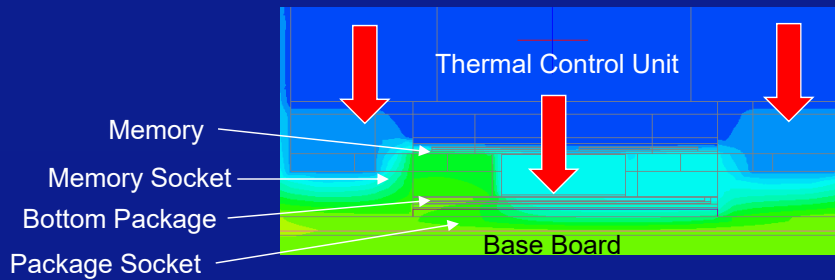
Temperature Distribution



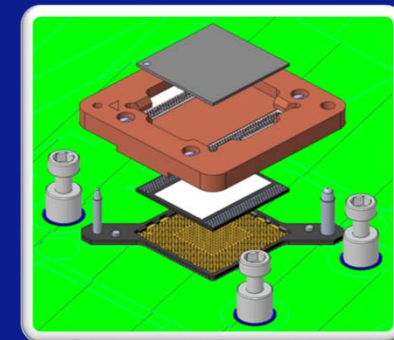
Solder-down Memory



Elastomer Memory Socket with Metal Insert

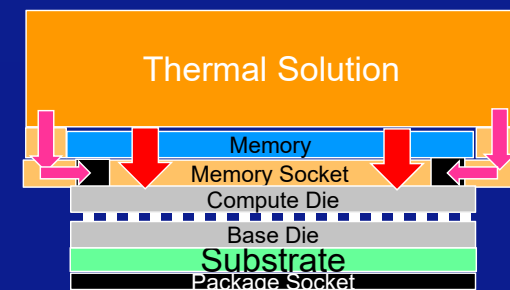


Split Conductive Memory Socket



Summary

- A new socket concept was introduced for improving the thermal conduction path of a 3D package
- With the use of split pogo pin conductive memory socket, the thermal resistance was significantly reduced
- This new concept enables the wide temperature range needed for test & validation even for a large package thermal resistance of a 3D package-on-package



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