

99% Validation Efficiency through Cloud Power Sequencing

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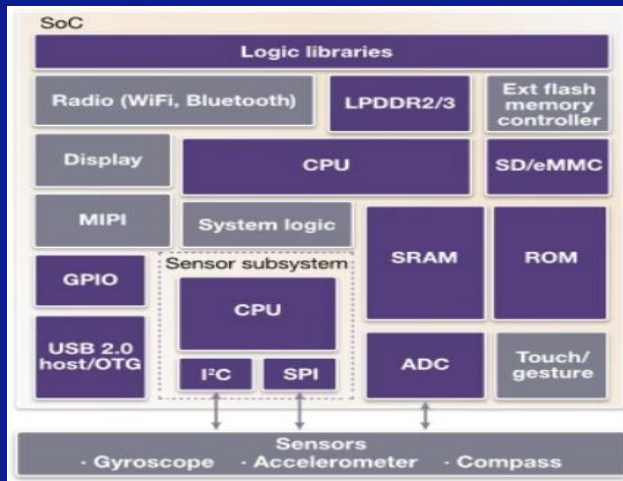
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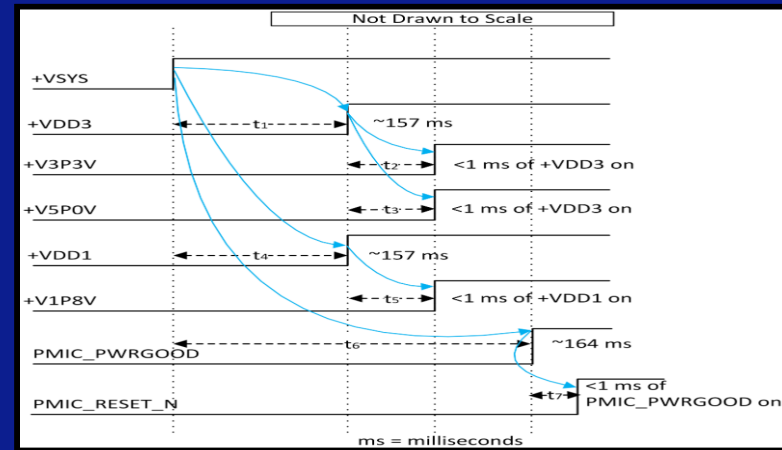
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What is Power Sequencing?



Example of SoC Block Diagram



Power On Timing Sequences

- Measure Power On and Power Down timings and Voltages
- Critical to ensure products functionality

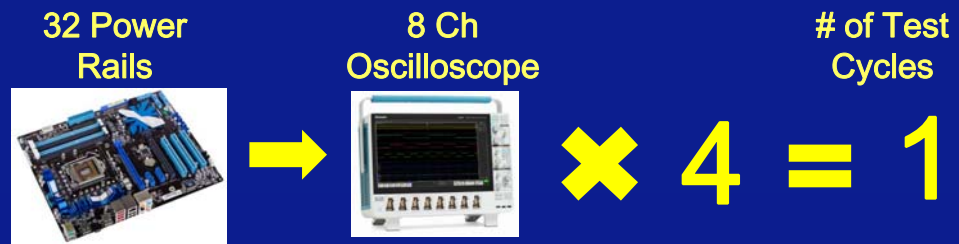
Problem Statement

- Cost to perform power sequencing test

- 4 x Tektronix MSO58 scope = \$140,000
- Power sequencing test time = 5 hours/test
- Engineer/technician involved = 2 heads
- Characterization method = manual
- Result accuracy = vary by person/skills

- Disadvantages:

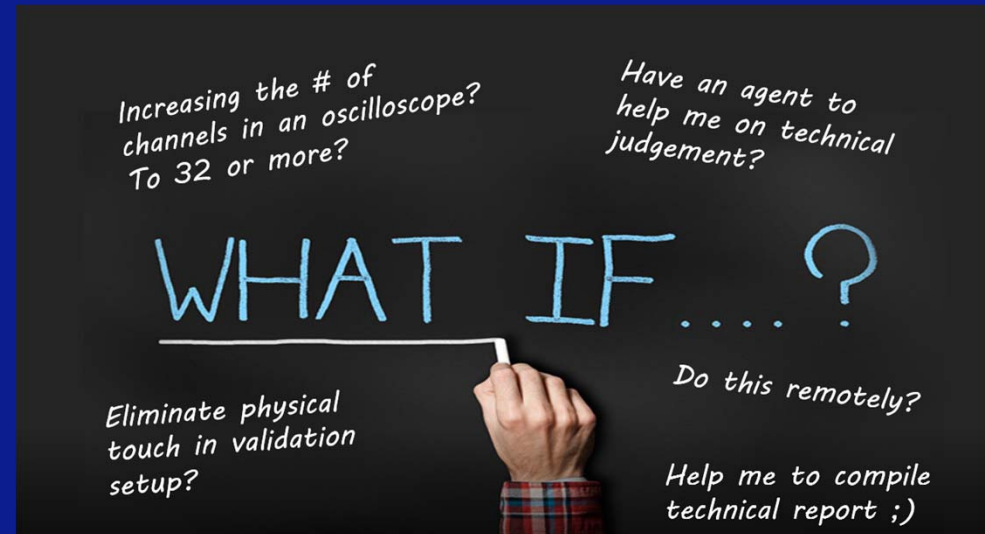
- Slow
- High cost
- Inaccurate
- In-depth technical skills required
- Physical touch required



Estimation of Performing Power Sequencing Test

Objectives

- Expands users' access to customers' reference boards through CLOUD to
 - Eliminated human dependencies and enabled measurement remotely
 - Highly accurate test results
 - Concurrently for multiple channels of measurements

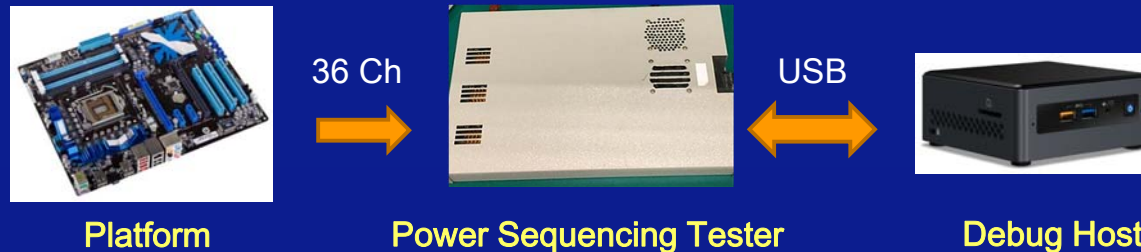


Frequent Asks from users

Solution Overview

Power Sequencing Tester serve as a multi-channel oscilloscope that

- Software : Applying FPGA (Field Programmable Gate Array) & Verilog scripting for the automation.
- Hardware Design : 36 probers & 4 GNDs are connected to platform to measure voltage and timing requirements.
- Dashboard : Graphical User Interface (GUI) is developed to allow easy entry of power rules, voltage specification. The graphs are plotted after post processing.
- Test Report : test results can be retrieved from debug host and report out as pass/fail in html/Pdf format.



Example of Power Sequencing Test
High performance, high capacity

Architecture Overview

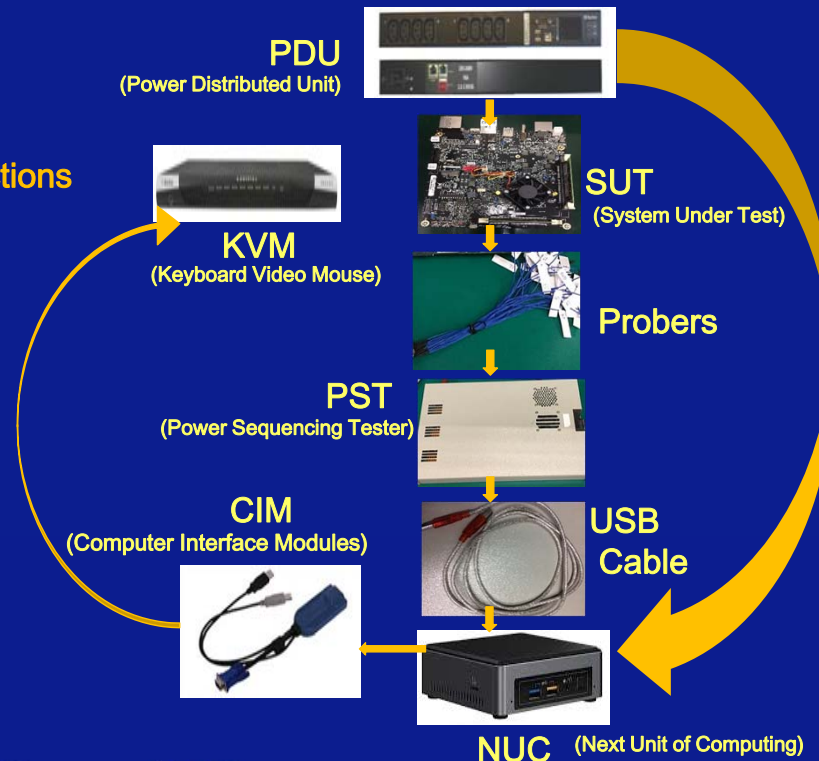
- KVM & PDU is to enable remote access and power cycling.
- NUC is connected to KVM via CIM cable.
- NUC can be configured as Virtual Machine.

PST Solution Specifications:

- 36 simultaneous measurement channels
- 8-bit resolution/channel
- Sampling rate at 1M/second/channel
- Input impedance @ 1M Ω
- 3 voltage range (0-5V, 0-20V, +/-10V)
- Stored up to 1min of measurement data
- Single channel edge triggering (rising/falling), with adjustable threshold and selectable channel

Architecture Overview

Hardware Connections



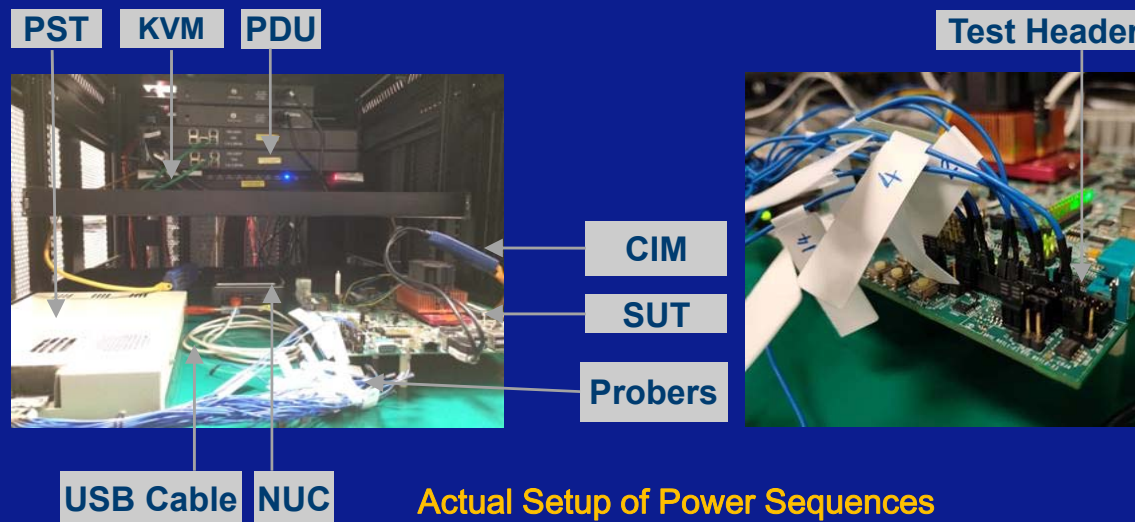
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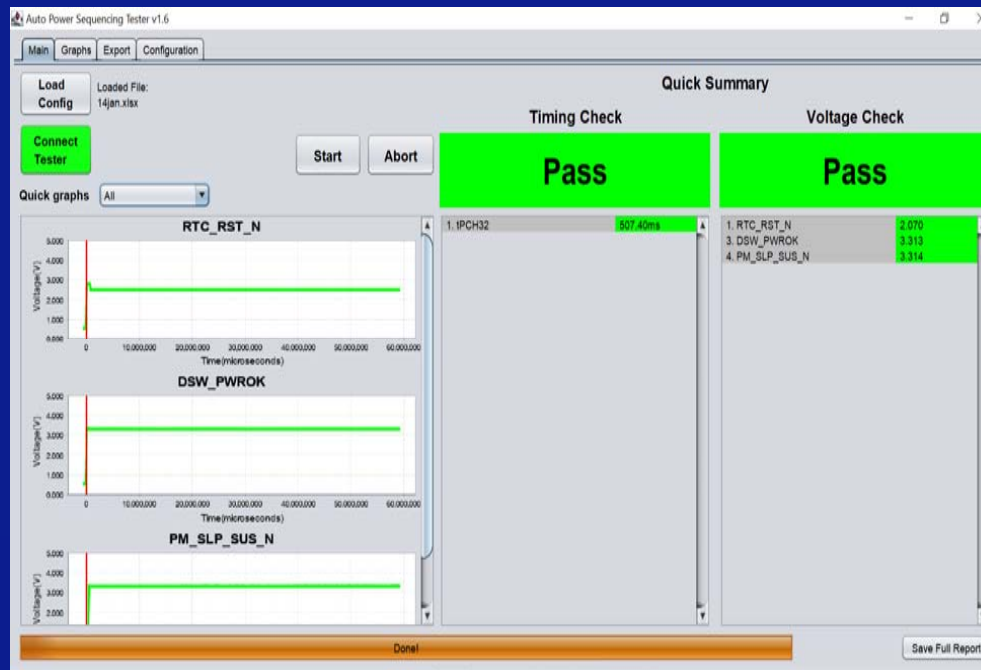
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Architecture Overview

- NUC can be configured as Virtual Machine (VM).
- VM is connecting to Cloud Environment to enable maximum efficiency.



Dashboard Overview



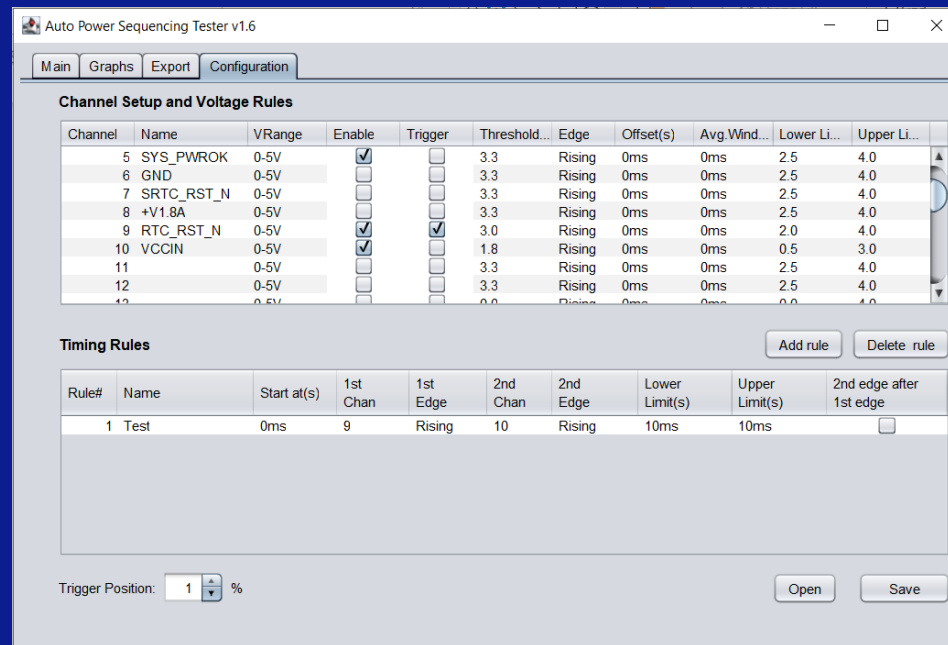
Screenshots of actual Power Sequencing Tests “ Main Tab



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Dashboard Overview



Screenshots of actual Power Sequencing Tests " Configuration" Tab



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Dashboard Overview



Screenshots of actual Power Sequencing Tests "Graph" Tab

Sample Report Overview

Power Sequencing Tester Report

Software Version: 1.6
 Creation Date: 2020-01-14T14:22:46.7301587+08:00[Asia/Singapore]
 Config file: C:\Users\WorkStation 1\Desktop\PST\PST_v1p4\14jan.xlsx
 Overall result: Pass
 Voltage check result: Pass
 Timing check result: Pass

Voltage checking rules and results

Showing only enabled channels

Chan #	Name	Meas. Voltage Range	Channel Enable	Trigger	Threshold	Trigger Edge	Meas. offset time	Avg. window time	Lower Limit	Upper Limit	Measured value	Result	Fail reason
1	RTC_RST_N	0-5V	True	False	1.5V	Rising	10.0000ms	10.0000ms	2.0V	3.0V	2.097V	PASS	
3	DSW_PWROK	0-5V	True	True	1.5V	Rising	10.0000ms	10.0000ms	2.5V	4.0V	3.314V	PASS	
4	PM_SLP_SUS_N	0-5V	True	False	1.5V	Rising	10.0000ms	10.0000ms	2.5V	4.0V	3.307V	PASS	

Timing checking rules and results

Rule #	Name	Start checking from	From Channel	From Channel Edge	To Channel	To Channel Edge	Lower Limit	Upper Limit	2nd edge only after 1st edge	Measured value	Result	Fail reason	Chart
1	pPCH32	1.0000ms	3	Rising	4	Rising	95.0000ms	5.0000s	true	1.0212s	PASS		Go

Example of Report for RTC, power OK signals measurements



Impact of Cloud Based Remote Debug

Components	Before	After	Improvements
Hardware Cost	\$140,000	\$30,000	78.57%
Test Time	5 hours/test	2 minutes	99.33%
Headcount	2 heads	0 heads	100.00%
Characterization Method	Manual	Systematic	100.00%
Result Accuracy	Vary by person/skills	Systematic	100.00%

- Better customer engagement & collaboration: Solution will be offered to Intel's customers as part of features in Cloud Based Remote Debug infrastructure
- Competitive advantage through IP: All SoC (System On Chip) designers performed power sequencing test

Summary

2 MIN **EFFICIENCY** Improved power sequencing test time by **99.33%**

COSTS **COST** Reduced **78.57%** of oscilloscope purchase in Intel

QUALITY **100%** accuracy in test results with details report

REMOTE Eliminate physical touch & automate validation process

The graphic features several icons: a blue arc with '2 MIN', a yellow tag with 'COSTS' and scissors, a red target with 'Quality', and a blue cloud with a lock icon. The background is a network of nodes and lines.

- In a nutshell, this Power Sequencing Tester is able to scale to support both internal validation teams as well as external customers for the critical issue debugging on power rail voltage and timings.

Acknowledgements

- Eric Chan - VP in Intel IoTG (Internet of Thing Group)
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- Goh, Kean Hean – Engineering Lab Manager
- Ooi, Seong Guan – Post-Silicon Technologist & Product Owner



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