New Tester Qualification using Parallel Test & Correlation for Soft Error Rate Measurements

KRISHNA MOHAN CHAVALI, JOSHUA DRAGULA
GLOBALFOUNDRIES

Virtual Event • May 11-13, 2020

Contents

- Abstract
- Soft Errors - Introduction
- Qual Requirements & Standards
- Methodology & Flow
- Parallel Testing & Data Collection
- Test Results & Correlation
- Costs & Cycle Time Savings
- Conclusion

Acronyms

- SER – Soft Error Rate
- SEU – Single Event Upset
- SET – Single Event Transient
- ASER – Alpha Soft Error Rate
- TNSER – Thermal Neutron SER
- HEN – High Energy Neutron
- pSER – Proton SER
- FF – Flip Flop
- MFF – Million FF's.
- FITs – Failures in Time
- STS_A: Chip with Standard FF's
- STS_B: Chip with Enhanced FF's
- MIL-STD – Military Standard
- JESD89 – JEDEC SER Standard

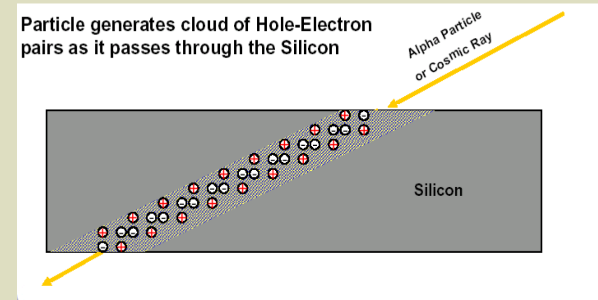
Abstract

- Off-shelf testers will not survive the accelerated harsh radiation environment.
- Custom designed new tester need to go through proper qualification procedure to ensure before releasing for regular SER testing.
- How a new package level tester was qualified with high energy proton beam SER stress testing, to qualify and to release.
- Proper correlation of new tester in beam test environment is planned.
- An existing old qualified tester was used as reference standard to compare.
- Both went through the proton high energy beam testing and data collection.
- Logic test chips from FinFETs bulk process were used by both testers.
- Testers run in parallel, through the beam environment, for data collection along with the correlation data results, presented.

Soft Errors - Introduction

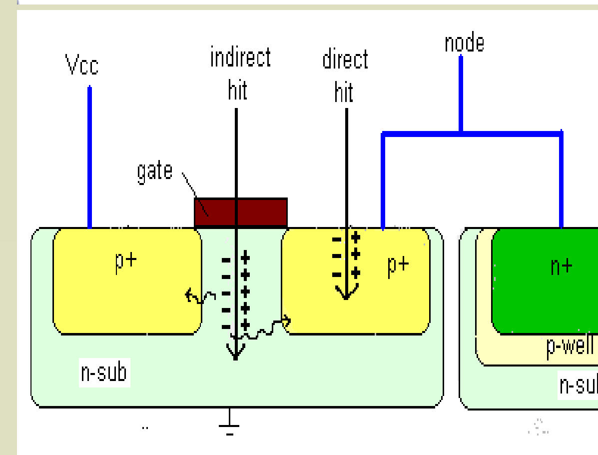
When alpha particles/cosmic rays fall on diffusion areas (of IC), the resulting electron funneling will cause the logic state to flip.

This phenomenon is called “Soft Error” or “Single Event Upset” (SEU’s).



- Radiation showers from environment cause electron-hole pairs’ generation.
- When these additional charges gets collected by diffusion areas, can flip node’s logic state causing “Soft Error” or SEU’s.
- Sort Error: Flipping of Node’s Logic State

  $1 \Rightarrow 0$ or $0 \Rightarrow 1$
- Biased nodes & diffusion areas are susceptible.



Factors that Impact SER

Process:	**Bumping/Assembly/Material:**

➢ Bulk or SOI.
➢ Doping concentration & profile
  ➢ in substrate and wells.
➢ Junction: Voltage & capacitance.
➢ Materials & Passivation:
  ➢ BPSG, SiN or Polyimide
	➢ Wafer Bumping:
	  ➢ SnAg or Copper Pillar
	➢ Assembly material & coating
	  ➢ Lead frame & Die attach
	➢ Molding Compounds:
	  ➢ Synthetic, plastic, ceramic

Design & Device:	**Application:**
➢ Bit Cell Size ➢ Redundancy ➢ Error Correction Code (ECC) ➢ Refresh Rate.	➢ Radiation Level ➢ Altitude & Latitude ➢ Consumer, Industrial ➢ Avionics, Space (Mission Critical)

Alpha Particles & Sources

Alpha particles are: Randomly generated, Charged, Energetic, Nuclear particles from several sources.

- Alpha particles are: Helium Nuclei,
- Composed of 2 protons & 2 neutrons and
- Have a charge state of plus two.

Sources: Well known sources of Alpha Particles:

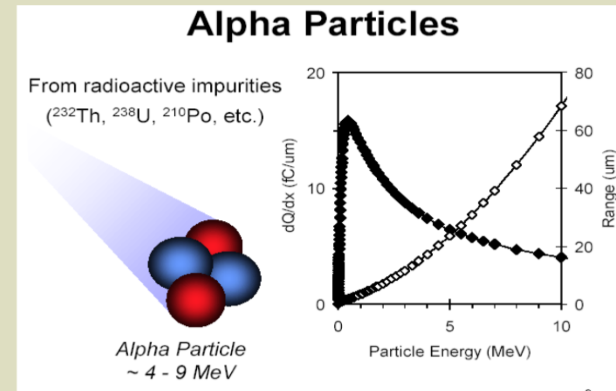
a) Cosmic rays: extraterrestrial rays from outer space.

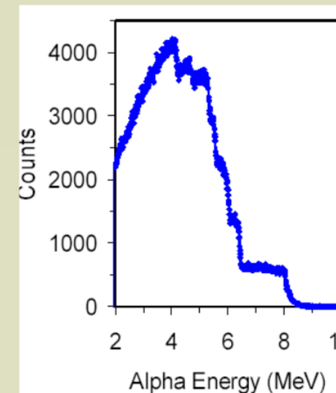
b) Decay of radioisotopes: Radon, Thorium, Uranium.

c) Lead based products: Solder, paint, etc.

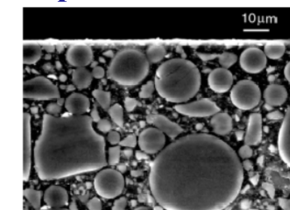
d) Concrete buildings, Ceramics and

e) Some plastics.





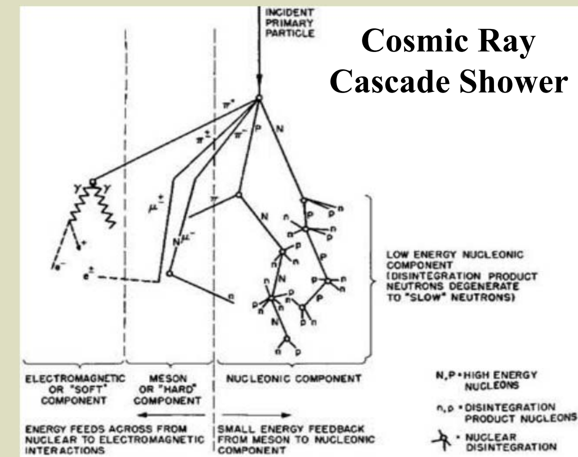
Alpha Emission Rates



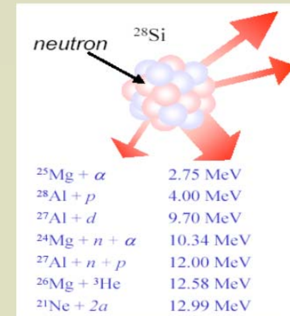
Processed Wafers	0.0005 α/cm²-hr
Cu Metal (thick)	0.0019
Al Metal (thick)	0.0014
Mold Comp.	0.024 - < 0.002
Underfill	0.002 - 0.001
Pb-solders	7.200 - < 0.002

Cosmic Rays & Spallation

- Cosmic Rays **originate in galaxy** / solar system.
- In Atmosphere, degenerate into Neutrons & Mesons.
- These neutrons and protons, undergo “strong nuclear interaction” with other matter.
- Protons can be shielded but Neutrons pass through matter until strike other nuclei & cause “**Spallation**”.
- Spallation generates large number of other high energy particles.
- They can even knock silicon atoms out of the lattice.
- The energy generates large numbers of electron-hole pairs along their path in silicon causing SER/SEU.



Spallation ➔



$^{25}Mg + \alpha$	2.75 MeV
$^{28}Al + p$	4.00 MeV
$^{27}Al + d$	9.70 MeV
$^{24}Mg + n + \alpha$	10.34 MeV
$^{27}Al + n + p$	12.00 MeV
$^{26}Mg + ^{3}He$	12.58 MeV
$^{21}Ne + 2\alpha$	12.99 MeV

SER Qual Requirements

- Soft Error Radiation (SER) tests are part of Tech. node Quals.
- SER Qualification and test methodology based on JESD-89.
- SER Qual is done using either SRAM or Logic test chips/vehicles.
- SER Qual Tests, generally, done in three radiation environments.
  - Alpha SER, Thermal Neutron SER and High Energy Neutron Beam SER.
  - **Alpha: @0-5MeV**; Thermal Neutron: @**5-50MeV**; HE Neutron:@**50-500MeV (1GeV)**.
- Commercial/off-shelf testers end up failing or give wrong results.
  - Due to the radiation interacting with test hardware, might produce wrong data.
- Custom designed testers to withstand harsh radiation environment.

SER – Test Standard

This test measures the failure rates: FITs/hr/MFF or FITs/hr/Mb

Under different accelerated radiation environments: Alpha, Thermal Neutron & High Energy Neutron etc.,

- JEDEC Standard No : JESD-89
- Military Standard No : MIL-STD-883E, Method 1032.1
- Radiation Source : Alpha, T. Neutron, HE Neutron
- Voltages Used : Vnom-10%, Vnom, Vnom+10%
- Stress Modes : Static and Dynamic
- Test Patterns : INV/CHBD, S0, S1, S0-1, S1-0.

TestConX™ New Tester Qualification using Parallel Test & Correlation for Soft Error Rate Measurements 10 2020

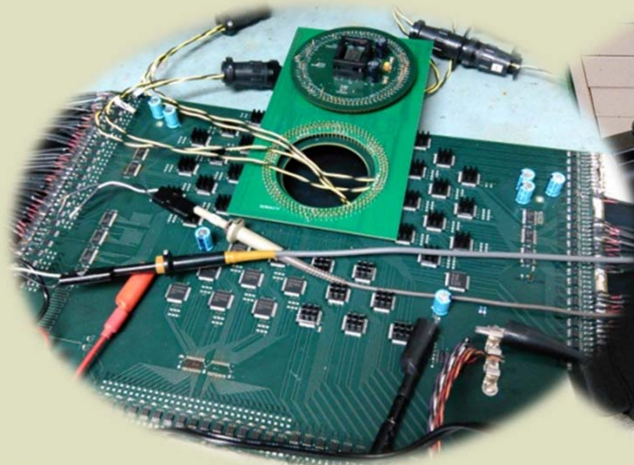
Need for 2nd Tester Qual

- Existing tester was 20years old, though working – need backup
  - If it fails – need 1year to redesign – Tech. node quals impact.
- Beam time is costly: @1000~1200 USD/hr, @30K for beam/qual alone.
  - By having 2 testers and parallel testing 2xDUTs can be tested.
- New tester completed assembly, integration & prelim tests – after 3years.
- Planned to use next Qual beam testing to use both testers in parallel.
- Existing tester was used as standard for reference data to compare.
- Data from both testers, running simultaneously can be correlated using:
  - Running both testers in parallel for each run, same duration, swapping DUTs etc.,
  - Distance & position of DUT from beam were **off-set by the Geometry Factor.**

New Tester: Serenity

- Capable of detecting Multiple Event Upsets
- 32 addresses (4096Mb) x 36 data bits = 144Gb
- Maximum speed 50MHz

Test-head

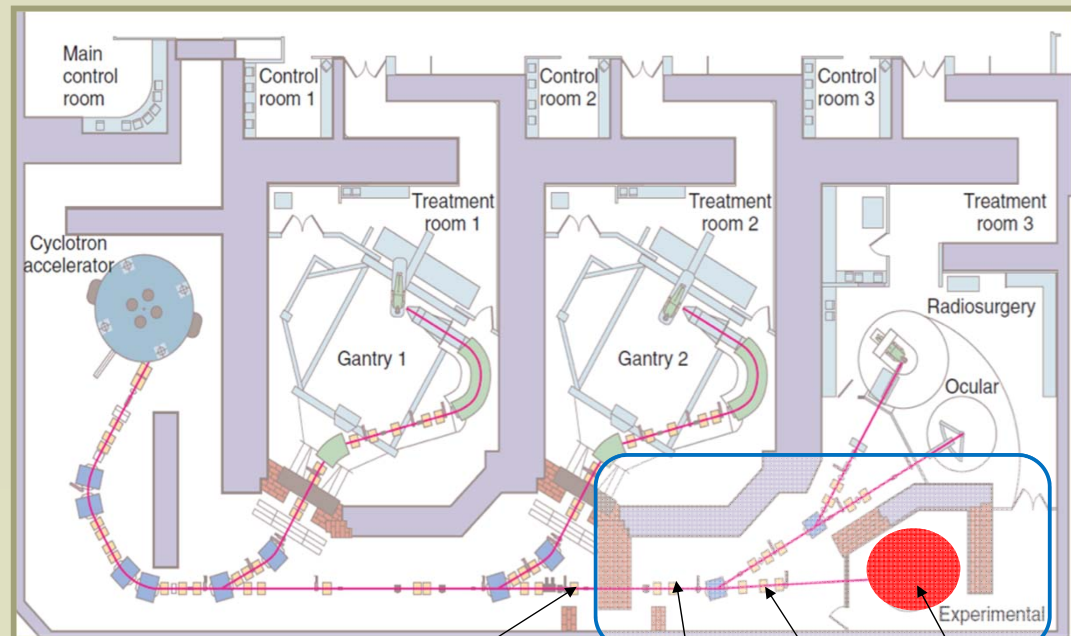


Tester

TestConX™ New Tester Qualification using Parallel Test & Correlation for Soft Error Rate Measurements 12 2020

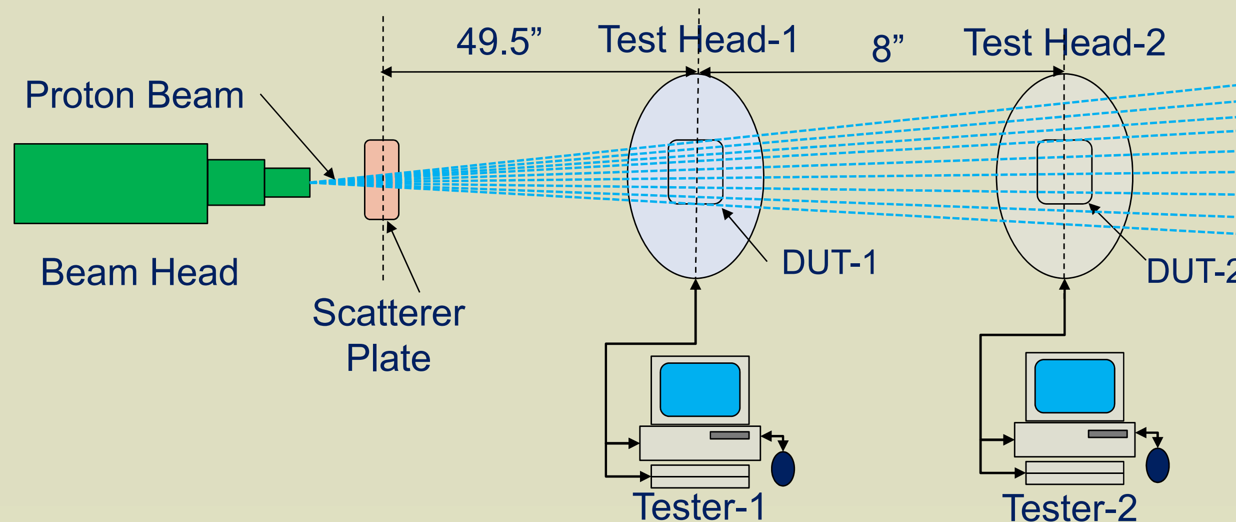
Soft Error Rate Testing Room

- The Test heads (1 &2), containing the DUT sockets, were placed directly in the proton beam path.
- The Testers 1 & 2 were placed on the side.
- Testing was performed in the Experiment room.



Test Board’s & Testers Arrangement

(For Parallel Testing)



- Measured Distance from scatter plate to the first test board = 49.5“
- 2nd test board was positioned 8" away behind the 1st test board as shown.
- So, for 2nd test board, the ratio of Fluence/Monitoring Units = 49.5^2/(49.5+8)^2 = 0.74

➔ Error Rate at 2nd test board should be @74% of error rate at 1st Test Board.

New Tester Qual Plan for SER

- Logic Proton beam tests are planned on packaged DUTs at MGH*.
  - MGH - Massachusetts General Hospital is the proton beam facility used.
- DUTs from 3 lots' from different zones are selected – shown below
- Two testers used: old & new with separate HW to expedite more data.
- More than 72 test runs on 36 DUTs with two testers collected.

Type	Lot ID	Assem ID	DUT IDs	DUT ID's by Wafer Zones			
				Center	Mid Zone	Edge	Extreme Edge
STS-A	8XYN23111	RFB5001	A41-A50	A48, A49	A45,A44	A42, A47	A41, A43, A46, A50
STS-B			B41-B50	B48, B49	B45,B43	B42, B47	B41, B44, B46, B50
STS-A	8XYN23110	RFB5000	A21-A30	A28, A29	A25,A23	A22, A27	A21, A24, A26, A30
STS-B			B21-B30	B28, B29	B25,B23	B22, B27	B21, B24, B26, B30
STS-A	8XYN22070	RFB4999	A01-A10	A08, A09	A05,A03	A02, A07	A01, A04, A06, A10
STS-B			B01-B10	B08, B09	B05,B03	B02, B07	B01, B04, B06, B10

Correlation Checks Planed

The below checks are implemented to correlate data between two testers (1 & 2):

- ✓ Equal number of DUTs tested on both testers – from all zones and lots.
- ✓ Testers were run in parallel for each test run – two DUT cards used.
- ✓ 2Pcs of DUT boards were ordered – same design & supplier.
- ✓ Test duration for each test run (beam exposure) is same for both testers.
- ✓ DUTs from one DUT card and tester were swapped to collect data.
  - ✓ Run-1: Terster-1, DUT-1 and Tester-2, DUT-2 ➔ Run-2: Tester-1, DUT-2 and Tester-2, DUT-1
  - ✓ Both Run-1 and Run-2 are run with same beam fluence*, voltage, patterns and type.
- ✓ Data on two test chips collected with both testers: Standard & Enhanced FF's.
- ✓ Data on two types of Logic fails collected: SEU's and SET's.

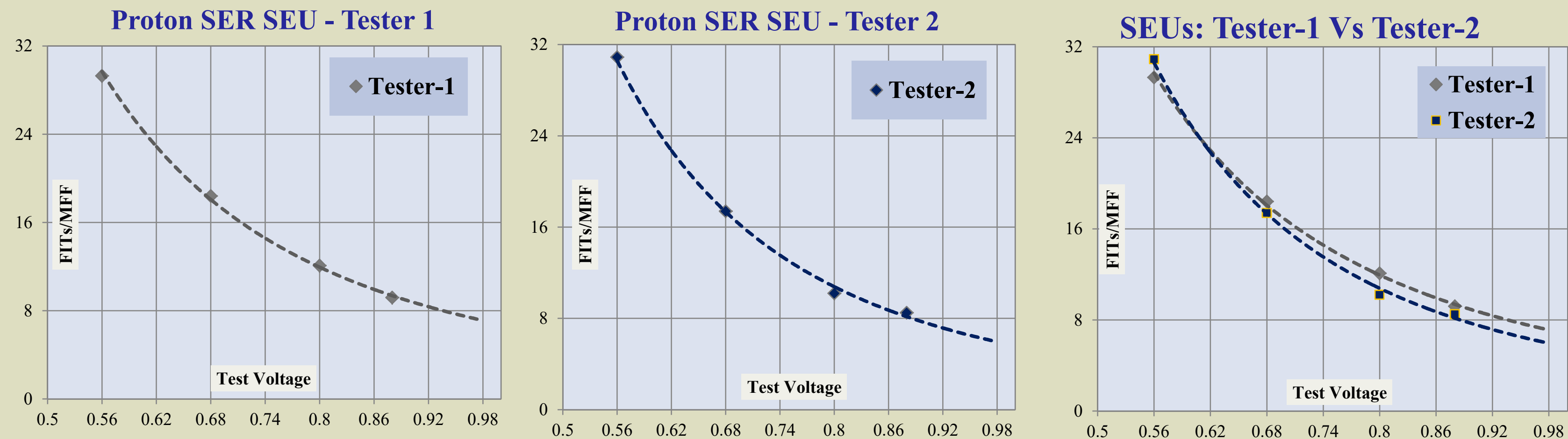
*__Fluence__ is radiation flux integrated over duration of exposure.

Correlation by DUT's Swap Data

- ✓DUTs from one DUT card and tester were swapped to collect data.
- ✓The fail rate and FITs data collected by swapping found to be @13%
  - ✓For SER tests, given the variations, <20% delta is within limits.

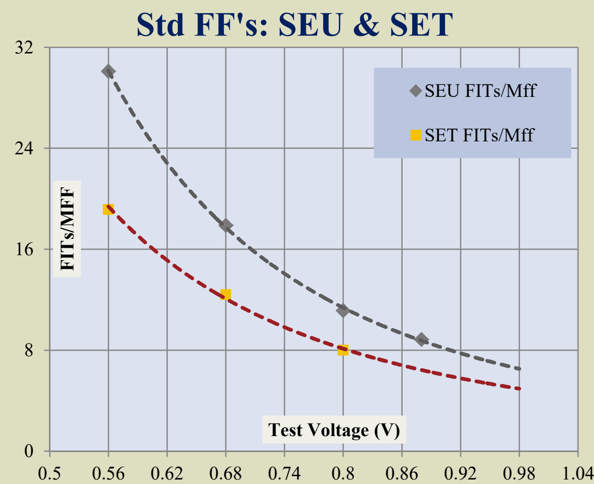
Swap	MeV	Type	Pattern	Voltage	T1-FITs	T2-FITs	Delta %
A28 on T1 A29 on T2 Test Data	150	SEU	S1	0.72	11.67	14.11	17
				0.80	8.48	9.40	10
				0.88	6.88	7.53	9
A29 on T1 A28 on T2 now swap on Testers	150	SEU	S1	0.72	9.87	11.44	14
				0.80	8.22	8.84	7
				0.88	7.12	7.59	6
	150	SET	S1	0.72	6.62	7.75	15
				0.80	4.48	5.38	17
				0.88	3.44	4.17	17
						Avg. Delta	**@13 %**

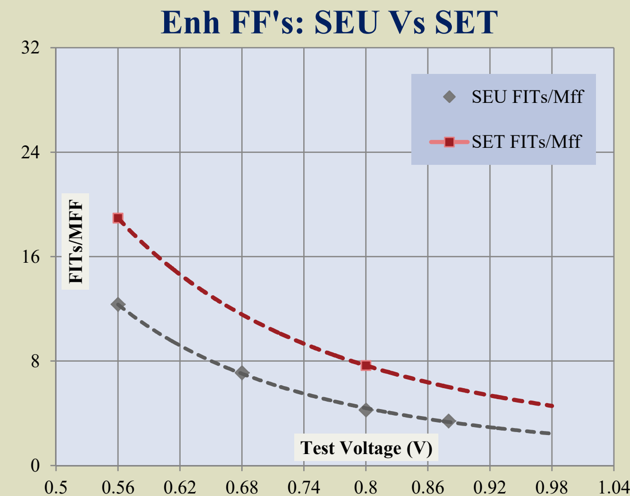
Logic pSER SEU data: Tester-1 Vs Tester-2



- SEU data on Standard FF's collected on both testers shows good voltage scaling.
- Data plotted separately & combined to compare for correlation – Chart-3 above.
- Data collected from both testers is well correlated on measured SEU data.
- Data from total 72 test runs (36 DUTs on each tester) was collected and compared.
- Test & stress data correlates well with old tester, the new tester is considered as Buy-off.

SEU's & SET's: Standard Vs Enhanced FF's





- Data from both testers for each run was checked to be same (within +/-20%).
- Enhanced FF's data show @ 3X improvement on SEU's – as expected.
- SETs fail data show same contribution on both Standard & Enhanced FFs.
- Logic SER data show comparable results with SRAM data collected before.

Cost & Cycle Time Savings

Some of the advantages of using 2 testers in parallel for SER:

- 2x DUTs can be tested for each run Vs using 1 tester.
- Need two DUT boards for parallel testing: 2K Vs 4K USD.
- Considering beam cost & cycle time savings ➔ justified.
- Beam time to book can be halved as 2x DUTs can be tested.
  ➔ 50% reduction in beam costs can be achieved.
  ➔ This will further reduce trip costs – hotel/stay costs by 50%.
- Project/trip Test time can also be reduced:
  - 3persons x 3days ➔ 2persons x 2days ➔ @40% reduction.
  - Saved time used for data checks & analysis – faster Qual.

Conclusion

- SEU & SET data on 2 test chips collected on both testers:
  - Good voltage scaling observed both old and new testers.
- Data from total 72 test runs (36 DUTs on each tester) compared.
- Both testers data for each run was checked to be same: < +/-20%.
- Enhanced FF's show @ 3X improvement on SEU's – expected.
- SETs FITs show same contribution on Standard & Enhanced FFs.
- Data plots from both testers on SEU & SET data – well correlated.
- Logic SER data show comparable results with SRAM data.
- New tester's test & stress data correlates well with old tester
  - The new tester is considered Qualified and released.

References

1) JESD89: Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices by JEDEC.

2) Alpha Particle induced Single-Event Error Rates and Scaling Trends in Commercial SRAM Cells by I. Chatterjee, B. L. Bhuva, S.J. Wen, R. Wong.

3) Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic Premkishore Shivakumar et. all, Proceedings of the 2002 International Conference on Dependable Systems and Networks.

4) SER Scaling and Trends in Planar Submicron Technology Nodes by Krishna Mohan Chavali, EDTM-2017, Tokyo, Japan.

5) Soft Error Rate from Planar to FinFETs and Bulk Vs SOI by Krishna Mohan Chavali, EDTM-2018, Tokyo, Japan.

6) Soft error rate scaling for emerging SOI technology options, by P. Oldiges et al., in Proc. 2002 Symposium VLSI Technology Dig. Tech. Papers, HI, June 11–13, 2002, Tech. Papers, pp. 46–47.

Acknowledgements

The author would like to Acknowledge and Thank GF's in-house Test, Bump/Assembly & REL ENG

- Teams at Malta, DRS & EFK Fab sites
- Collection of data on few test modes
- For support on external beam arrangements
- On time, efforts and resources.

Author also like to thank the reviewers for:

- Valuable suggestions & recommendations
- To improve the quality of the presentation.

COPYRIGHT NOTICE

The presentation(s)/poster(s) in this publication comprise the proceedings of the 2020 TestConX Virtual Event. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2020 TestConX Virtual Event. The inclusion of the presentations/posters in this publication does not constitute an endorsement by TestConX or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by TestConX. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

"TestConX" and the TestConX logo are trademarks of TestConX. All rights reserved.

www.testconx.org