Design of Modular Ultra-Low Voltage Power Delivery System for Sub-7nm SOC Validation

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Agenda

- 7nm SOC validation platform design challenges
- Modular platform architecture
- Power delivery network design strategies
- Validation and measurement
- Summary

7nm SOC Validation Platform Design Challenges

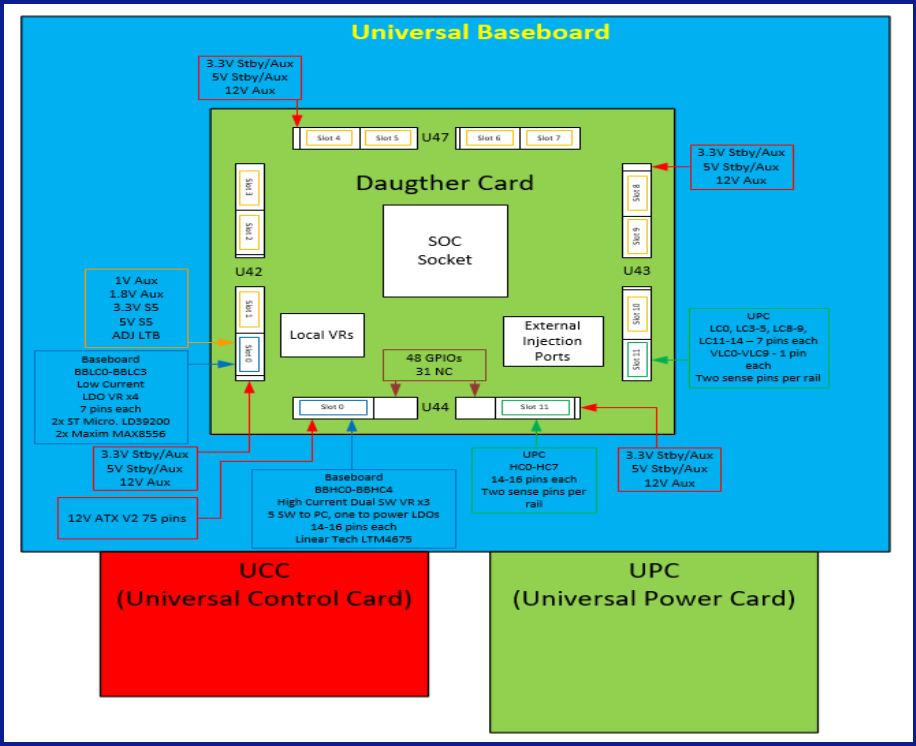
- Multiple voltage domains
- Ultra low voltages and high current
- Complex power up sequencing (over 40 rails)
- Low voltage AC/DC noise tolerance
- Tight transient response range

7nm SOC Validation Platform Design Challenges

Silicon Process Scaling

	7nm vs 10nm
Speed	Faster
Power	Less
Density	Higher
Core voltage	~0.6v (7nm), ~0.7v(10nm)

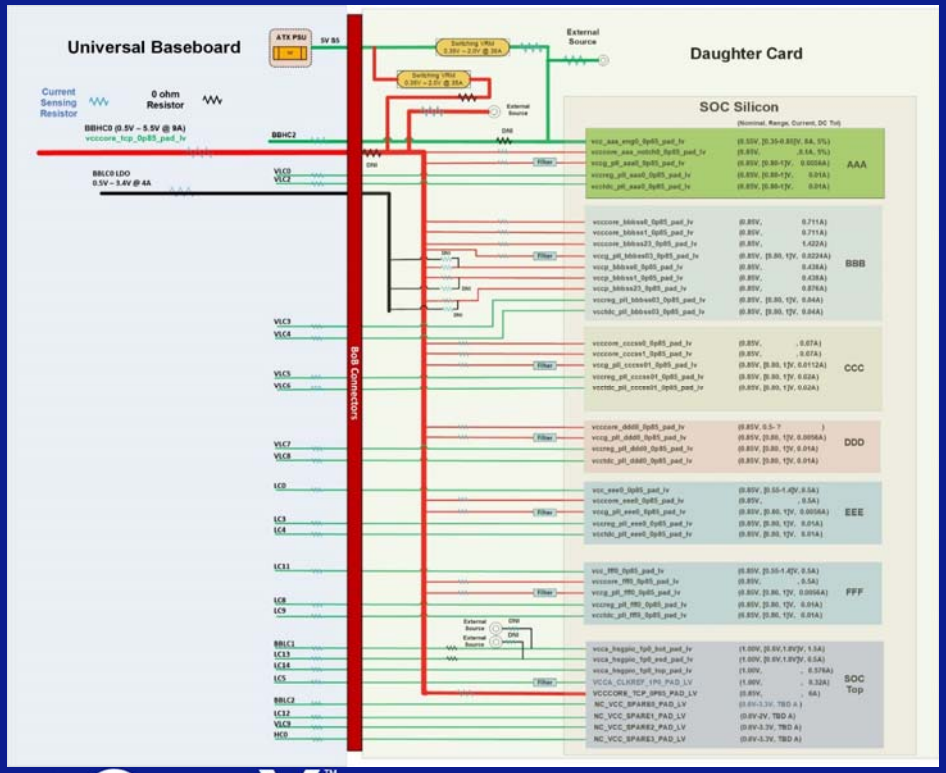
Modular Platform Architecture



Modules:

Universal Baseboard (UBB)
Daughter Card (DC)
Universal Control Card (UCC)
Universal Power Card (UPC)

Power Tree



Daughter card

Board to board connectors

Universal Baseboard (UBB)

Universal Base Board Stack up

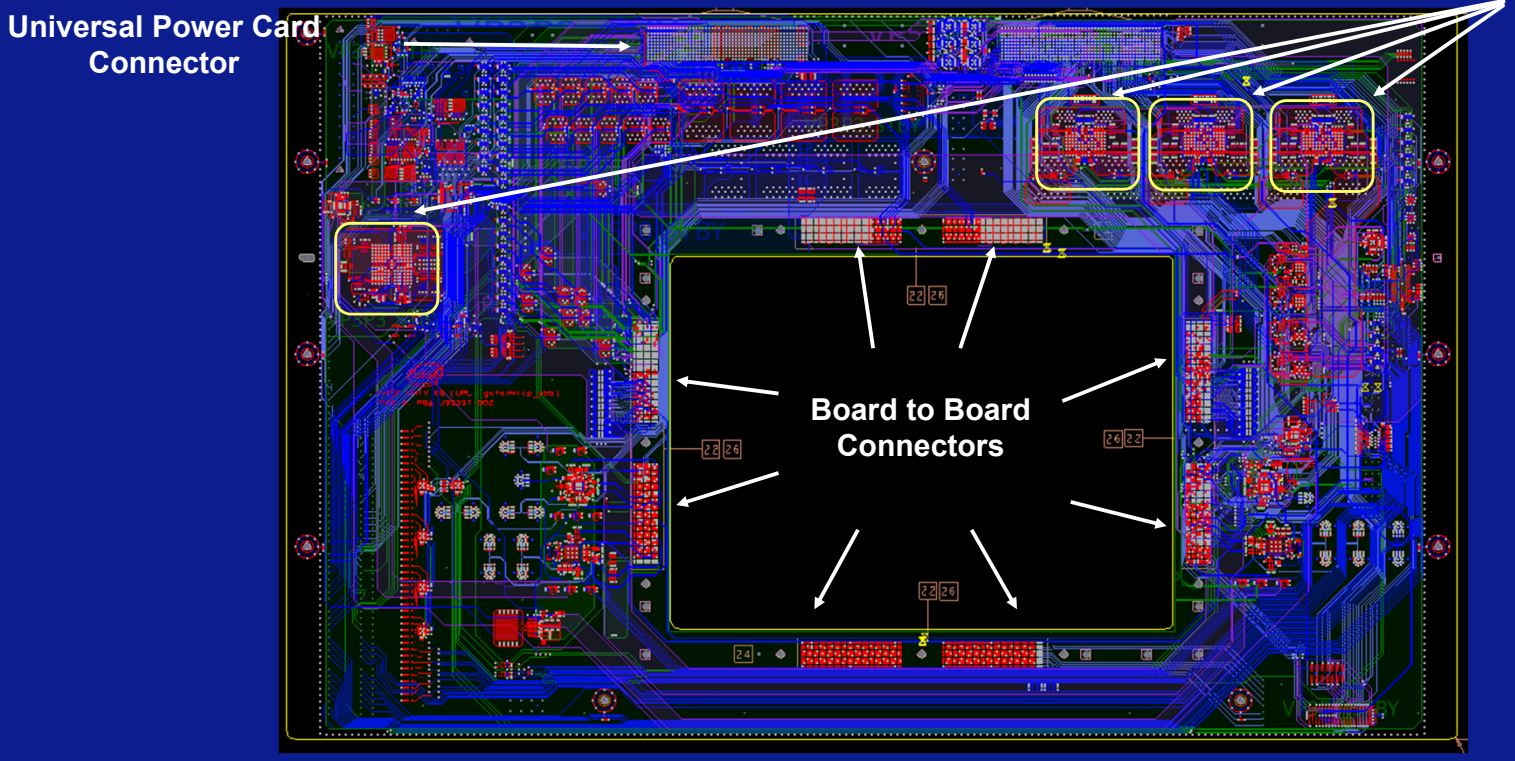
#	Name	Layer	Layer Function	Thickness Value mil
	SOLDERMASK_TOP	Mask	Solder Mask	0.5
1	TOP	Conductor	Conductor	1.4
		Dielectric	Dielectric	3.8
2	L02_GND	Plane	Plane	0.6
		Dielectric	Dielectric	4
3	L03_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4.1
4	L04_GND	Plane	Plane	0.6
		Dielectric	Dielectric	4
5	L05_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4.1
6	L06_GND	Plane	Plane	0.6
		Dielectric	Dielectric	4
7	L07_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4.1
8	L08_GND	Plane	Plane	1.2
		Dielectric	Dielectric	4
9	L09_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	4.1
10	L10_GND	Plane	Plane	1.2
		Dielectric	Dielectric	3
11	L11_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	3.3
12	L12_GND	Plane	Plane	1.2
		Dielectric	Dielectric	2.5
13	L13_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	3.3
14	L14_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	2.5
15	L15_GND	Plane	Plane	1.2
		Dielectric	Dielectric	3.3
16	L16_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	3
17	L17_GND	Plane	Plane	1.2
		Dielectric	Dielectric	4.1
18	L18_PWR	Plane	Plane	1.2
		Dielectric	Dielectric	4
19	L19_GND	Plane	Plane	1.2
		Dielectric	Dielectric	4.1
20	L20_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4
21	L21_GND	Plane	Plane	0.6
		Dielectric	Dielectric	4.1
22	L22_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4
23	L23_GND	Plane	Plane	0.6
		Dielectric	Dielectric	4.1
24	L24_SIG	Conductor	Conductor	0.6
		Dielectric	Dielectric	4
25	L25_GND	Plane	Plane	0.6
		Dielectric	Dielectric	3.8
26	BOTTOM	Conductor	Conductor	1.4
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.5
		Surface		

Power layers:
L9, L11, L13,
L14, L16, L18

Ground layers:
L2, L4, L6, L8, L10
L12, L15, L17,L19
L21,L23, L25

Signal layers:
L3, L5, L7, L20, L22,
L24

Universal Base Board Layout



Daughter Card Stack up

Objects		Types		Thickness
#	Name	Layer	Layer Function	Value mm
		Surface		
	SOLDERMASK_TOP	Mask	Solder Mask	0.0127
1	TOP	Conductor	Conductor	0.03556
		Dielectric	Dielectric	0.09652
2	L02_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.1016
3	L03_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.10414
4	L04_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.1016
5	L05_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.10414
6	L06_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.1016
7	L07_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.10414
8	L08_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.1016
9	L09_PWR	Plane	Plane	0.03048
		Dielectric	Dielectric	0.10414
10	L10_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.0762
11	L11_PWR	Plane	Plane	0.03048
		Dielectric	Dielectric	0.08382
12	L12_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.0635
13	L13_PWR	Plane	Plane	0.03048

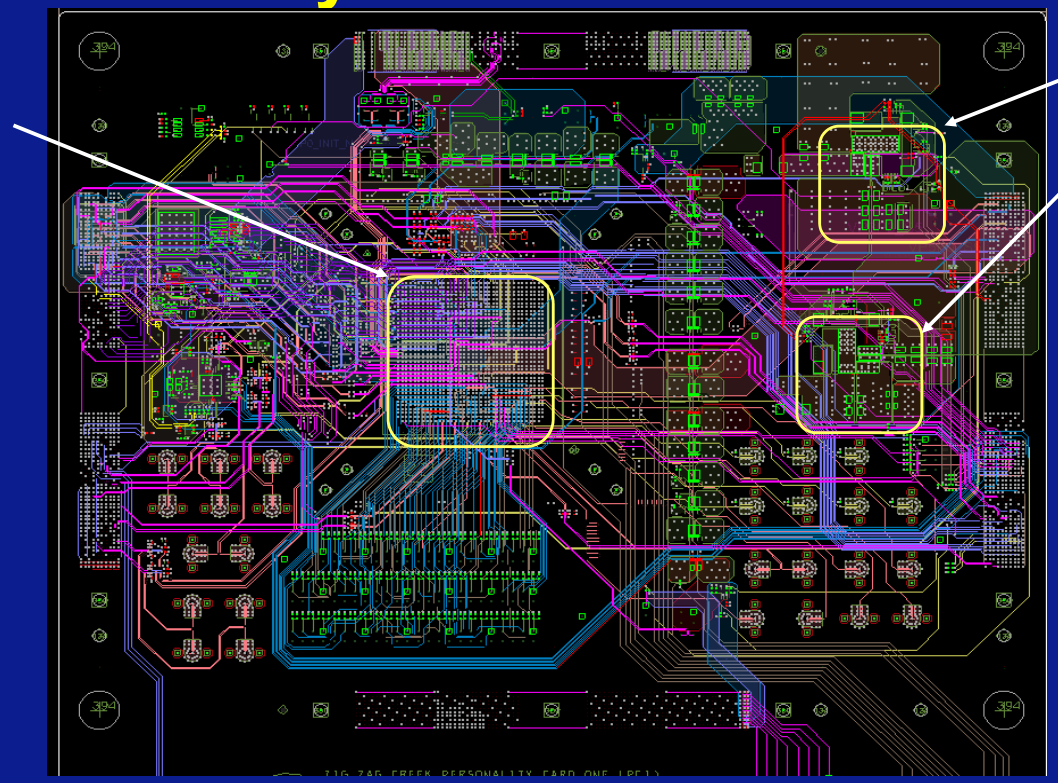
Objects		Types		Thickness
#	Name	Layer	Layer Function	Value mm
		Dielectric	Dielectric	0.08382
14	L14_PWR	Plane	Plane	0.03048
		Dielectric	Dielectric	0.0635
15	L15_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.08382
16	L16_PWR	Plane	Plane	0.03048
		Dielectric	Dielectric	0.0762
17	L17_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.10414
18	L18_PWR	Plane	Plane	0.03048
		Dielectric	Dielectric	0.1016
19	L19_GND	Plane	Plane	0.03048
		Dielectric	Dielectric	0.10414
20	L20_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.1016
21	L21_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.10414
22	L22_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.1016
23	L23_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.10414
24	L24_SIG	Conductor	Conductor	0.01524
		Dielectric	Dielectric	0.1016
25	L25_GND	Plane	Plane	0.01524
		Dielectric	Dielectric	0.09652
26	BOTTOM	Conductor	Conductor	0.03556
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.0127
		Surface		

Power layers:
L9, L11, L13,
L14,L16, L18

Ground layers:
L2, L4, L6, L8, L10
L12, L15, L17,L19
L21,L23, L25

Signal layers:
L3, L5, L7, L20, L22, L24

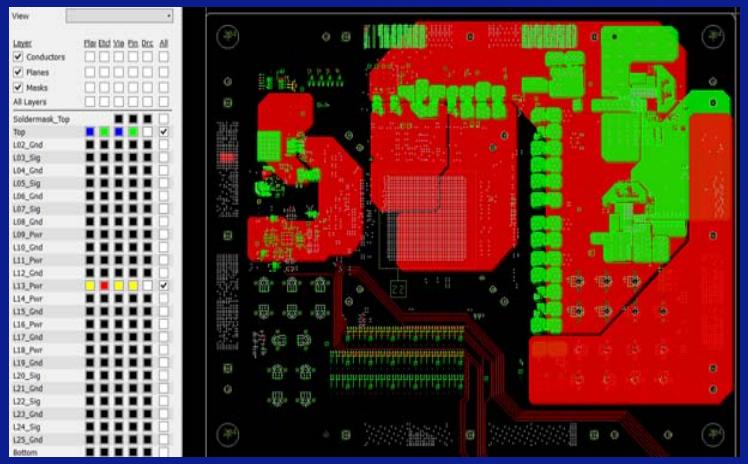
Daughter Card Layout

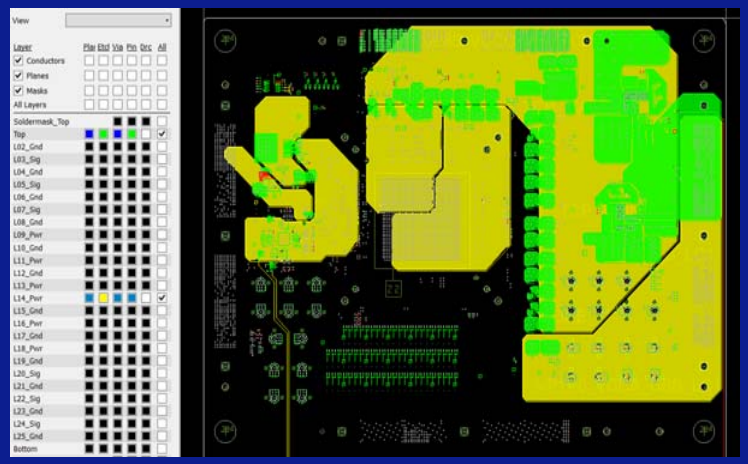


Power Delivery Network Design Strategies

- Power planes partition
- DC and AC Platform performance optimization
- AC noise and load transient minimization

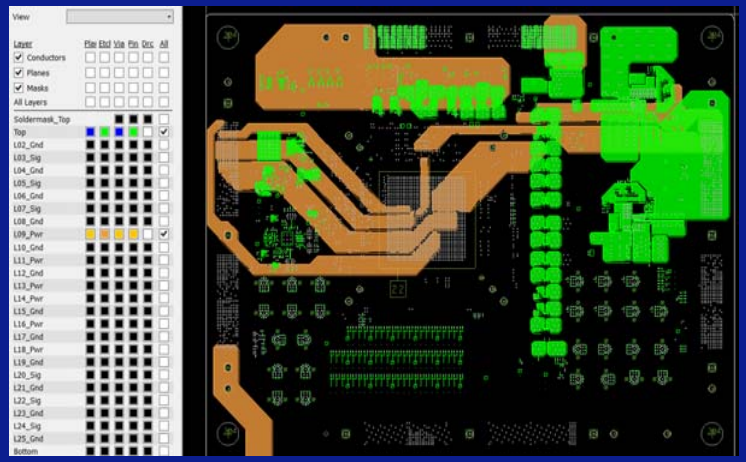
High Current Power Rails Planning

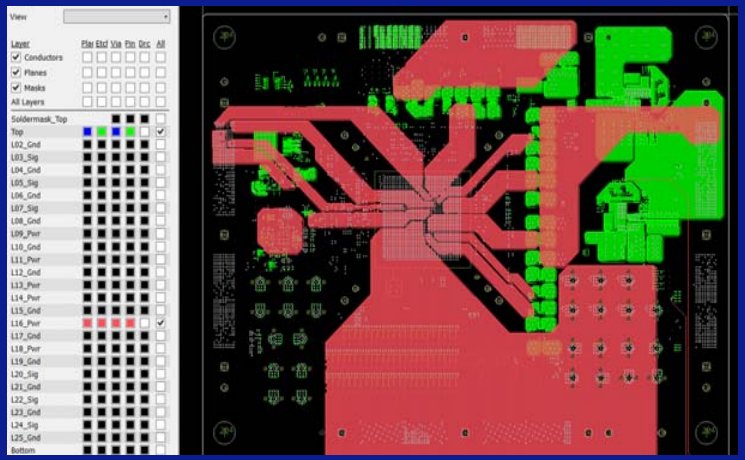




High current power rails use adjacent planes

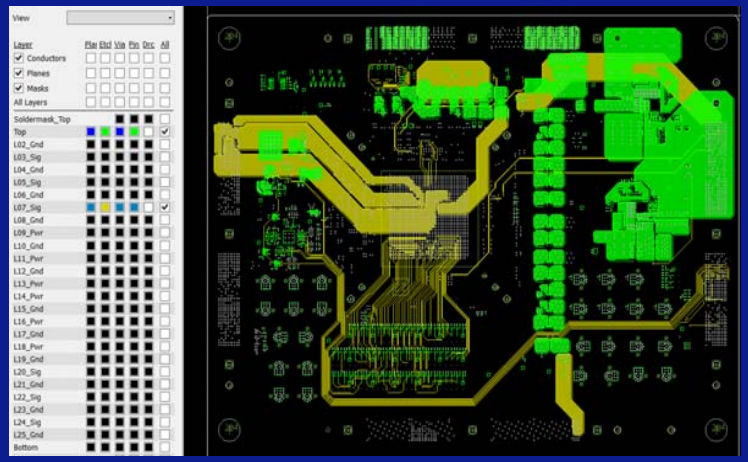
Low Current Power Rails Planning

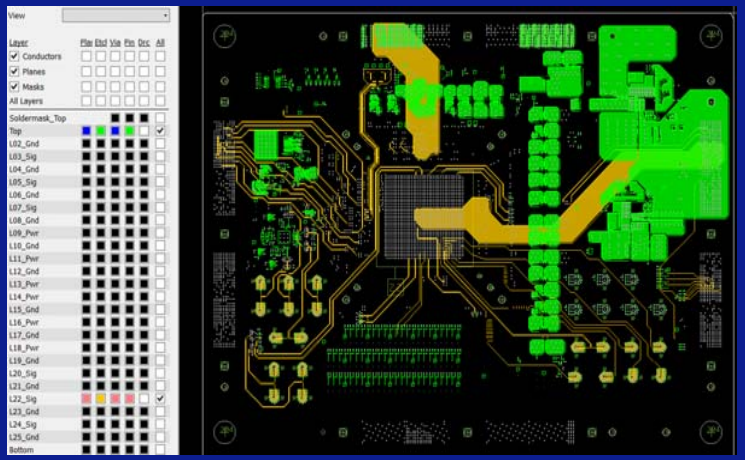




Low current power rails need proper space to avoid interferences

Low Current Power Rails Planning

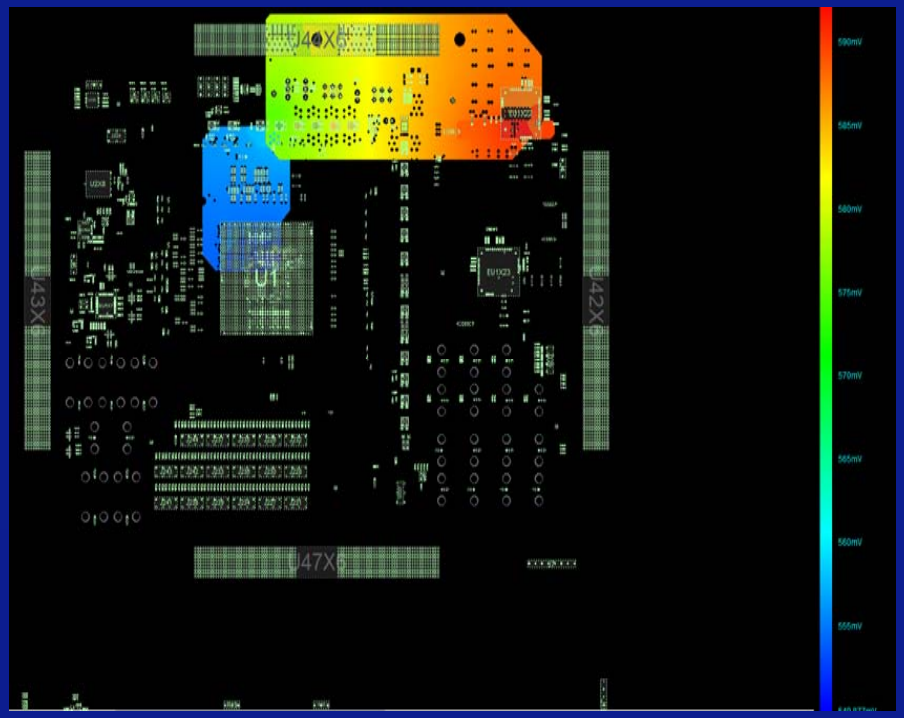




Platform Power Performance Optimization

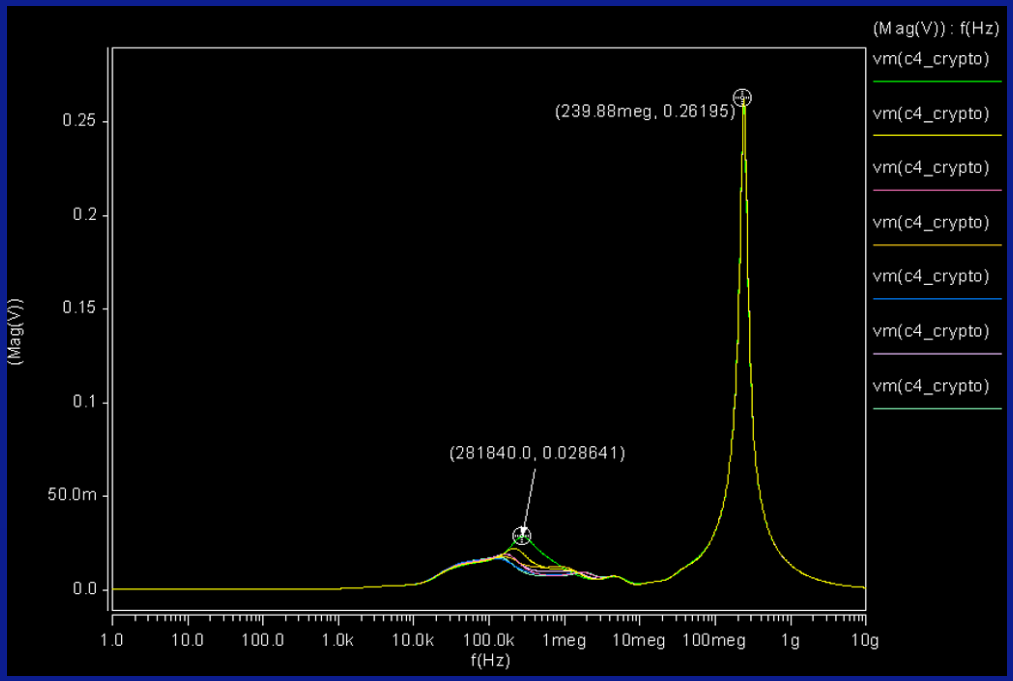
- Optimal placement of VRs
- Use of PowerDC (Cadence tool) to optimize power shapes
- Reduce power rails IR drop
- Use of PowerSI (Cadence tool) to reduce power rails impedance
- Isolation of power rails to reduce noise

Platform Performance IR Drop Optimization



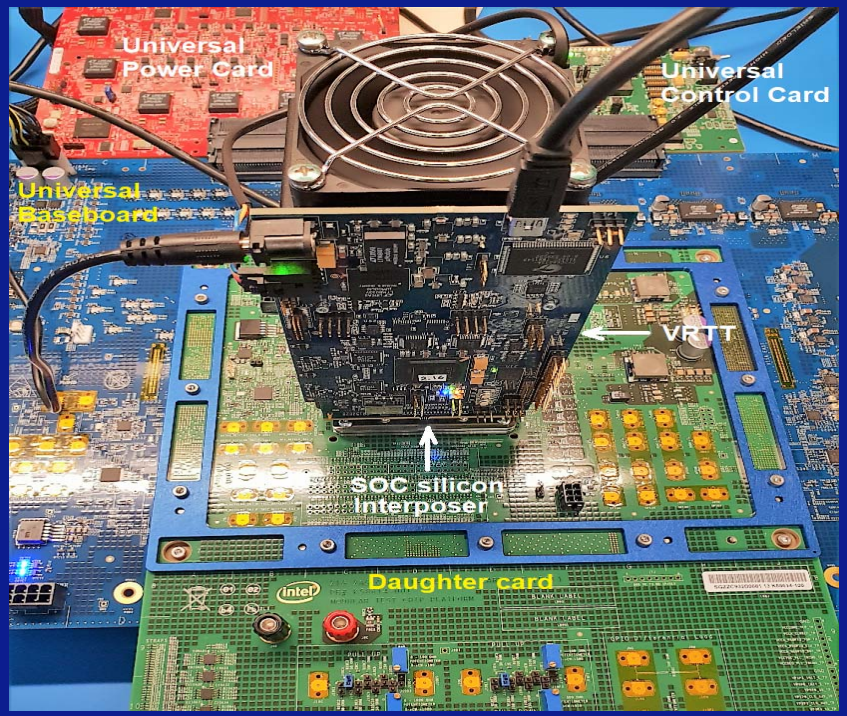
Identify IR hot spots

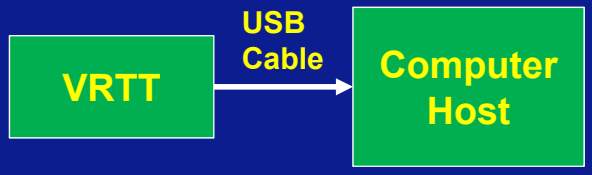
Platform Performance Impedance Optimization



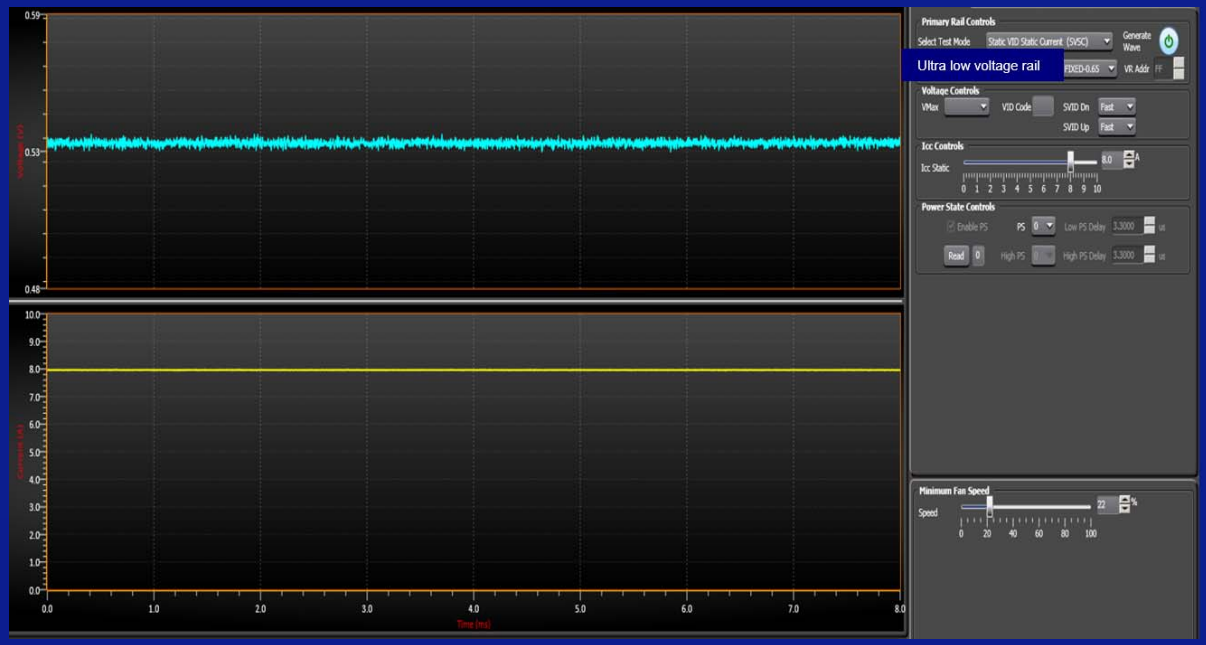
Power rail impedance needs to be minimized

Validation and Measurement Set Up



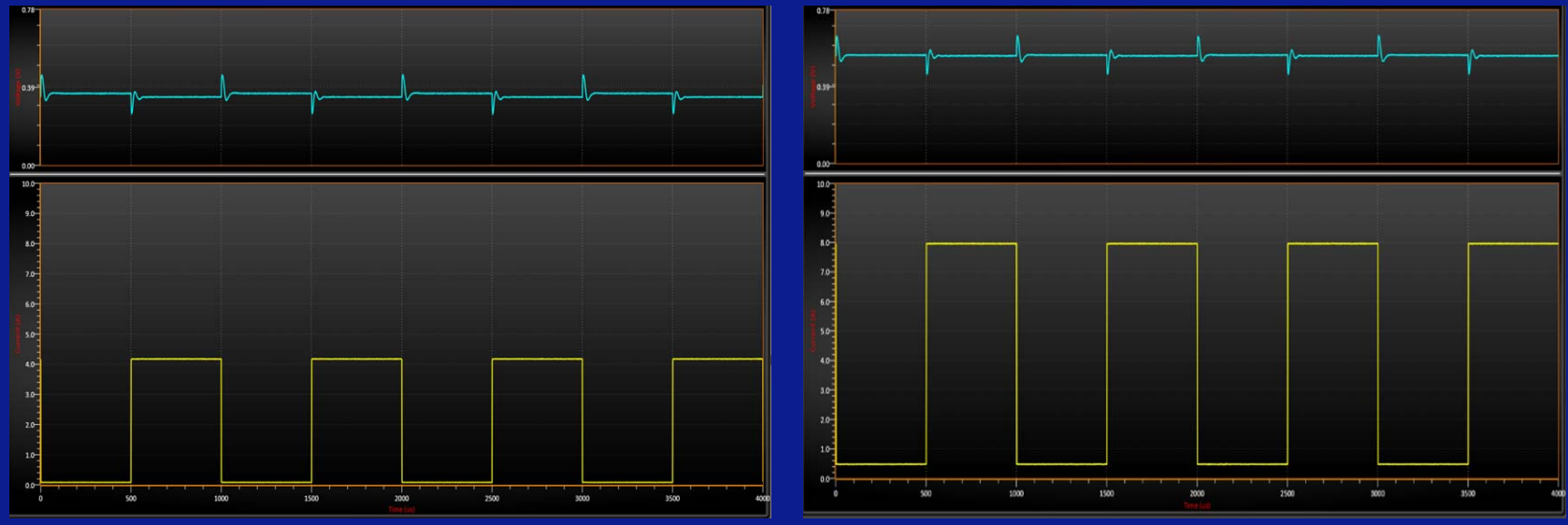


Measurement Data for DC Static Loading



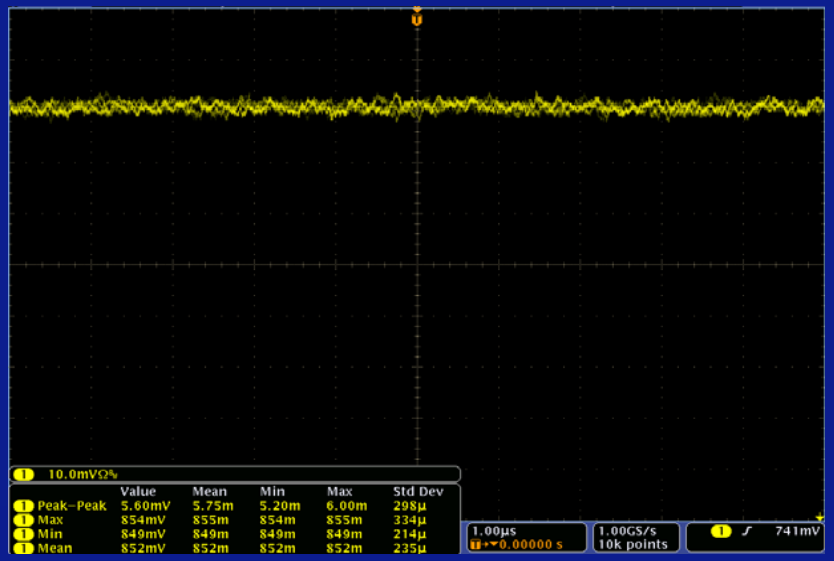
Voltage needs to be stable under heavy load

Measurement Data for Load Transient

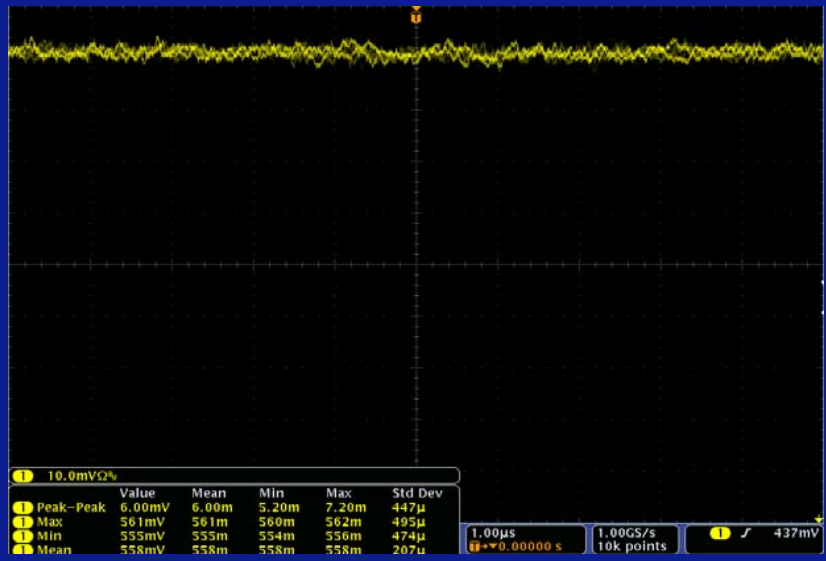


Voltage ripples need to be minimized under load transient

Measurement Data AC/DC Performance



Low voltage high current rail

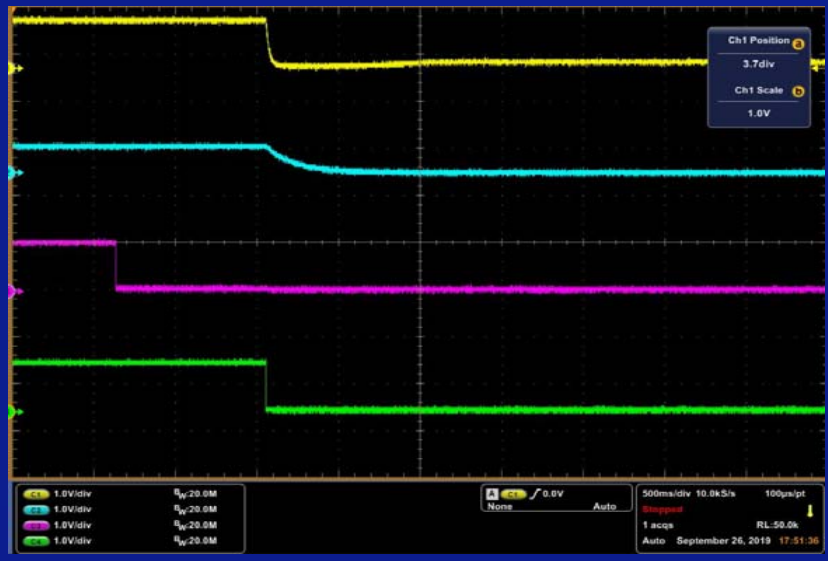


SoC silicon main core power rail

Peak to peak voltage < 10mV meets design spec.

Power Sequencing Control

Power Up Sequence



Power Down Sequence

This is an example, similar for other rails power up/down sequence

Summary

- Optimal power delivery is the key for successful sub-7nm SOC validation
- Multi-domain and ultra low voltage require optimal power planes partition
- IR drop and AC/DC noise should be minimized
- Tight load transient response to guarantee reliable operation

Acknowledgement

The author would like to thank Paul Marciniak, Dan Simon, and Ray Lamoreau for their support. Thanks also go to Rahima Mohammed and Naveid Rahmatullah for the reviews.