New Spins - Printed Circuit Boards (PCBs)

Accelerate PCB Design Using AI and Machine Learning-Based Smart Router

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Agenda

- PCB platform design process
- Technical challenges
- New intelligent routing technologies
- Case studies
- Summary





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PCB Platform Design Process

- Collect customers' requirements
- Generate schematic and netlist
- Plan PCB layer stackup
- Create layout constraints
- Place board components
- Route board



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Technical Challenges

- Diverse PCB platforms, i.e., analog, digital, and mixed signal designs
- Irregular routing patterns
- Complex and stringent layout constraints
- Manual and iterative process to arrive at an optimal routing solution





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Technical Challenges



- High density and high pin count package with over thousands of pins
- Very small interposer PCB geometry and limited routing space of 2"x3" or smaller
- Small BGA pitch size less than 1mm





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Manual Routing Bottleneck

- Most of the time is spent on routing the remaining 10% nets
- If no satisfactory solution is found, previous routings have to be erased
- Have to explore new strategies and start over
- This manual trial and error process continues until all nets are routed



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Disadvantages of Manual Routing

- Iterative process requires user intervention
- Sequential process means only one strategy can be done at a time
- Very labor intensive
- Costly in terms of time and layout resources
- Low return on investment



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New Intelligent Routing Technologies

- Machine learning based routing techniques
- Use of Genetic Algorithms to optimize route strategies
- Use of Neural Networks to evaluate effectiveness of each solution
- New router performance scales well with computing resources



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Al Routing Process

- Layer assignment (Via exploration and learning)
- Al directed global router is used for topological routing
- Detailed router transforms topological routes into DRC clean wires
- Delay and phase tuning
- Global and detailed routers co-optimization



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Evolutionary Via Strategy(Genetic Optimization)

Code	Action
A(n)	No Via on Layer N
B(n, m)	1 Via solution on layers n, m
C(n, m)	1 Via solution on layers n, m
D(a, d)	Move Via
E(n)	Bundle Solution on layer n
F(n)	Diff Pair on Layer n





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Via Strategy Actions



Connection using no via



Connection using one via between layer A(blue) and layer B(pink)





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GO Fitness Functions

Name	Description	Pro	Con	
Crossings	Returns the sum of the total number of connection crossings on each layer.	Fast, and easy to determine if the flow is working as it can be manually validated.	Does not consider congestion.	
RUDY	Returns the worst congestion given the probable routes	Better than Crossings with respect to accuracy and still fast.	Large approximation of the routing space, not very accurate.	
FGR	Returns the number of un- connects from a Fast Global Router	Extremely accurate	Slow	
CNN	Convolutional Neural Net trained on Actual Router	Somewhat accurate, instantaneous speed. Can be trained on different design styles.	Requires careful training.	

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Limitations of Evolutionary Via Strategy

- Will find a good solution (eventually)
- Each case is a ground up optimization process
- Inefficient use of information

What if this system could learn from past designs?



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Global and Detail Routers



Topological routes produced by the AI Global Router



Transformed routes from the detail router



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AI Smart Router Advantages

	Manual Routing	Legacy Auto Router	Al Smart Router
Stackup planning	\checkmark	✓	\checkmark
Constraints creation	\checkmark	\checkmark	\checkmark
Components placement	\checkmark	\checkmark	\checkmark
Routing	Manual and interactive	Using DO files and need debugging	✓ No any user involvements
Speed	Labor intensive. Very slow	Improved speed for some simple designs	✓ Full automatic and very fast
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CPU N-1 Interposer



Manually routed and tuned CPU N-1 interposer (120 hours)



Automatic routings of N-1 CPU interposer using the AI Global router (45 minutes)



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PCB Complexity and Routing Challenges

- Complex BGA escape/fanout
- Power plane generation
- Advanced design constraints

Name	Completion	Nets	Wires	Vias	Layers
Another type of Interposer	100	2041	8787	13820	14
Open Source PCB 1	100	387	1293	2371	6
Open Source PCB 2	99	431	1481	2665	8
Modular Validation Board	95	912	850	1729	14



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Future Plans

- Implement reinforcement learning via strategy
- Expand RL framework to include component placement and metal fill
- Incorporate SI/PI/Thermal reward generators
- Layer utilization efficiency improvement
- Analysis driven optimization
- Constraint harvesting





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Summary

- PCB platform design is a complex and time consuming process
- Manual routing methods are no longer able to meet time to market requirements
- Machine learning based AI smart router drastically accelerates the PCB design process



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