Challenges and Solutions for Characterizing 112G PAM4 Signals

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Product Test Cycle

- **Wafer test**
  - Wafer sort
  - Design screening

- **Packaged test**
  - Does IC meet specification?

- **Product test**
  - Does product meet its specifications?

- **System test**
  - Does product meet requirements in its intended application?

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ATE Strategy

2018

Instruments integrated in load boards

2019

Instruments redesigned to become an Advantest V93000 test-head extender

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Features needed for ATE success

ATE Firmware 10x faster than benchtop

Bit Error Rate Tester (BERT)
- Pulse Pattern Generator (PPG)
  - PRBS7-31, PRBS13Q/31Q, SSPRQ
  - Tx equalization (pre- and post-emphasis)
  - Error insertion
  - Gray coding, polarity inversion
- Error Detector (ED)
  - Feed Forward Equalizer (FFE)
  - Decision Feedback Equalizer (DFE)
  - BER counters
  - FFE Equalizers with reflection cancellation and DFE

Digital Storage Oscilloscope (DSO)
- Fast acquisition, FPGA-based
- Sensitivity: 10 mVpp to 1200 mVpp
- Intrinsic Jitter: 200 fs rms
- Full Eye and Mask measurements
- SSPRQ & up to PRBS16 pattern lock
- Jitter Decomposition (TJ, RJ, DJ)
- Continuous Time Linear Equalizer (CTLE), S2P De-embedding, FFE, DFE, etc.
- NRZ and PAM measurement Libraries (APIs)
- Memory depth: $2^{16}$ Pattern Length
- Fast sampling rate > 100 MHz
Why PAM4?

Transmission channels are lossy
- 10 dB at 13 GHz typical

Modulator bandwidths are limited
- 40 GHz available today

PAM4 Modulation
- Same data throughput at half the frequency
- Double data rate at the same frequency
- 2 bits/symbol, data rate = 2 x symbol rate

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TDECQ – The New Transmitter Figure of Merit

Transmitter Dispersion Eye Closure (Quaternary)

- “New” mask margin test for PAM4 - predictor of system performance
- dB ratio of how much noise can be added to the transmitter signal vs. an ideal signal, at a target symbol error ratio
- Mimics behavior of a real receiver after equalization
- ATE instrument should be able to perform at speed TDECQ measurements
- Good correlation between TDECQ and link performance

\[ TDECQ = 10 \log_{10} \left( \frac{QMA_{\text{outer}}}{6} \times \frac{1}{Q \cdot R} \right) \]

R is noise margin at a fixed symbol error rate
- Higher R is better
- Lower TDECQ is better

Other measurements:
- Linearity
- Eye width, eye height
- Skew
Channel Effects
Problem Statement

Channel effects

- Impaired signal at DUT, coming from instrument
- Impaired signal at instrument, coming from DUT
De-embedding of Channel Effects
3 Methods

**Method-1:** DSO de-embedding
- Use s-parameters to de-embed channel effect
- S-parameters can be from VNA, simulation, or DSO

**Method-2:** FFE taps generated by DSO are used to configure the PPG signal shaper to compensate for channel losses

**Method-3:** Error detector of the BERT uses an equalizer (FFE, DFE, CTLE) to compensate for channel losses
**Method-1: DSO de-embedding**

- **DSO** measures and de-embeds the channel in frequency domain.
- **DUT** signal after compensating for the trace losses.

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Method-2: PPG Signal Shaper

- PPG
- ED
- Blind-Mate Connector
- DUT
- DSO

Distorted signal from channel → DSO calculates FFE taps → FFE taps from DSO loaded in PPG
Calibration - Calkit
Fully Automated Cal Procedure

- Calkit has load board form factor
- It contains all the cables and brackets for quick mount

PCB Cut-out

Calibration:
PPG to DUT Path Compensation
DSO to DUT Path Compensation

ML4035

- Simply undock load board and mount Calkit instead
- No need to touch the ML cassettes
- Quick connect to external calibration reference ML4035
- ML4035 cabling de-embedded
Multi-purpose ATE Testing

Reconfigurable Load Board with Personality Daughter Cards

- Simplified Reconfigurable Load Board Design
- Solution to test high port count devices (AI, Ethernet Switch, etc.)
- Characterization, HVM, Thermal, and SLT applications
- Modular personality cards for different applications
- Flexibility to test a DUT on the same platform for R&D and HVM
- Access to external and internal instrumentation
- Access for probing control and power
Example: High Lane Count High Speed Input/Output System

Exploded 3D View

- ATE Load Board
- MultiLane Instruments
- V93000 ATE Tester Extender Frame
- MultiLane Daughter Cards
- DUT
Load board Topologies

With Docking Plate for NS6040 Handler

Without Docking Plate

Daughter Cards

Up to 8 Daughter Cards for a Total of 256 Differential High-Speed Lanes

GPIO to tester resources (I2C, MDIO, Power)
Daughter Card Variety Per Test Requirements

- Optics
- 18 dB Loopbacks
- Splitters/Break-out
- Golden DUT
- PCIe 5.0
- RF Switches
- 0 dB Loopbacks
Personality Cards

1. Passive Loopback with different loss profiles
   a) 0 dB, 12 dB, etc.
2. Loopback with crosstalk injection circuitry
3. Resistive Splitters & Switches with access to instruments in the Twinning
4. HSIO Lanes to high density coax from either top or bottom
5. SLT with optical modules
6. PCIe Gen5 compliance card
7. Active Instrument cards
8. Golden DUT
Personality Card - QSFP-DD

Daughter Card for 32 differential TX and 32 differential RX

QSFP double-density optical modules
Personality Card - X dB Loopbacks + Crosstalk Option

- Enhanced BIST
- Allows controlled noise injection
- Allows separate TX and RX Characterization

0 dB loopbacks realized with shorts between the individual TX/RX pairs

Passive Differential Loopback Traces with 6 dB, 12 dB, 18 dB loss profile at Nyquist with programmable crosstalk (options)
Personality Card - Resistive Splitter

PCIe 5.0 DUT  Daughter Card

32  32  32  32

ML SI Instrument
Personality Card - Splitters / RF Switches / Bias-Tees

- 60 GHz RF switches
- Bank of 40 GHz Splitters
- Bank of 40 GHz Wideband Bias-Tees
Application – Example TIA/Driver Testing

AT-series BERTs / TDRs

AT-series DSOs

AT-series BERTs

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Application – Example TIA/Driver Testing

BER vs input power

Eye diagram – non-linearity/imbalance

Gain curve vs input power/bandwidth control
Conclusions

• 112G - 56 GBd PAM4 - is the new electrical/optical high-speed Ethernet standard
• Testing required from wafer level to system test
• 112G BERT & DSO Solutions available in ATE format
• Signal Integrity measurements require special attention
• Multi-purpose ATE test solution to enable the full product test cycle
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