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Archive

Embedding Reliability Detection for Zero Field Failures

Nigel G Kissaun
ELES Semiconductor Equipment

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Shanghai ▪ October 29, 2019

ELES

Automotive vs Consumer Requirements

Stringent application environment in Automotive

Consumer	Automotive
	
Temperature range: **0°C – 40°C**	Temperature range: **-40°C – 150°C**
Operating time: 3 – 5 years	Operating time: 15 years
Vibration: negligible	Vibration: 0 – 2000 Hz
Acceleration: negligible	Acceleration: 500 m/s²
Tolerated failure rate: **1000 ppm**	Tolerated failure rate: **target zero defect**
Documented failures: no	Documented failures: yes
Change management: no	Change management: yes
Long term supply: no	Long term supply: up to 30 years

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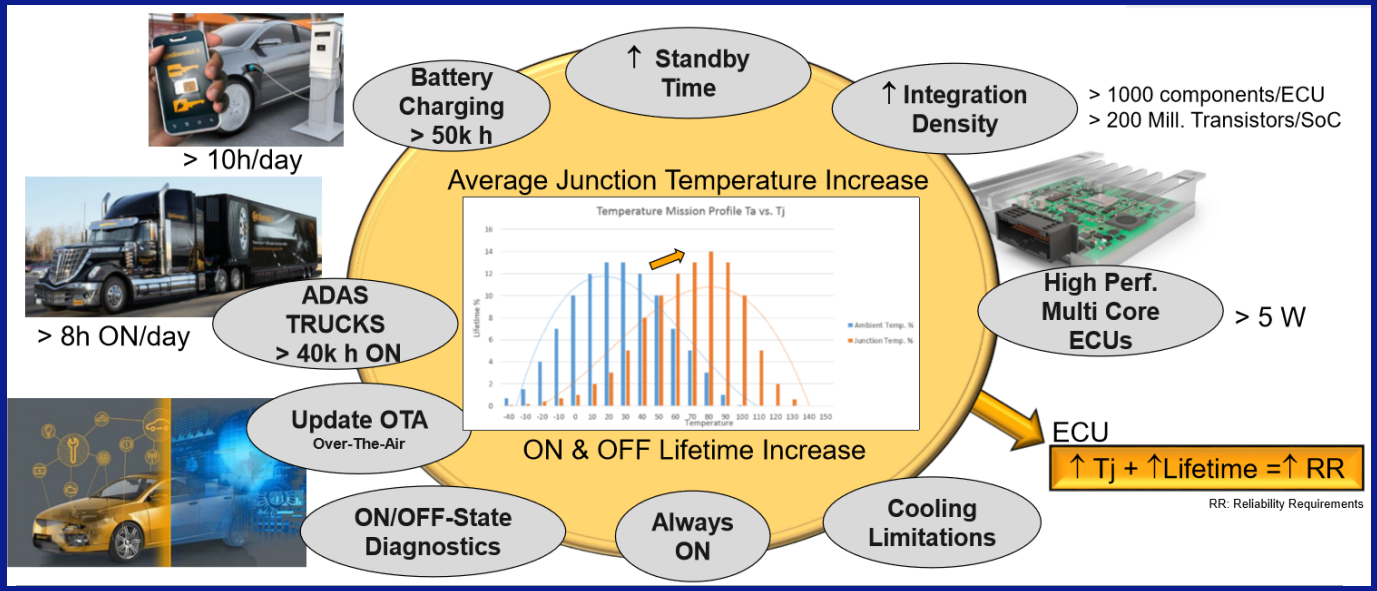
Increasing Requirements of Automotive



AEC Reliability Workshop 2018, Carsten Olhoff, Continental Group

Car Sharing, Overnight Battery Charging and OTA s/w updates → Increase in hours of use per day

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Impact of Automotive Failures

Zero Failures Goal

Audi

- **7.000 semiconductors per car**
- **4.000 cars** turned out **per day**
- **1/ppm failure rate = 28 defective cars** per day

BMW

- **3.500 semiconductors per car**
- **10.000 cars** turned out **per day**
- **1/ppm failure rate = 35 defective cars** per day

The **impact of Non-Reliability** is too high.

The **reputational damage** deriving from a failure in semiconductor devices could mean consumers are less likely to buy their next car from the same company

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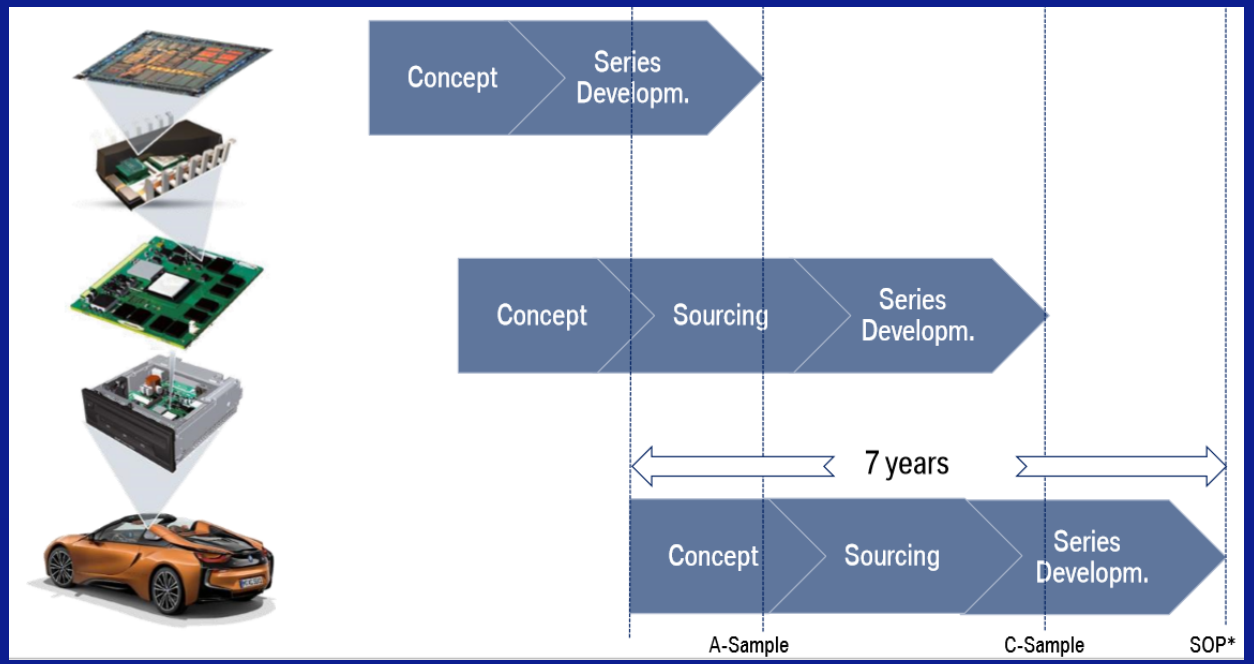
Current Car Model Time-to-Market



'Quality & Reliability as an Enabler for Future Automotive Electronics', Dr Oliver Senftleben, BMW Group

Traditional Supplier-Customer Staggered Approach

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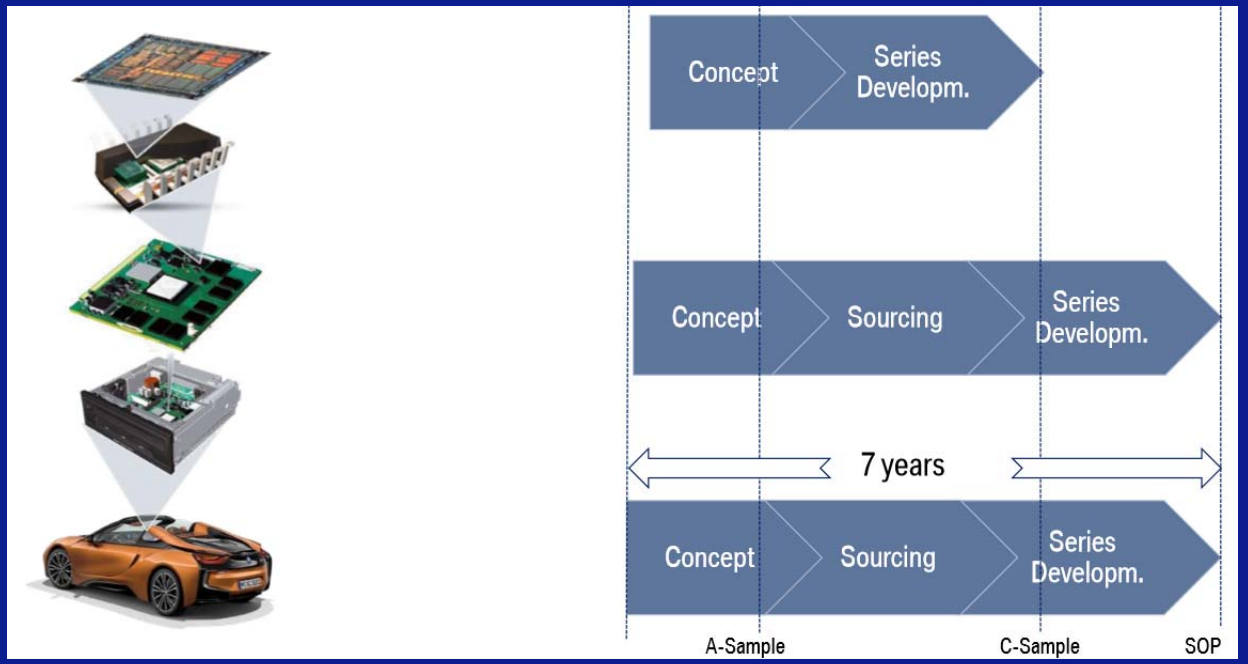
Future Car Models Time-to-Market

Semiconductor Supplier

Module (Tier1) Supplier

Car Manufacturer



'Quality & Reliability as an Enabler for Future Automotive Electronics', Dr Oliver Senftleben, BMW Group

Concurrent Approach to reduce Time-to-Market

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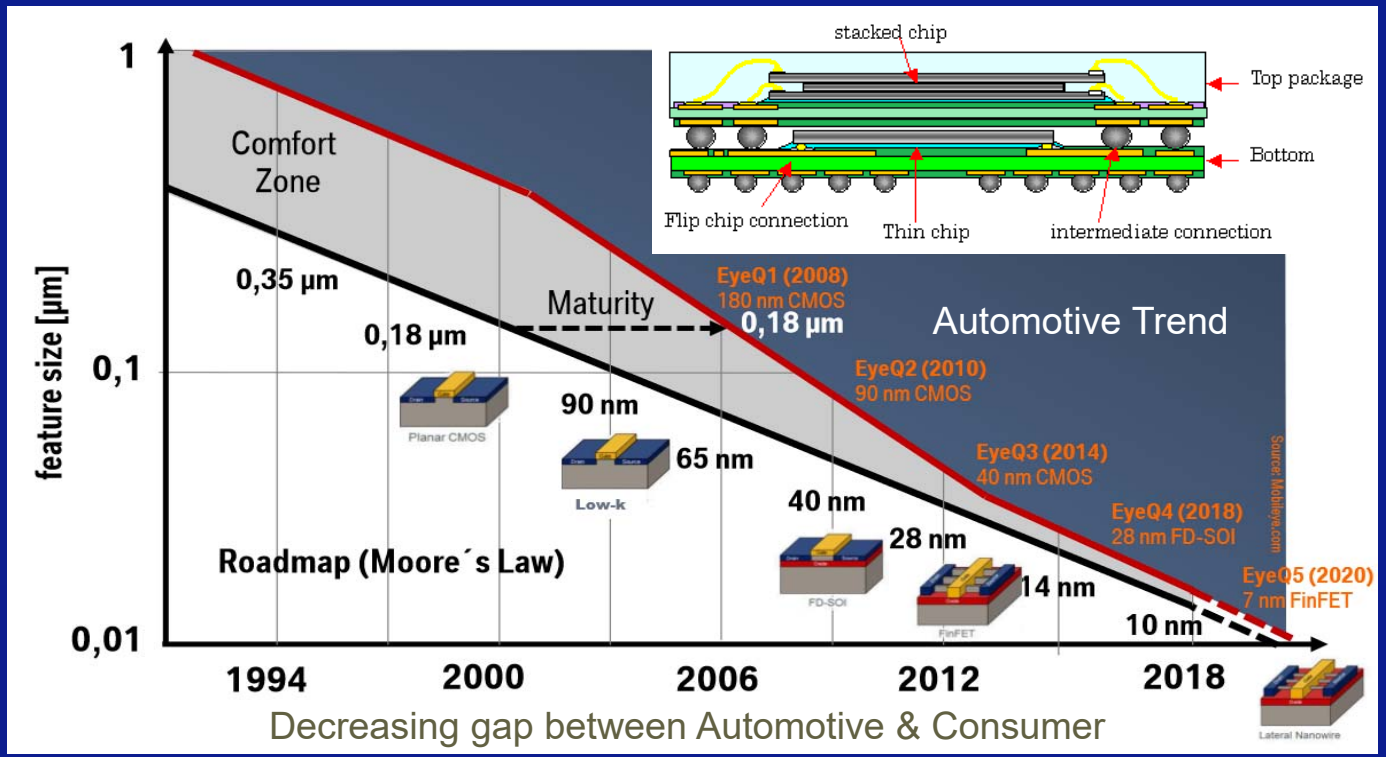
Automotive IC Technology Trend vs Moore's Law



"Complexity, Quality and Robustness - The Challenges of Tomorrow's Automotive Electronics", U. Abelein, H.Lochner, D. Hahn, S. Straube

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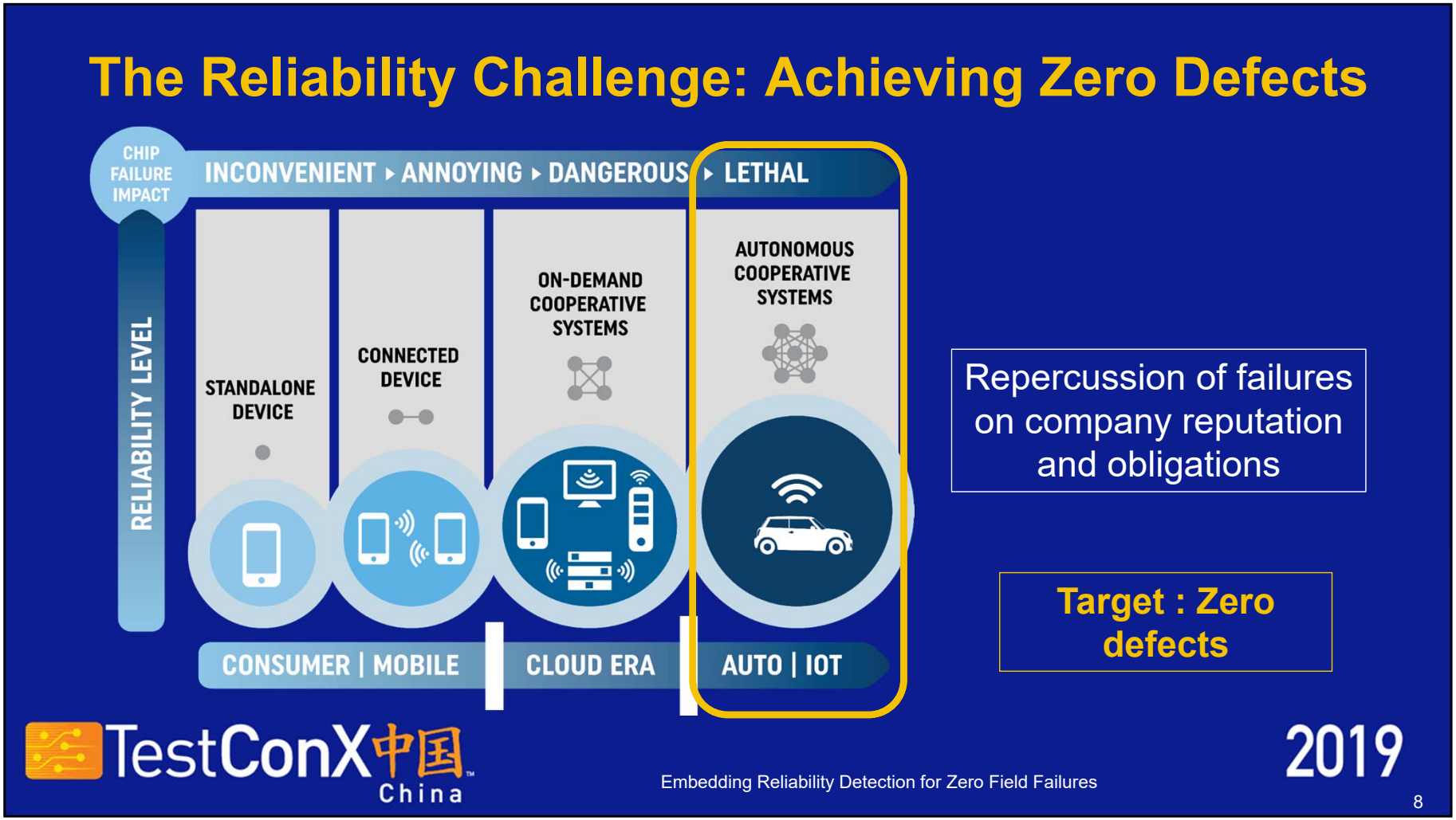

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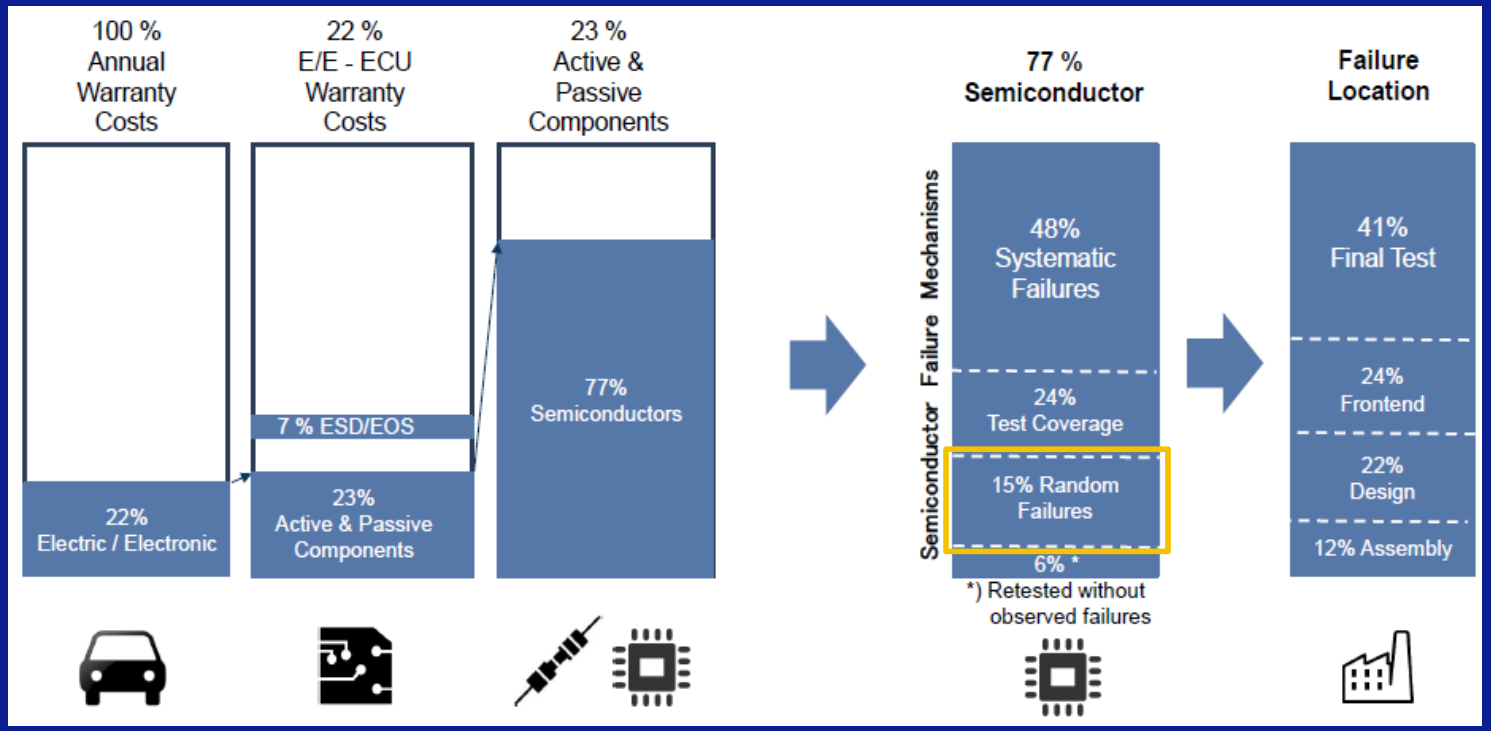
Random Semiconductor Failures in the Distribution of Automotive Field Failures



'Semiconductor Management at BMW Group', Reinhard Sttadler Apr 2017

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Time-dependent Classification of Faults in Semiconductors

Permanent Faults: Repeatable failures due to irreversible physical changes.

Transient Faults: Non-repeatable failures in random locations, induced by temporary environmental conditions (Cosmic rays, EMI).

Intermittent Faults: Fault may or may not always induce an error, but when it does, it occurs in the same location due to unstable or marginal hardware.

- Intermittent faults are a major source of errors in ICs
- Root cause ranges from manufacturing residuals to oxide breakdown
- Intermittent faults are activated and deactivated by voltage, frequency, and temperature variations.
- The increasing circuit complexity is expected to increase the likelihood of intermittent faults, despite extensive use of fault avoidance techniques.

'Intermittent Faults & Effects on Reliability of ICs', Cristian Constantinescu, Reliability & Maintainability Symposium, 2008

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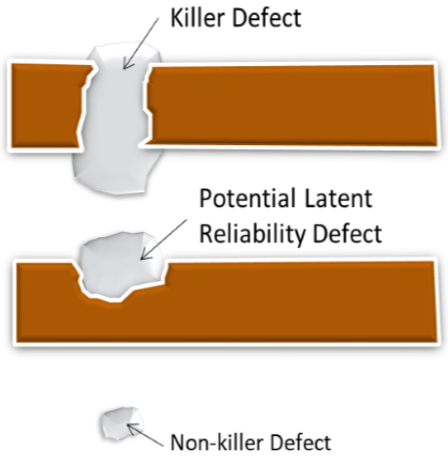
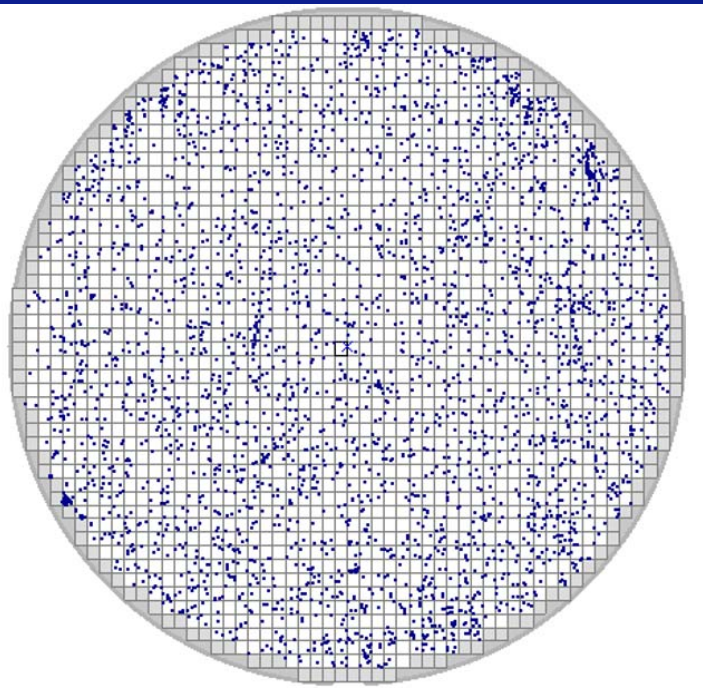
Which Defects Matter?

Overkill = Yield Loss => Cost

Top view of two metal tracks.





Potential Defects vs Potential Failures

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Key trends Driving the Need for Reliabilty Improvement

1. Increasing demands on the use of the car
2. Increase in the Semiconductor components per car
3. Reduction of Time-to-market of car models
4. New applications needing new technologies with lower maturity

All four trends are increasing the reliability risk

To address this challenge, we'll present here an effective methodology called RETE.

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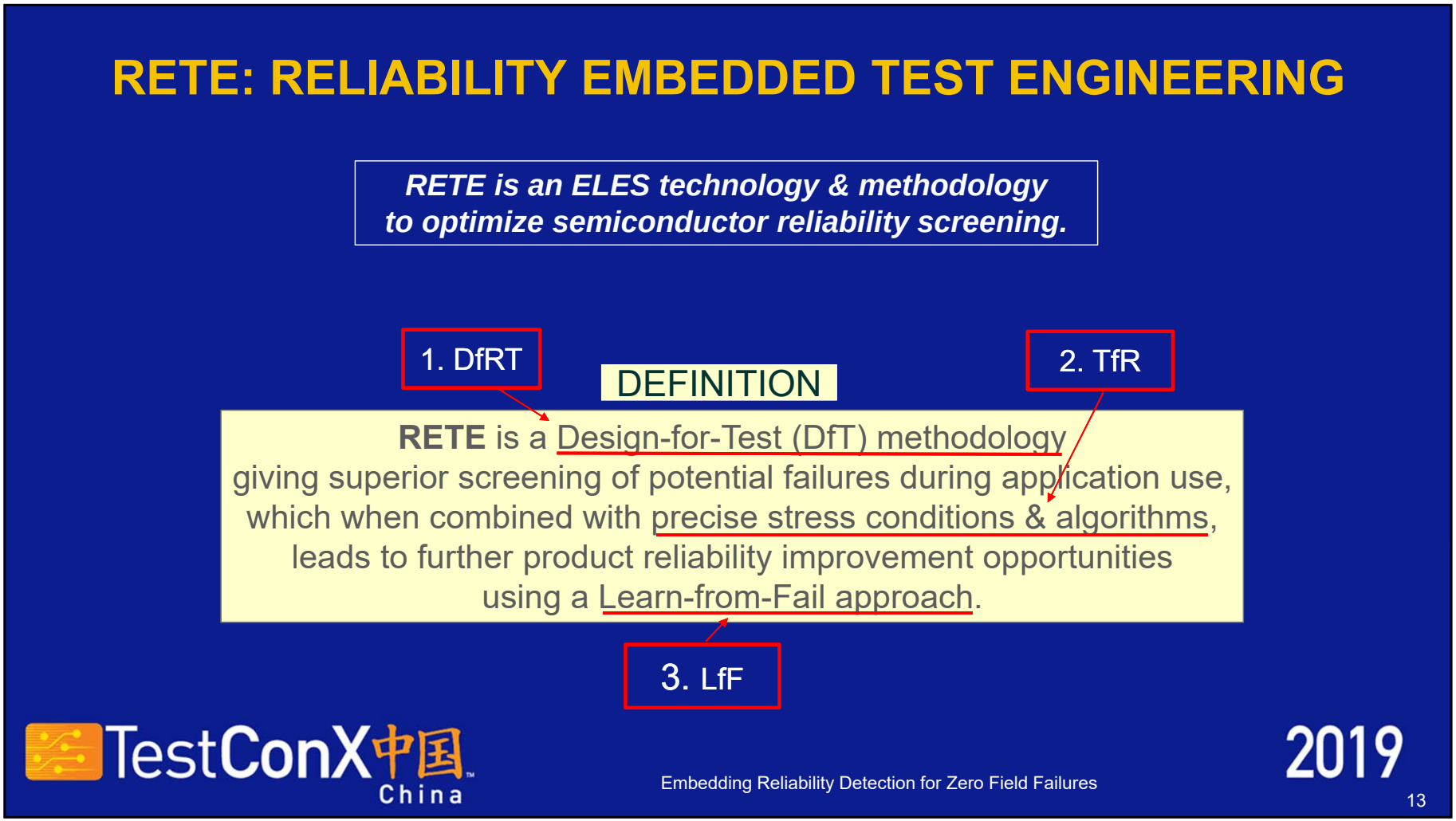
RETE: RELIABILITY EMBEDDED TEST ENGINEERING
RETE is an ELES technology & methodology to optimize semiconductor reliability screening.
1. DfRT
2. TfR
DEFINITION
RETE is a Design-for-Test (DfT) methodology giving superior screening of potential failures during application use, which when combined with precise stress conditions & algorithms, leads to further product reliability improvement opportunities using a Learn-from-Fail approach.
3. LfF
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RETE Flow for a New Device

1. RETE DfRT :-

1) Review:	Check product against each item in the RETE DfRT Checklist.
2) Compliance:	Calculate the overall compliance index.
3) Gap Analysis:	Identify all the DfRT opportunities.
4) Proposal:	Recommend DfRT improvements to the product.

2. RETE TfR :-

1) Stress Matrix:	Define the stress conditions V/I, temp, freq, cycles.
2) TFR Algorithms:	The screening Algorithms followed by immediate test.
3) Total Test:	DfT Testing during Burn-in - use of ATE Tests.

3. RETE LfF :-

1) Realtime Analysis:	Realtime fail tracking with decryption (RTI) for fast feedback.
2) Adaptive Flow:	Adaptive Test based on external data inputs (EWS, FT, aging).
3) Offline Analysis:	Data to help identify root cause of failures & corrective action.

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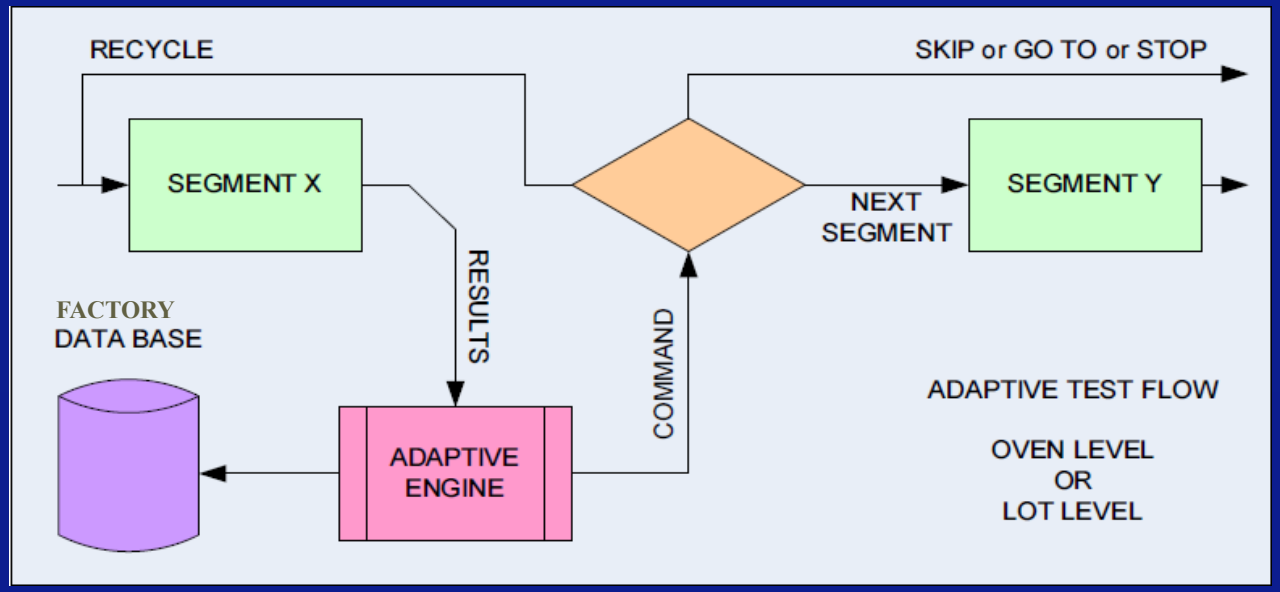
Adaptive Learn-from-Fail (LfF)

The flow of testing can change on the fly based on results or inputs coming from other data sources such as Probe, Final Test, Aging Data Results, Big Data, Non-conforming lots.



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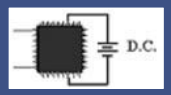
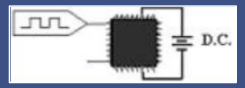
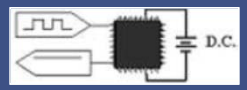
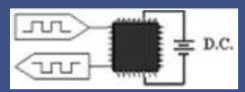
The Evolution of Stress Methods in Production

STRESS METHOD	SCHEMATIC	DESCRIPTION
Static		IC is stressed at static and constant conditions, IC is not toggling.
Dynamic		Input stimulus for toggling device's internal nodes.
Monitored		Input stimulus for toggling device's internal nodes and real-time monitoring of IC signals.
TDBI (Testing during Burn-in)		Input stimulus for toggling device's internal nodes, monitoring results and taking decisions on the part.

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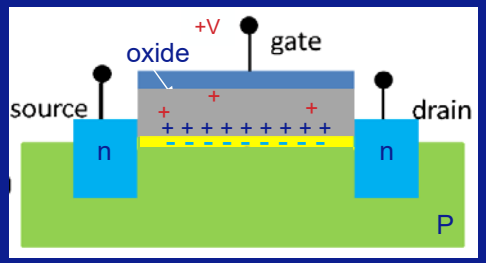
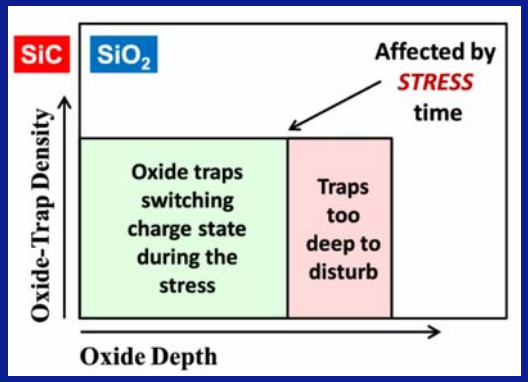
Catching Intermittent Faults – Trapped Charges





- One failure mode is intermittent trapped charges in Silicon Dioxide
- The trapped charges are harmless as long as they don't move
- However with aging (simulated by temp & voltage stress) the trapped charges tunnel through the oxide and shift the Threshold Voltage
- Removal of the stress, resets the drift and trace of the fault disappears
- Traps can be significant in Silicon Carbide technology, the future of Automotive Power Electronics
- AEC Q100 specifies to test within 96hours, but for the Vt to be seen, it needs to be tested immediately.

Ref: SiC MOSFET Reliability and Implications for Qualification Testing.
Aivars J. Lelis, Ronald Green, and Daniel B. Habersat, U.S. Army Research Lab, Adelphi.
2017 IEEE International Reliability Physics Symposium (IRPS).

So Test needs to be done straight after removal of stress in the same Chamber, to observe drift in Vt due to intermittent trapped charges.

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ART200 Base System

DfT Test Platform (per slot)

- 288 I/O channels - 20MHz Test Rate
- Flexible Algorithmic Pattern Generator
- 512Mb onboard pattern memory (64MV)
- On-the-fly fast pattern reloading
- Real time monitoring & logging
- V / I measurement capability

Power Supply Platform (per slot)

- #6 basic power supplies ±20V-60W

Thermal Platform (2 chambers)

- #2 Temp zones, up to #12 Test slots each
- Temperature range -40°C to 150°C
- Temp Uniformity / Accuracy: ±3 °C @2KW
- Temp gradient: up to 5° C /min (DUTs off)
- PLC oven control, self diagnostic, facilities log
- More than 2 x 9KW dissipated
- Balanced fans for very low vibration
- Automation: sliding doors, remote control
- System Health monitoring

HTOL Qualification & Production Burn-in

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ART200hp Hybrid for High Power Dissipation

Local Temperature Control per device with:

- **Air Cooling for dissipation up to 150W per device**
- **Liquid Cooling for dissipation up to 1000W per device**

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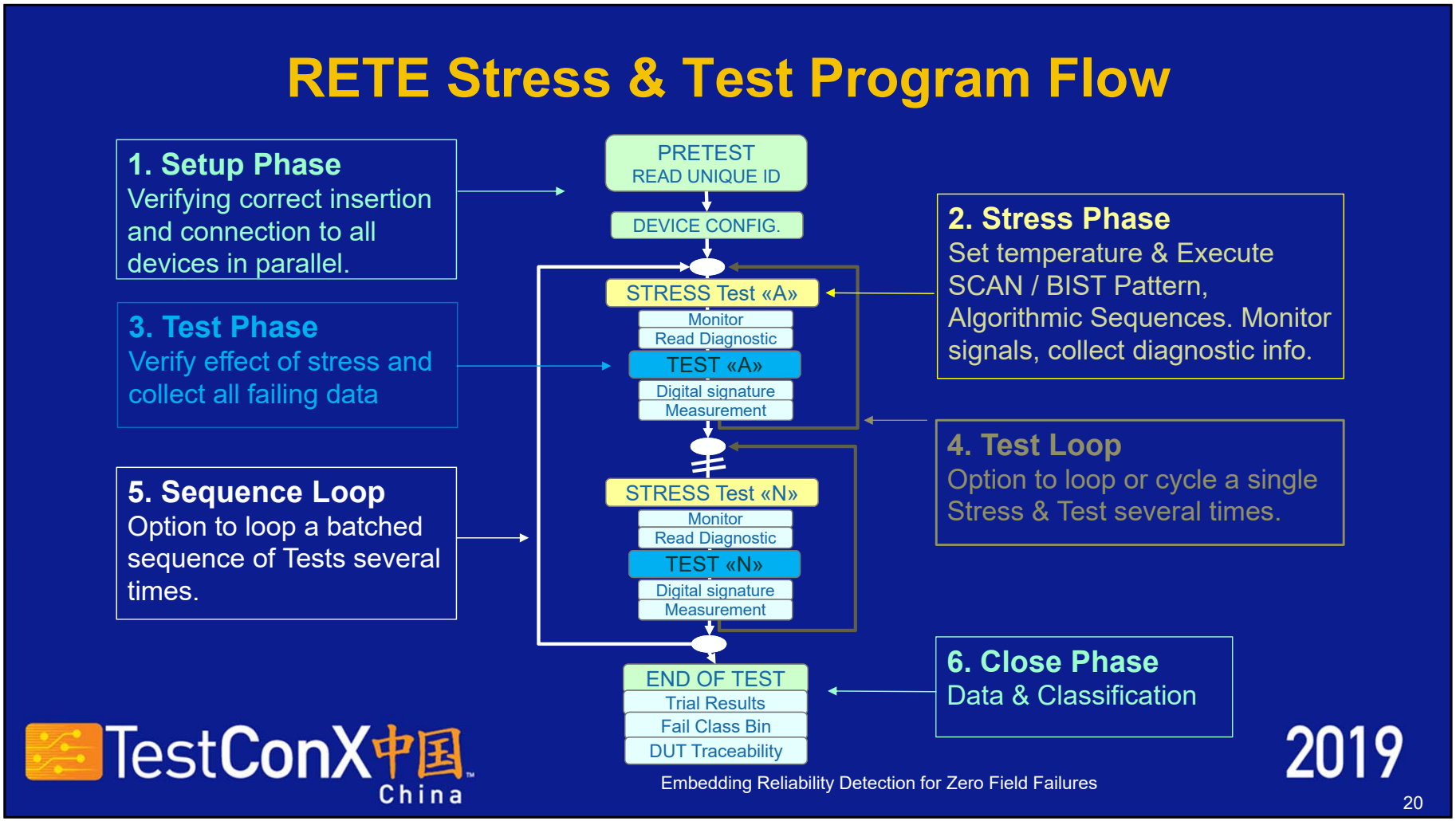
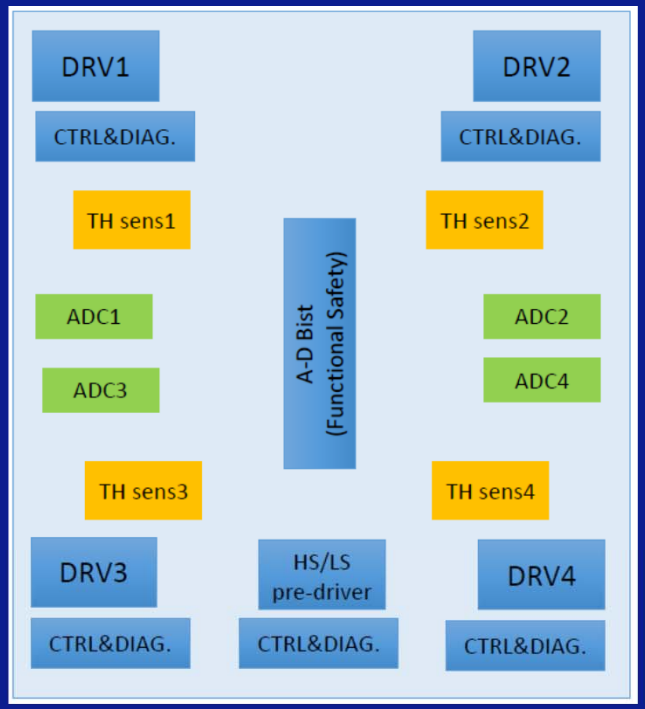
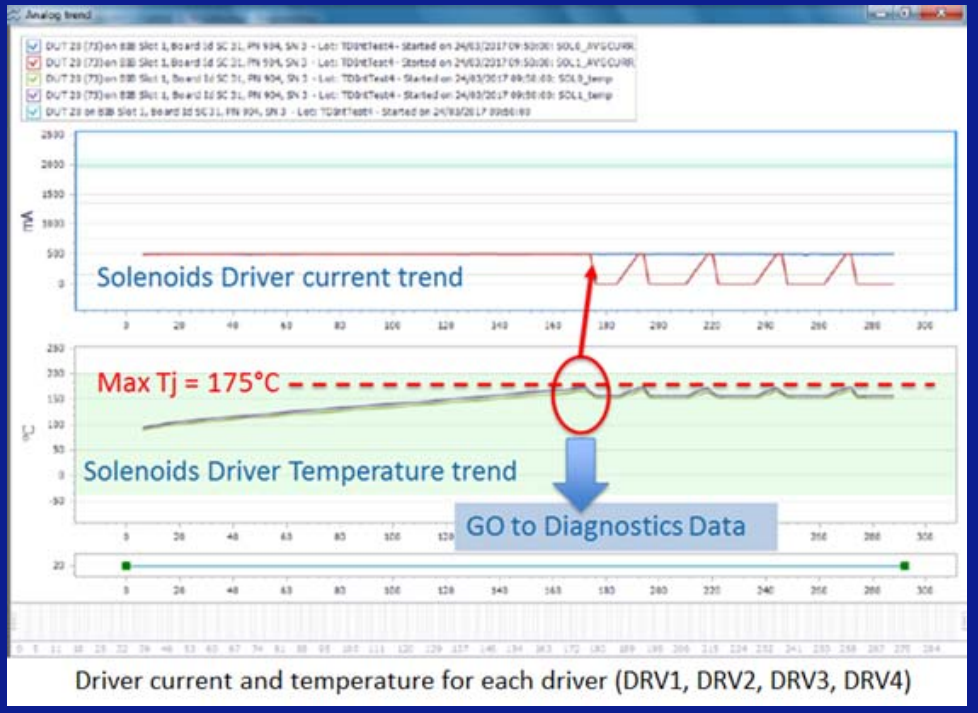


RETE on Mixed Signal Automotive





Driver current and temperature for each driver (DRV1, DRV2, DRV3, DRV4)

During qualification, Thermal sensor on Output Driver 2 detects >175'C and goes into a controlled shutdown.

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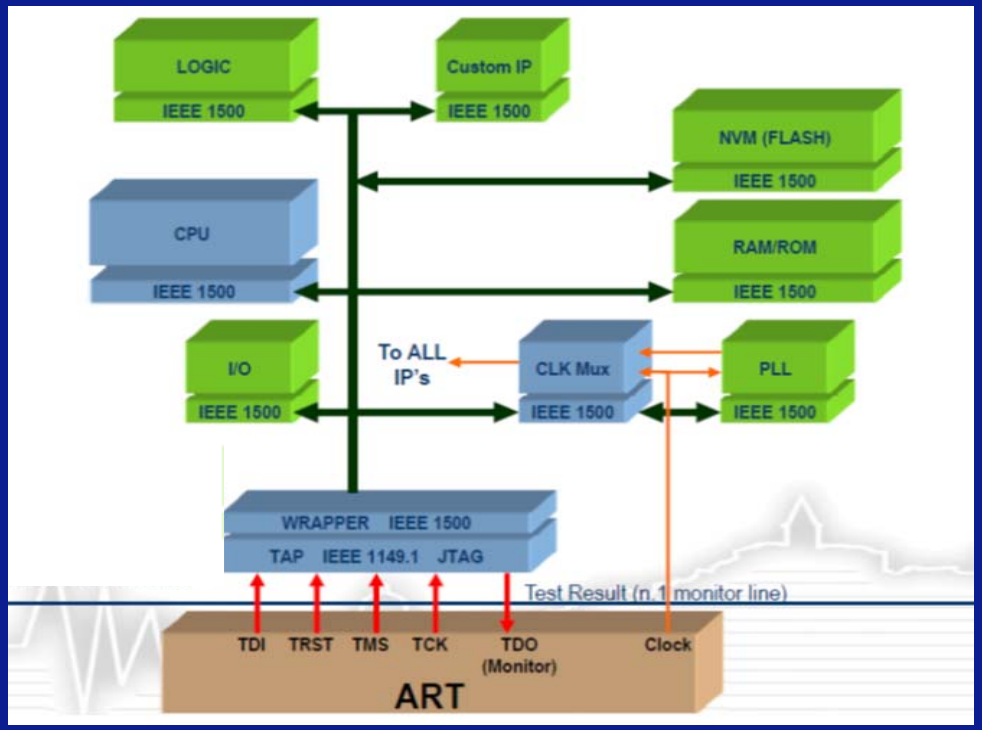
RETE on MCU with E-Flash



BIST multiplexer allows chip 10MHz clock to be sped up by connecting directly to the PLL at 1GHz.

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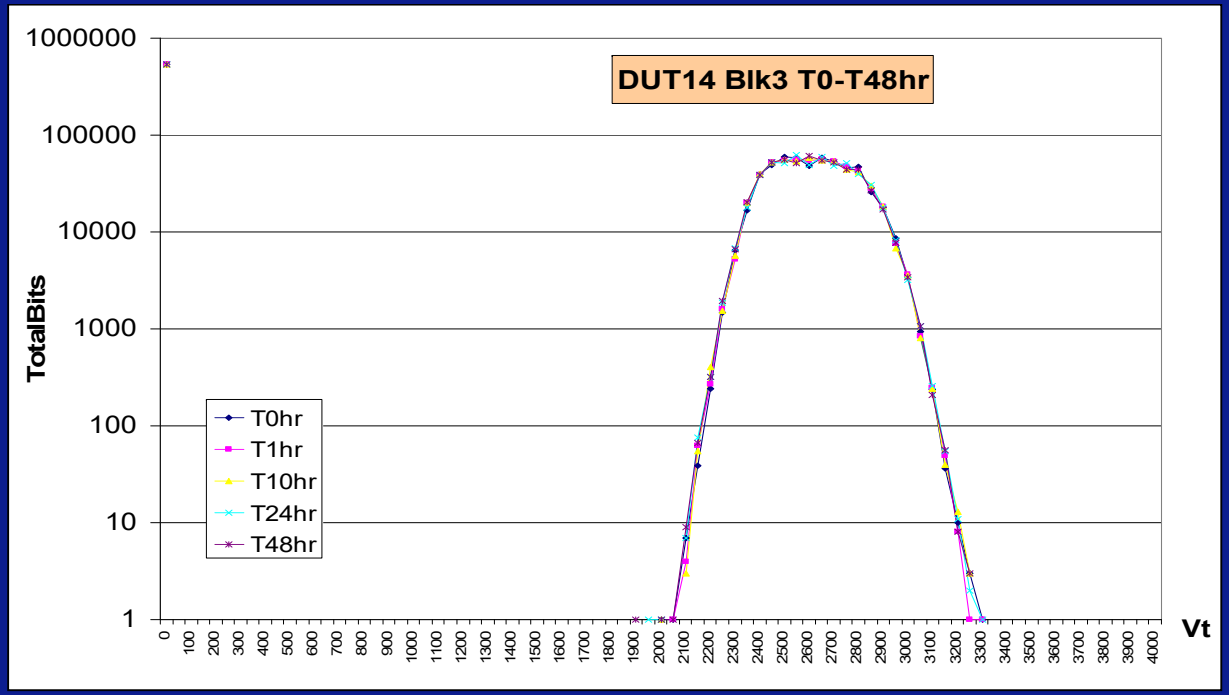
RETE Qual Monitoring of Flash Memory Cell Vt Drift



Full HTOL qualification with continuous uninterrupted monitoring and no need of retest on ATE.

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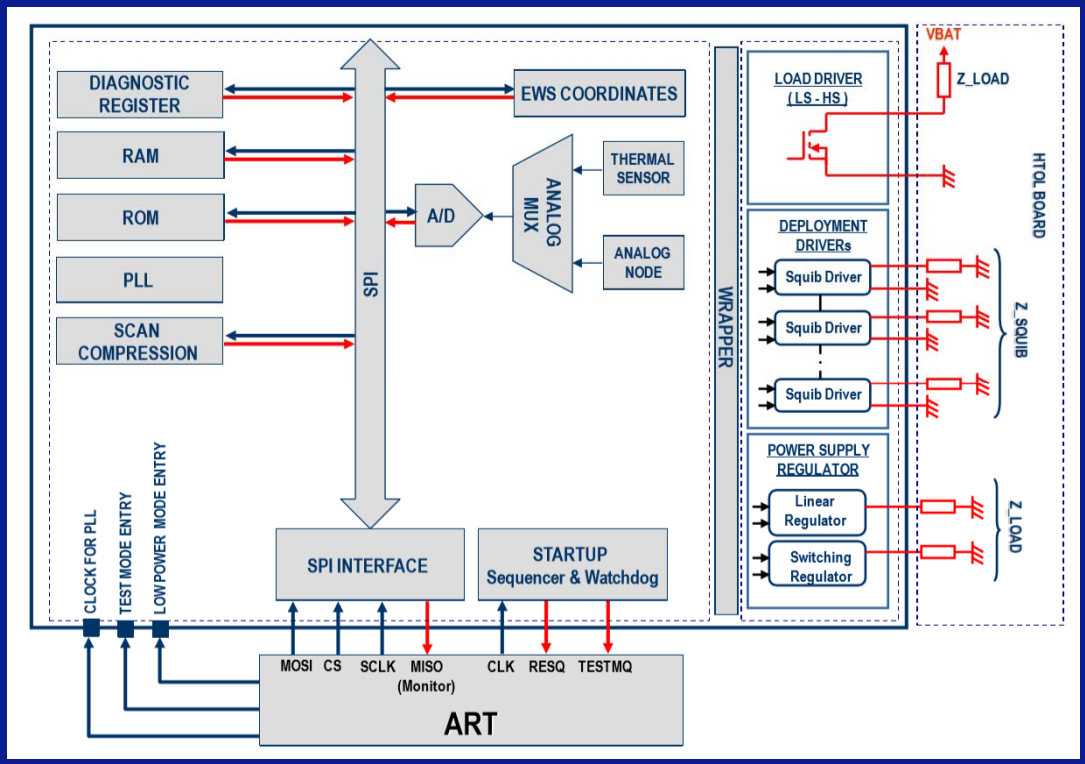
RETE Analog DfT on Smart-Power



Use of Internal A/D to measure Load currents

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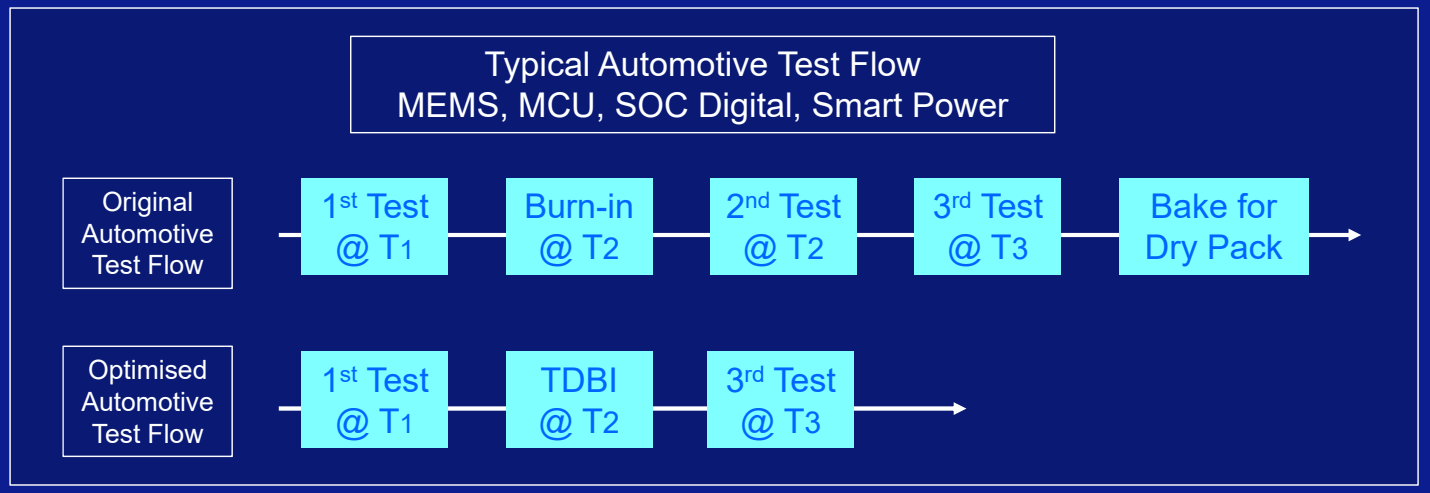
RETE Enables Final Test Flow Reduction (1/2)



Cost Reduction and Simplification of Production Test flow.
From Burn-in to TDBI (Testing During Burn-in) and Total Test

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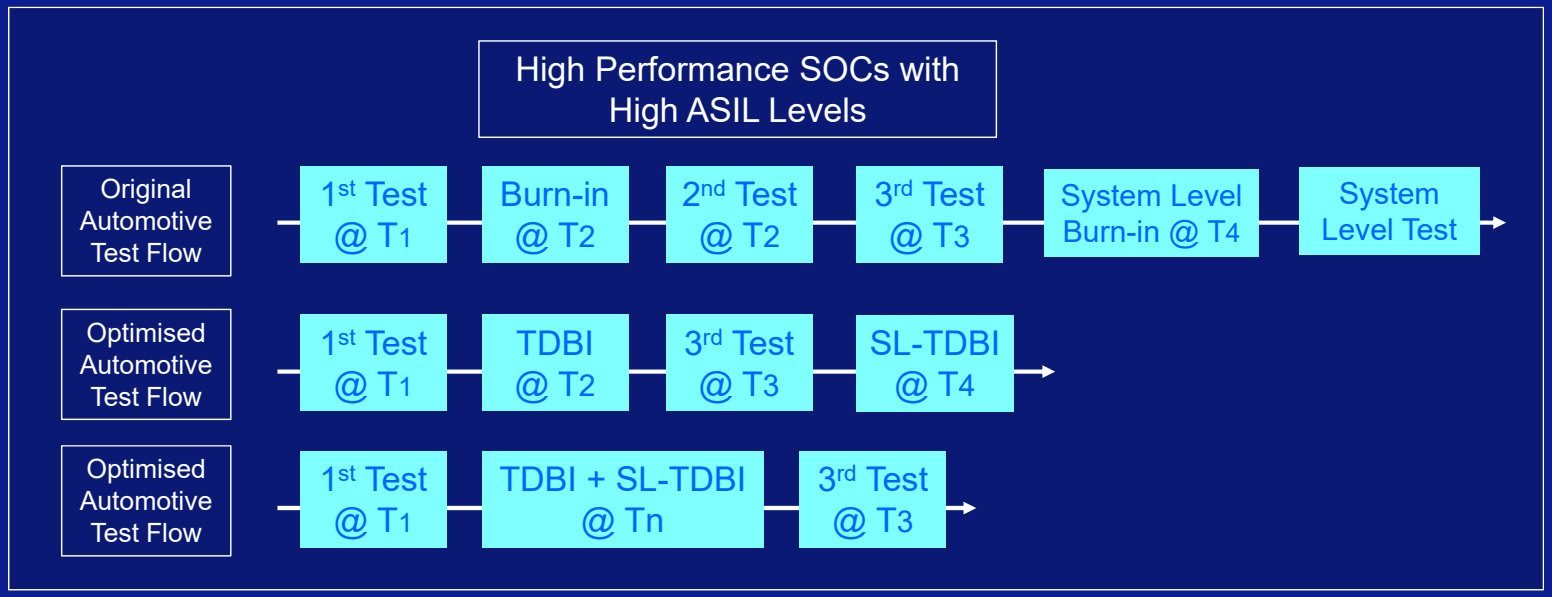
RETE Enables Final Test Flow Reduction (2/2)



Cost Reduction and Simplification of Production Test flow.
From Burn-in to TDBI to SL-TDBI (System Level TDBI)

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7 Steps to Zero Defects

1. Design with DfRT approach
2. Use of algorithms which take advantage of DfT
3. Use of full stress matrix to screen TfR
4. In-situ Stress & Test to screen intermittent failures
5. Increase Test coverage with DfT in chamber vs ATE
6. Use Learn-from-Fail (LfF) data to improve processes
7. Adaptive LfF for more optimised flows

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