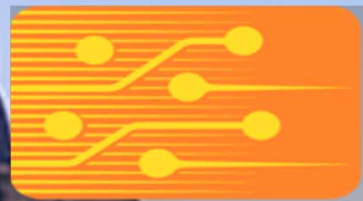

# TestConX 中国 China

October 29, 2019

InterContinental Shanghai Pudong Hotel

# Archive

# Review today's test strategy on ATE and SLT

**Liang "Neil" Zhang**
**Teradyne**

Shanghai ▪ October 29, 2019

## Content

- Device test trend and challenge
- High throughput SLT test
- Speed up IP debug
- Case study on test strategy definition
- Conclusion

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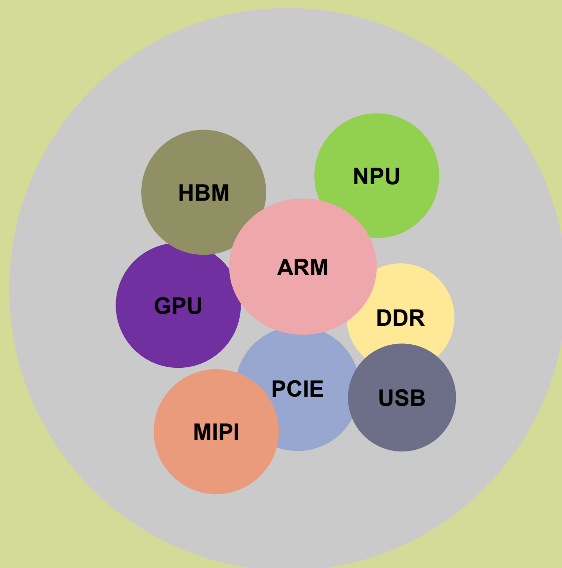
## Device is now much more complex




- **More IP integrated (ARM, NPU, GPU, Sensor ..)**
- **Advance process introduced (10nm -> 7nm -> 7+nm -> 5nm ..)**
- **Highly integration in package ( 2.5D -> 3D package)**
- **High quality requirement and short time to market**

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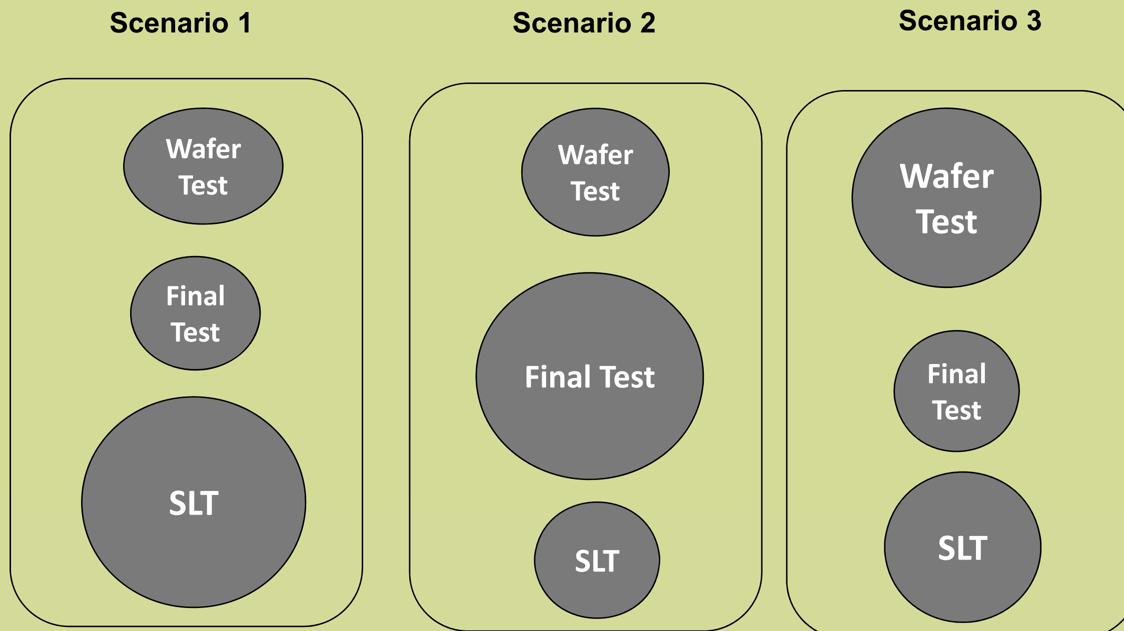
Review Test Strategy for the Device Challenge
Scenario 1
Wafer Test
Final Test
SLT
Scenario 2
Wafer Test
Final Test
SLT
Scenario 3
Wafer Test
Final Test
SLT
More CP test needed due to yield concern of advance process
More SLT introduced due to complex IP integration and un-know failure
Device bring up time accelerated from months to weeks
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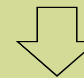
# High Throughput SLT Solution is Required

**Teradyne SLT Solution - Titan**

SLT normally take much longer test time than ATE (10 times more!)
Traditional SLT handler is limited to *12* or *16* sites



- Supports up to **320** sites per system
- Supports PoP, PGA, BGA, LGA, etc.
- Test sites are fully asynchronous (load and test)
- System can be serviced while running for ~100% OEE

High Throughout
Cost Effective

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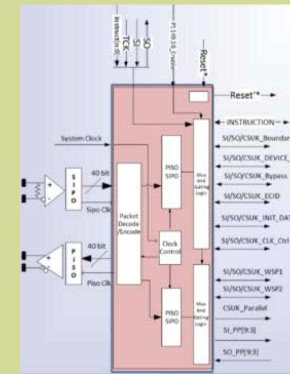
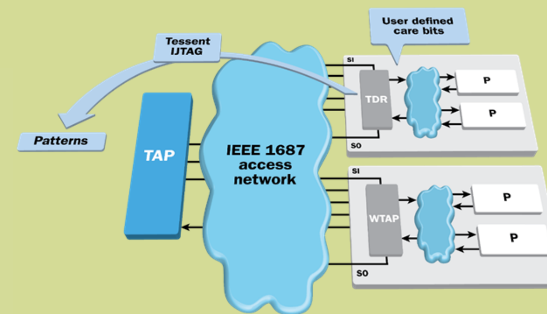
## Industry Standard Trend

- ❑ **IEEE 1149.10**
  - – Scan test over high speed Interface (like USB)
- ❑ **IEEE1687/1500**
  - – Allows IP vendors to offer standardized access to Silicon IP for test
- ❑ **Accellera "Portable Stimulus Group" (IEEE 1800.2-2017)**
  - – system-level design, modeling, and verification standards



Source: IEEE High Speed JTAG P1149.10 Working Group

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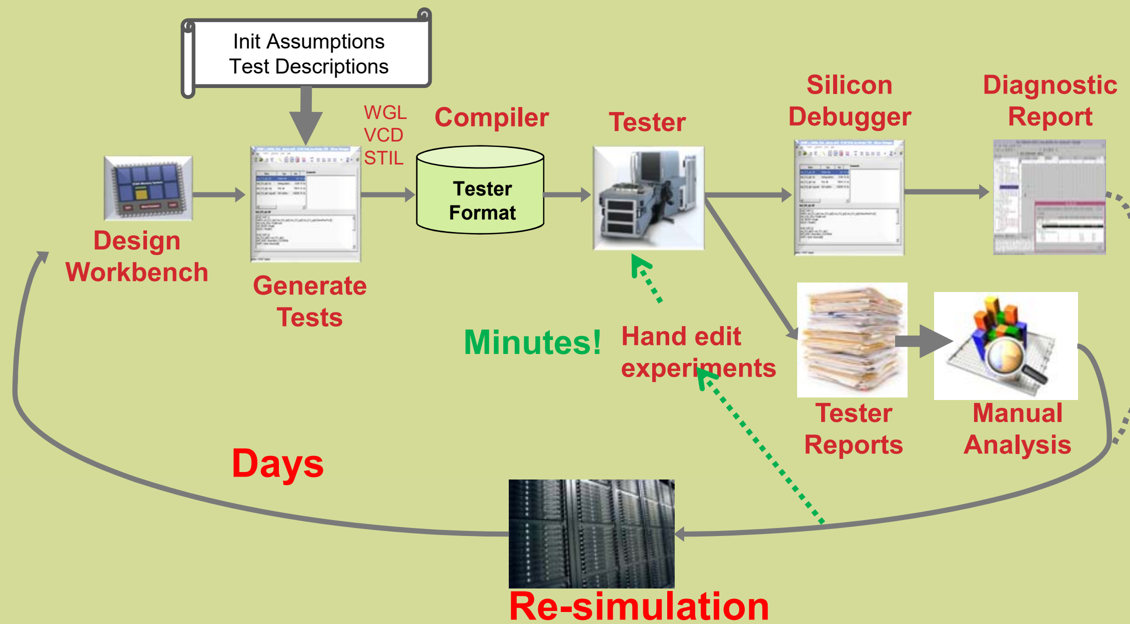
Device Bring up Take More Time
Init Assumptions
Test Descriptions
WGL
VCD
STIL
Compiler
Tester
Silicon
Debugger
Diagnostic
Report
Tester
Format
Design
Workbench
Generate
Tests
Minutes!
Hand edit
experiments
Tester
Reports
Manual
Analysis
Days
Re-simulation
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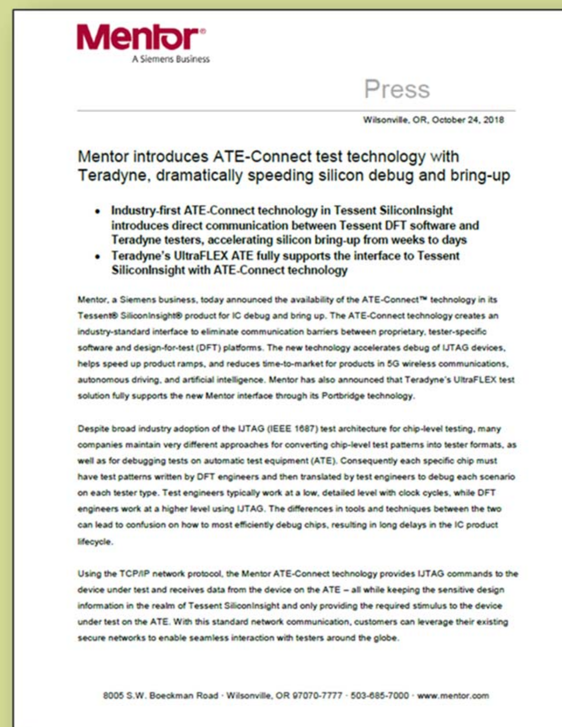
## Teradyne/Mentor Announcement at International Test Conference

- Mentor introduces ATE-Connect™ test technology with Teradyne, dramatically speeding silicon debug and bring-up



Mentor
A Siemens Business

Press

Wilsonville, OR, October 24, 2018

Mentor introduces ATE-Connect test technology with Teradyne, dramatically speeding silicon debug and bring-up

- **Industry-first ATE-Connect technology in Tessent SiliconInsight introduces direct communication between Tessent DFT software and Teradyne testers, accelerating silicon bring-up from weeks to days**
- **Teradyne's UltraFLEX ATE fully supports the interface to Tessent SiliconInsight with ATE-Connect technology**

Mentor, a Siemens business, today announced the availability of the ATE-Connect™ technology in its Tessent® SiliconInsight® product for IC debug and bring up. The ATE-Connect technology creates an industry-standard interface to eliminate communication barriers between proprietary, tester-specific software and design-for-test (DFT) platforms. The new technology accelerates debug of IJTAG devices, helps speed up product ramps, and reduces time-to-market for products in 5G wireless communications, autonomous driving, and artificial intelligence. Mentor has also announced that Teradyne's UltraFLEX test solution fully supports the new Mentor interface through its Portbridge technology.

Despite broad industry adoption of the IJTAG (IEEE 1687) test architecture for chip-level testing, many companies maintain very different approaches for converting chip-level test patterns into tester formats, as well as for debugging tests on automatic test equipment (ATE). Consequently each specific chip must have test patterns written by DFT engineers and then translated by test engineers to debug each scenario on each tester type. Test engineers typically work at a low, detailed level with clock cycles, while DFT engineers work at a higher level using IJTAG. The differences in tools and techniques between the two can lead to confusion on how to most efficiently debug chips, resulting in long delays in the IC product lifecycle.

Using the TCP/IP network protocol, the Mentor ATE-Connect technology provides IJTAG commands to the device under test and receives data from the device on the ATE – all while keeping the sensitive design information in the realm of Tessent SiliconInsight and only providing the required stimulus to the device under test on the ATE. With this standard network communication, customers can leverage their existing secure networks to enable seamless interaction with testers around the globe.

8005 S.W. Boeckman Road · Wilsonville, OR 97070-7777 · 503-685-7000 · www.mentor.com

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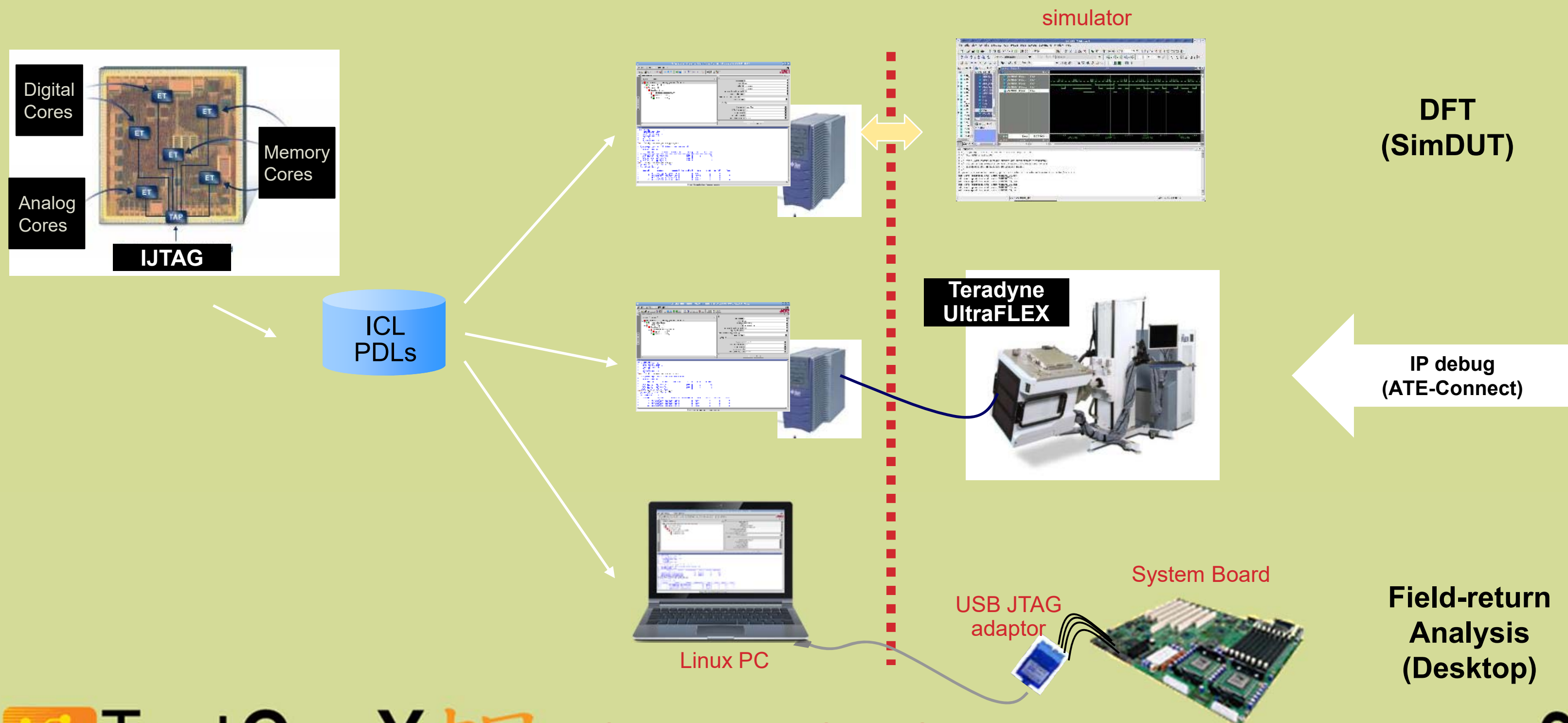
Tessent SiliconInsight: Consistent Debug Environment
Digital Cores
Memory Cores
Analog Cores
IJTAG
ICL PDLs
simulator
DFT (SimDUT)
Teradyne UltraFLEX
IP debug (ATE-Connect)
System Board
USB JTAG adaptor
Linux PC
Field-return Analysis (Desktop)
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SiliconInsightSetupSpecification
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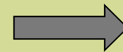
## Debug Device in Simple Way

**Pattern Based**

- Take more time to generate pattern
- Need DFT/TE close work

**Protocol Based**

- Debug in straight forward way
- DFT and TE can work independently



```
# The read_adc procedure requires a channel # (from 0 to 7).
#   The ADC then converts voltage on this channel to a 12-bit unsigned binary
value.
#   This value is then compared against an all-zero value.

iProc read_adc { ch wait } {
    iNote "Starting measurements on channel $ch"
    iWrite measure_ch $ch
    iWrite measure_start Convert
    iApply

    iNote "Waiting for $wait TCK cycles before moving on..."
    iRunLoop $wait -tck
iWrite measure_start Idle
    iApply

    iNote "Checking that measure_done = 1 and extracting results"
    iRead measure_done Done
    iRead measure_dataread 0b000000000000
    iApply
    iNote "Done."
}
```

Read routine

Wait time + de-assert measurement start

Measurement shift-out

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# Case Study in Emerging Markets

**AI**

- ❑ There are two pieces to AI: Infrastructure and Edge
- ❑ Infrastructure will always use SLT for the usual reasons
- ❑ What About Edge devices?
- ❑ Now it's about volume, cost and reliability
- ❑ More like applications processors we do today that have a wide range of test strategies

**ADAS**

- ❑ Automotive IC manufacturers seem to know how to make complex devices without using SLT
- ❑ What about Level 3 / 4 ADAS?
- ❑ What about the higher volume devices (e.g. MCUs)?

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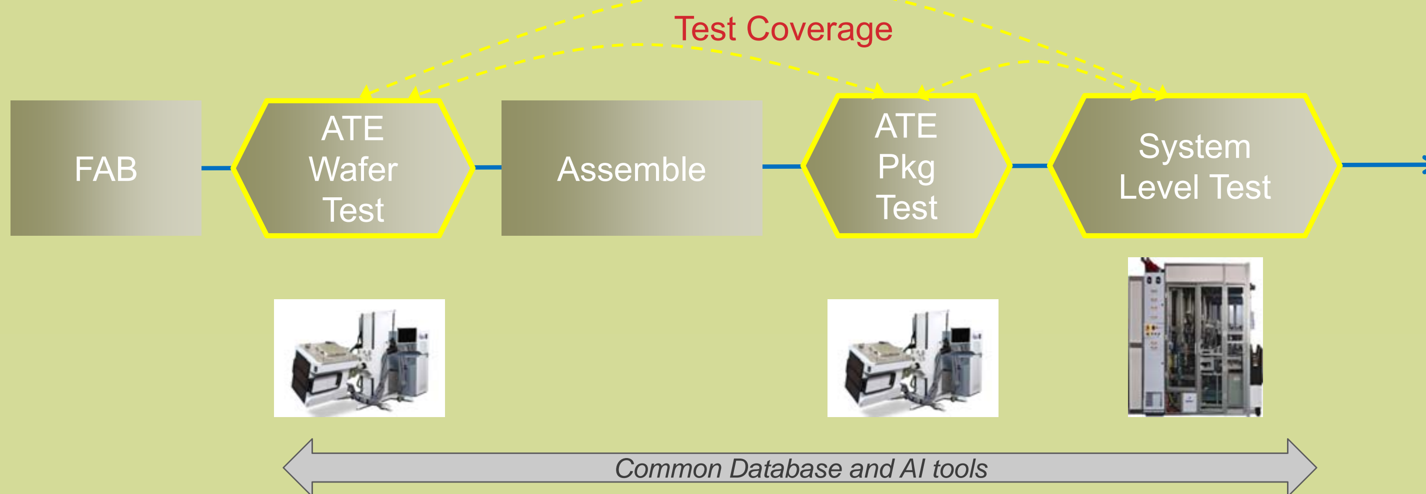
# Big Data Help on Test Strategy

- Balance Test Coverage Between Test Insertions for the best mix of cost, quality and yield
- Use Common Data Analysis and AI tools across the entire flow

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## Bridge the ATE and SLT

- **Unify programming environments for ATE and functional/SLT**
  – efficient test deployment, code portability, better failure analysis
- **Balance test coverage and test cost based on big data**
  – Test strategy for each insertion would be different for different application
- **New AI techniques will help to improve coverage and identify right strategy**
  – Outlier detection, etc.

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