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Beyond Sort, Burn-In, and Class Testing: Post-Silicon Validation Hardware Strategy

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1

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Agenda

- Goals and Objectives
- Introduction
- Hardware Solutions
- Case Studies
  - Power Measurement and Challenges of >340 A
  - Socketing Large BGA Packages
  - Scaling Thermal Tools for Products with >500 W and -40 C Temperature Requirement
- Closing Summary

Goal

- Introductory tutorial covering systems, sockets, and thermal tools used in post-silicon Functional Validation along with the challenges and solutions to satisfy Validation requirements.
- Attendees should be familiar with the silicon product manufacturing test flow and have a basic understanding of post-silicon functional validation.

Objectives

This tutorial will provide attendees with a basic understanding of:

- The different types of post-silicon validation
- The goals of Functional Validation and types of HW used
- How validation differs from manufacturing test
- Types of sockets and thermal tools used by Functional Validation
- Challenges with managing Functional Validation scope and optimizing hardware strategies
- Challenges with development of high-power measuring solutions, socketing of large BGAs, and Thermal tools for high power/low temperature components

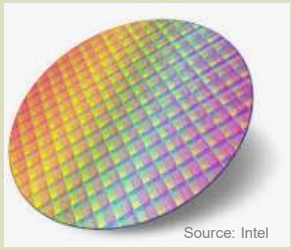
Introduction

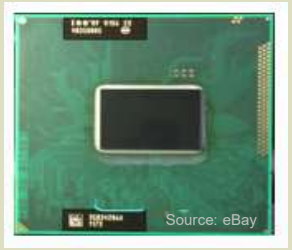
- Manufacturing Test
- What is Validation
- Validation vs Burn-in
- Types of Post-silicon Hardware
- Post-silicon Validation Sockets
- Post-silicon Validation Thermal Test Systems
- Types of Post-silicon Validation

Introduction

MANUFACTURING TEST FLOW AND POST-SILICON VALIDATION

Simplified Manufacturing Test Flow


Source: Intel


Source: eBay

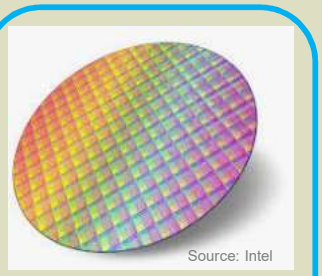

Source: AEHR Test Systems


Source: AEHR Test Systems

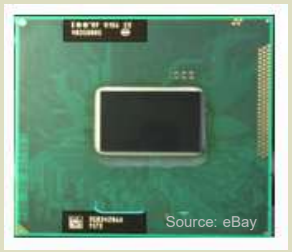

Source: Intel

Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Simplified Manufacturing Test Flow



Sort Testing



Package Parts

Burn-In Testing

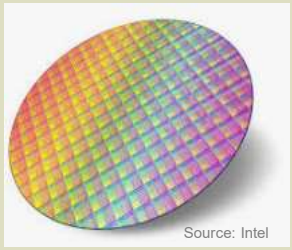
Class Test

Ready to Ship

Sort Testing

Wafer or singulated die level testing to select good die that will move on packaging

Simplified Manufacturing Test Flow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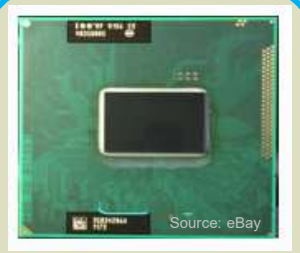

Source: eBay


Source: AEHR Test Systems


Source: AEHR Test Systems

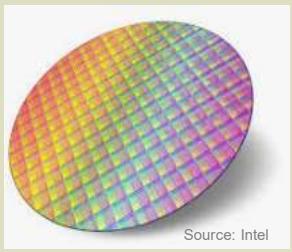

Source: Intel

Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Package Parts

Good die from Sort are attached to substrates along with other components and may include a heat spreader (not shown); Testing may or may not be done prior to Burn-in

Simplified Manufacturing Test Flow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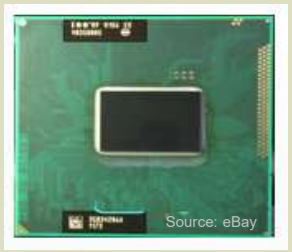
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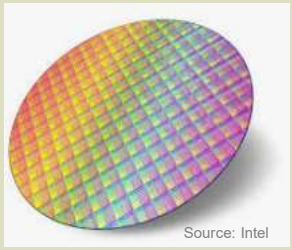
Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Package Parts

Packaged parts tested at elevated voltage and temperature to eliminate defective components

Simplified Manufacturing Test Flow



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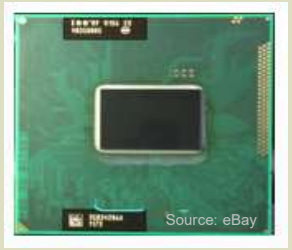


Package Parts

Burn-In Testing

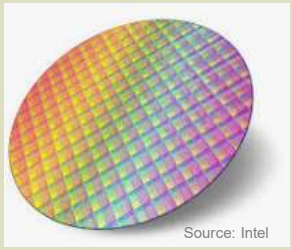
Class Test

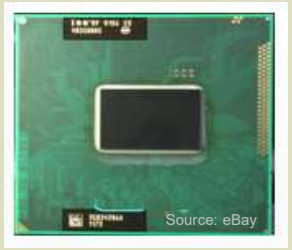
Ready to Ship

Class Test

Also called final test, parts are tested and classified according to performance and capability across temperature and voltage

Simplified Manufacturing Test Flow



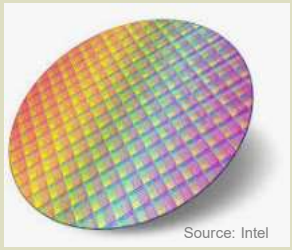


Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Product Ready

After Class Test, products are packaged and ready to ship

Simplified Manufacturing Test Flow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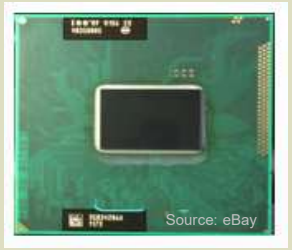
Source: eBay


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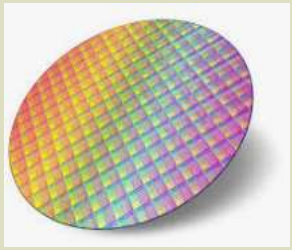
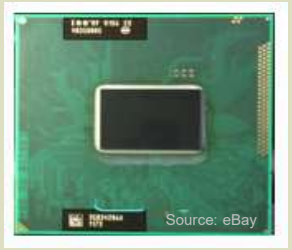
Source: Intel

Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Applies to mature products, ignores initial component post-silicon validation

Simplified Manufacturing Test Flow





Sort Testing → Package Parts → Burn-In Testing → Class Test → Ready to Ship

Post-Silicon Validation

Reality: Post-Silicon Validation is *not* Manufacturing Test and happens in parallel with the Test Flow ending when product quality launch criteria has been met

Introduction

POST-SILICON VALIDATION OBJECTIVE

Validation Definition

Methodology to confirm that a component's design exactly matches its functional specifications

Validation Objective

- Validation assures components meet:
  - Applicable end-user use case requirements
  - Architectural design specification
  - Industry specifications (Example: USB, PCIe)
  - Internal specifications for proprietary interfaces

Validation Classes

Pre-silicon
RTL

Validation Classes

Pre-silicon
RTL

Post-silicon
Component

Validation Classes

Today's tutorials will focus on the platform hardware used in Post-silicon validation

Source: Intel

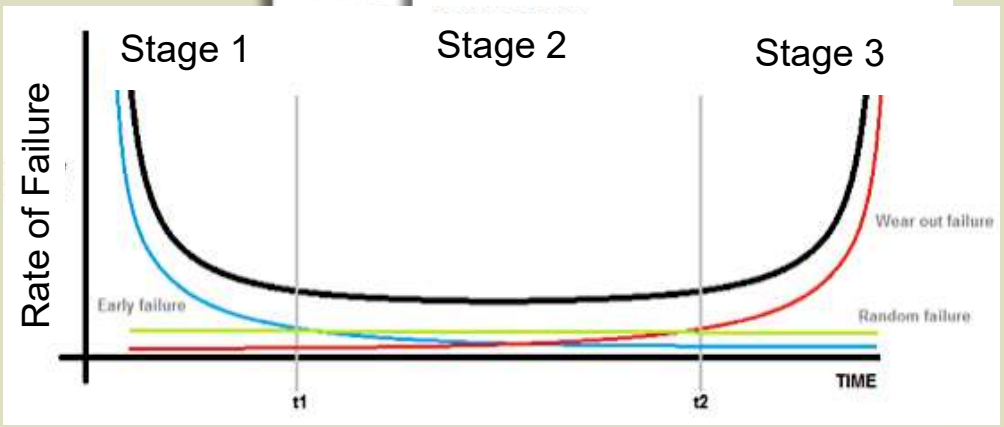
Post-silicon Component

Validation Goals vs Burn-in

- Validation:
  - Show that CPU's design exactly matches its *functional* specifications

Validation Goals vs Burn-in

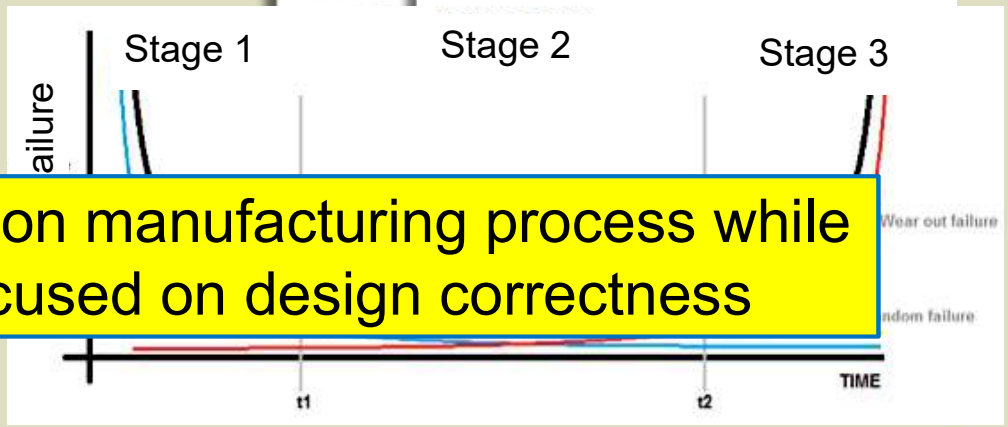
- Validation:
  - Show that CPU's design exactly matches its *functional* specifications
- Burn-in:
  - Detect early failures
  - Increase reliability
  - Lower Defective Parts Per Million in Stage 1: Infant Mortality



Source: EDN Network, Burn-in 101

Validation Goals vs Burn-in

- Validation:
  - Show that CPU's design exactly matches its *functional* specifications
- Burn-in:
  - Detect early failures
  - In
  - L
    M
    Mortality



Source: EDN Network, Burn-in 101

Burn-in is focused on manufacturing process while validation is focused on design correctness

Introduction

TYPES OF POST-SILICON HARDWARE

Section Agenda

- Definitions
- General anatomy of:
  - Reference Platform
  - Synthetic Platform
  - I/O Characterization Platform

Definition: Reference Platform

- Reference Platform
  - Intel developed
  - Representative of a general OEM/ODM system
  - Fully engineered starting point for leveraged designs
  - Includes minimal non-product system features to enable validation

Definition: Synthetic Platform

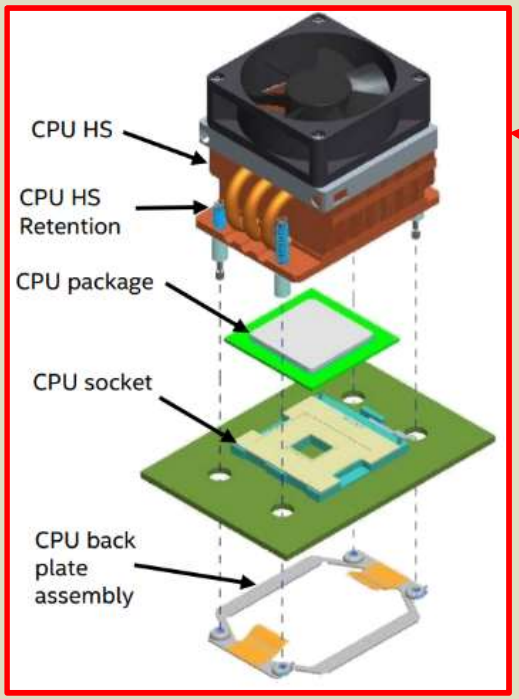
- Synthetic Platform
  - Imitates a Reference Platform in some ways
    - Can boot and run operating system (OS)
    - Shares majority of firmware, but is different (FW)
  - Non-Reference Platform
    - Form factor
    - Power delivery
    - High Speed Interface Topologies

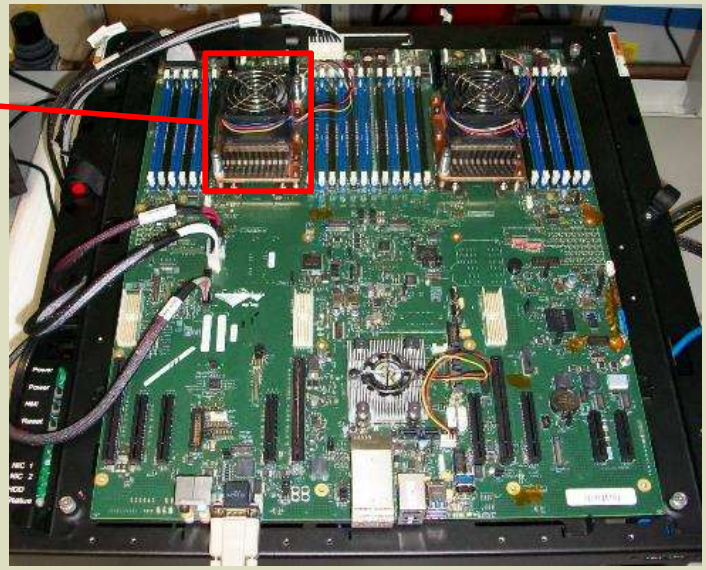
Reference Platform

Source: Intel

2 Socket Reference Platform

Exploded View Heat Sink and Socket Assembly

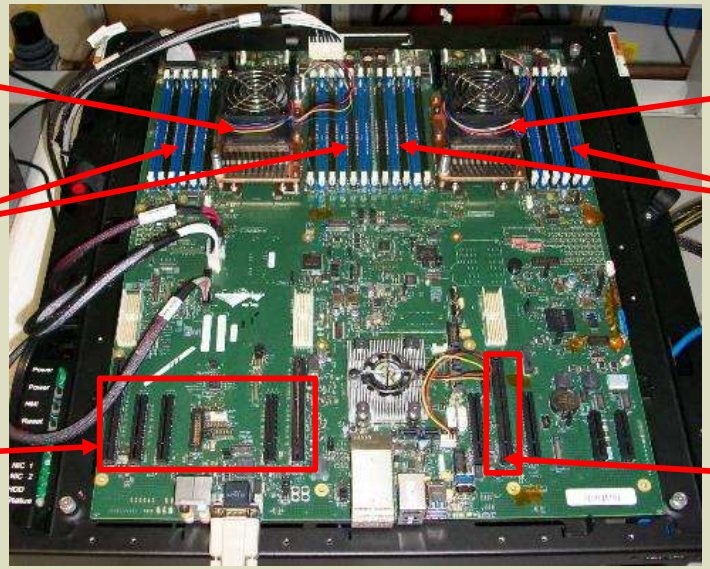




Source: Intel

2 Socket Reference Platform

Reference Platform Key Components

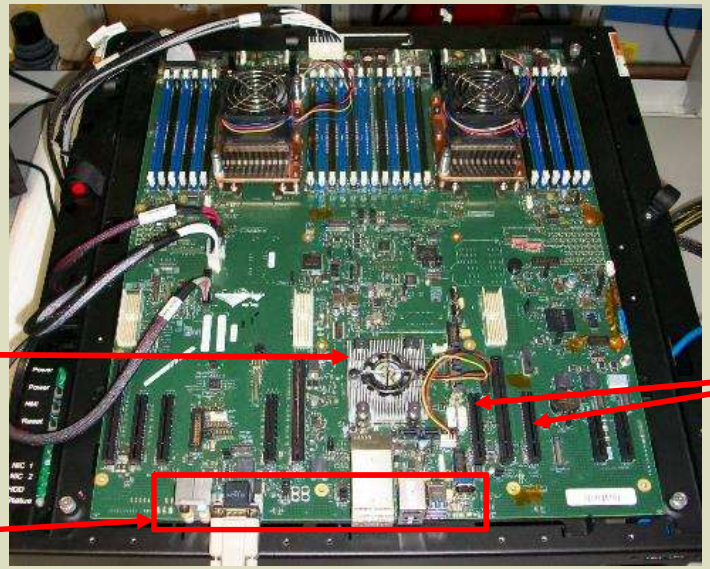


Source: Intel

2 Socket Reference Platform

Validation workhorse supporting the majority of the validation effort for Intel® Xeon® Scalable Processors

Reference Platform Key Components



Source: Intel

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Validation workhorse supporting the majority of the validation effort for Intel Xeon Scalable Processors

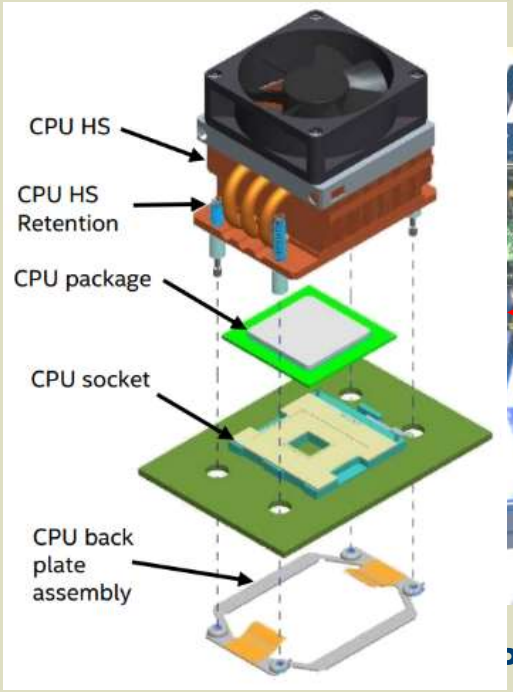
Synthetic Platform

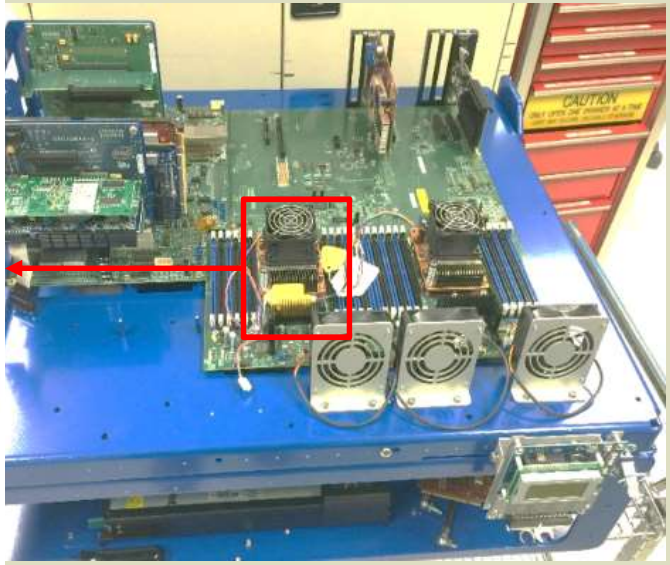
Source: Intel

2 Socket Platform Control Hub (PCH) Test Platform

Additional test coverage of PCH specific features such as High Speed I/O configurations and power consumption measurements

Synthetic Platform



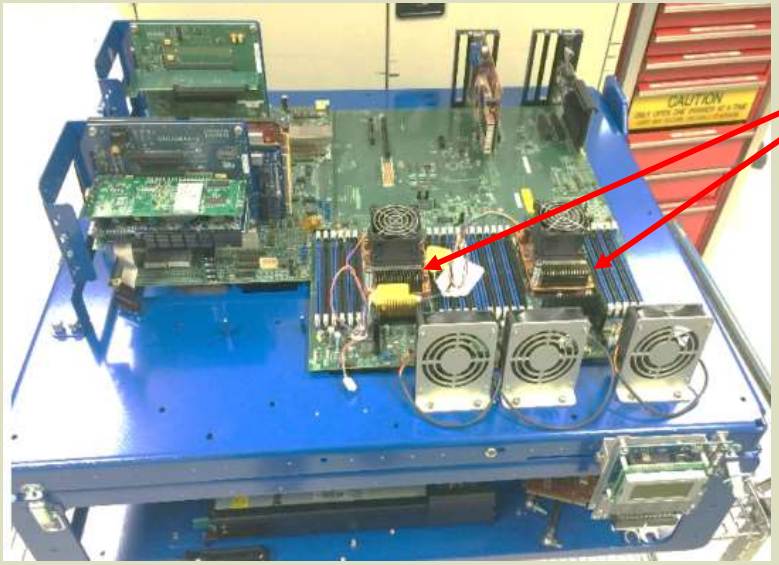


Source: Intel

Platform Control Hub (PCH) Test Platform

Additional test coverage of PCH specific features such as High Speed I/O configurations and power consumption measurements

Synthetic Platform Key Components



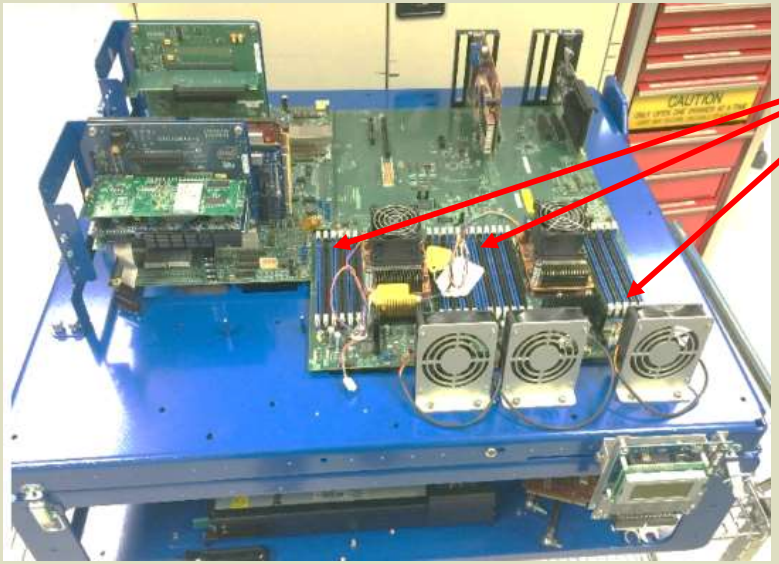
CPU Sockets (Shown with CPUs and Heat Sinks Installed)

Source: Intel

2 Socket Platform Control Hub (PCH) Test Platform

Additional test coverage of PCH specific features such as High Speed I/O configurations and power consumption measurements

Synthetic Platform Key Components



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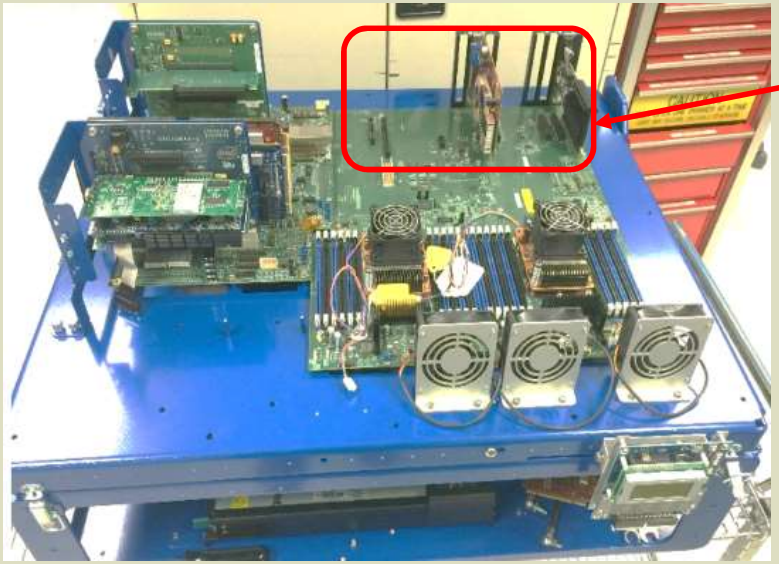

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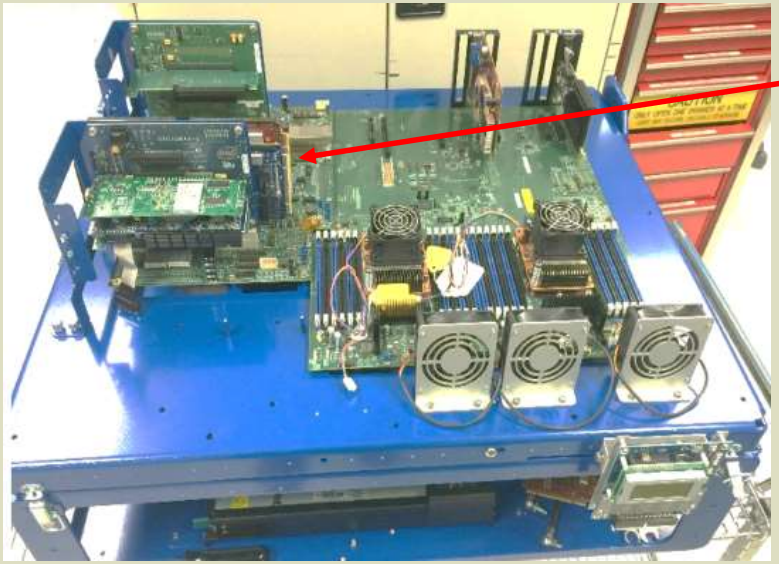


Source: Intel

2 Socket Platform Control Hub (PCH) Test Platform

Additional test coverage of PCH specific features such as High Speed I/O configurations and power consumption measurements

Synthetic Platform Key Components

PCH
PCIe Bifurcation
Boards

PCH I/O not shown

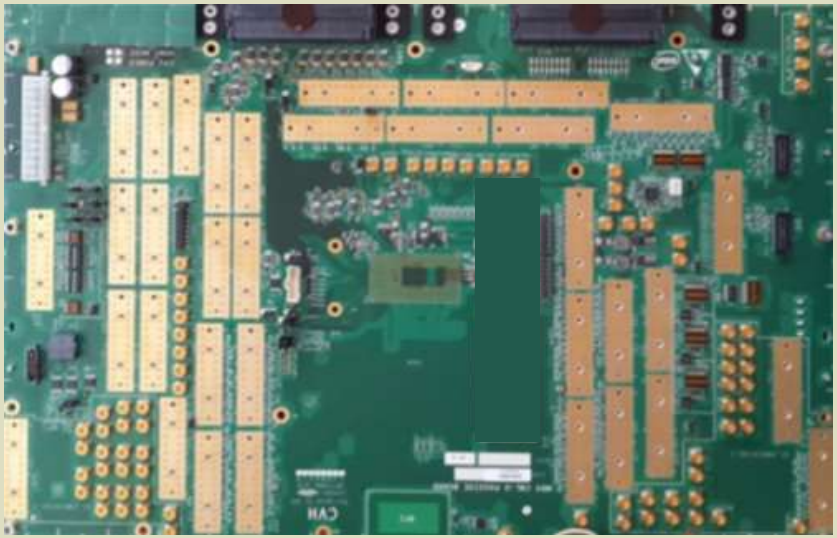
Source: Intel

2 Socket Platform Control Hub (PCH) Test Platform

Additional test coverage of PCH specific features such as High Speed I/O configurations and power consumption measurements

I/O Characterization Board

Robson Technologies, Inc.

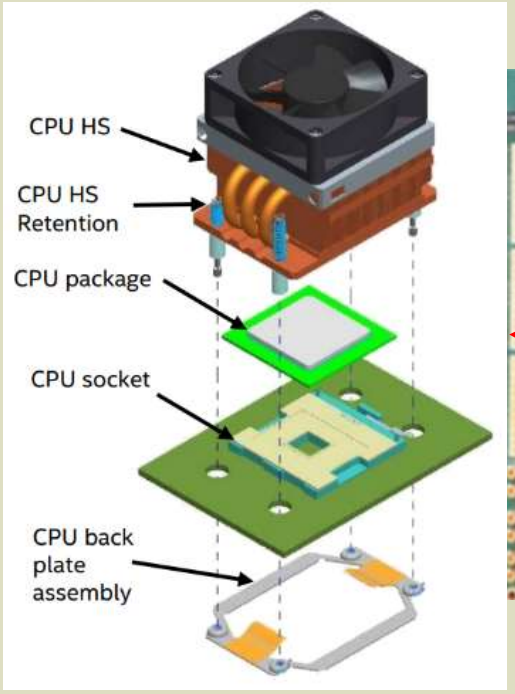


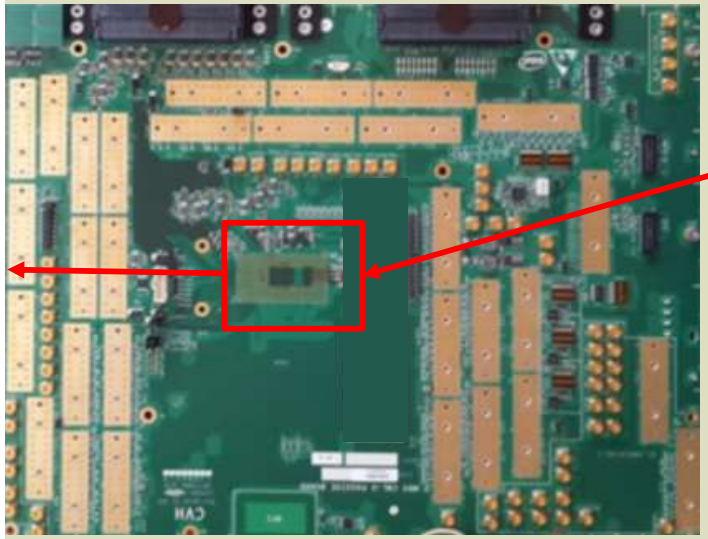
Source: Intel

I/O Characterization Board

Enables observation and measurement of a component's I/O

I/O Characterization Board Key Components





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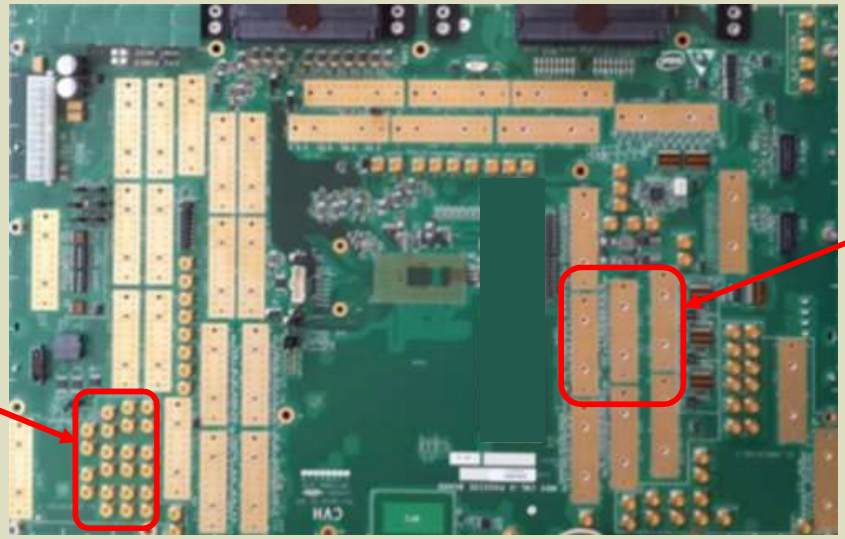


Source: Intel

I/O Characterization Board

Enables observation and measurement of a component's I/O

Introduction

POST-SILICON VALIDATION SOCKETS

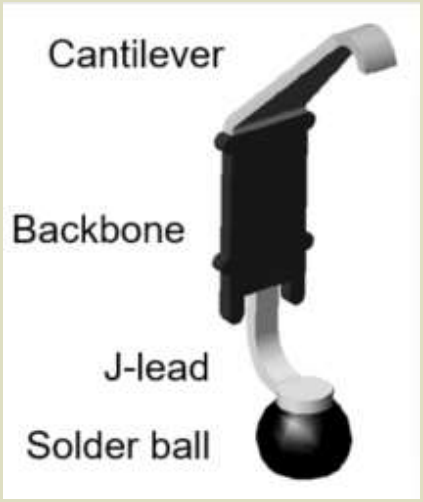
Agenda

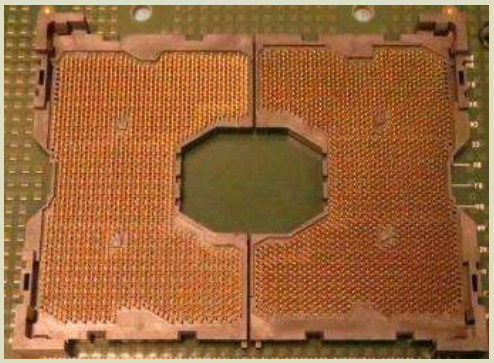
- Socket Introduction
- Trends
- Stamped and Formed Pin Socket
- Spring Pin Socket
- Elastomer Socket
- Typical Compression Heights
- Surface Mount vs Socketing Trade-offs

Socket Introduction

- Common types of sockets in post-silicon Validation
  - Stamped and formed pin sockets, elastomer sockets, spring pin sockets
- Substrate
  - Stamped and formed pin socket, BGA
- Environment
  - OEM products, HVM Testing (Burn-in and Class), Post-Silicon Validation Testing
- Application
  - CPU, GPU, Chipset, Memory, ASIC, Modem, FPGA, Interposer

Stamped and Formed Pin Socket (Used in both Production Boards and Validation Test Boards)

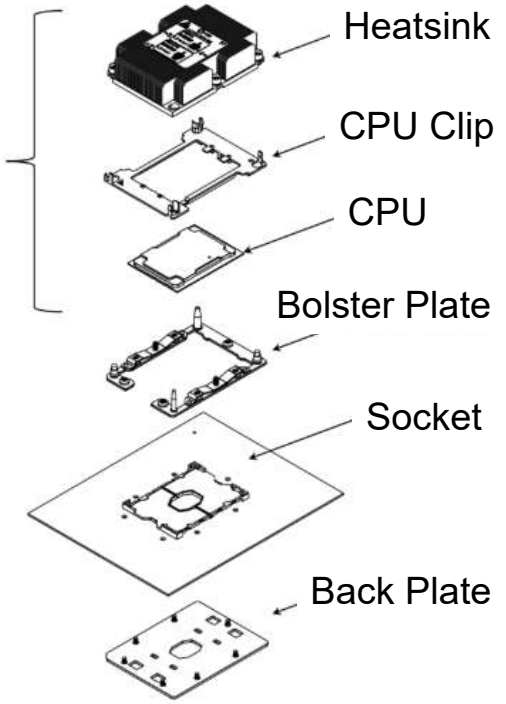




Source: Intel

Socket is surface mounted (soldered) to board

PHM (Processor Heatsink Module) Subassembly)

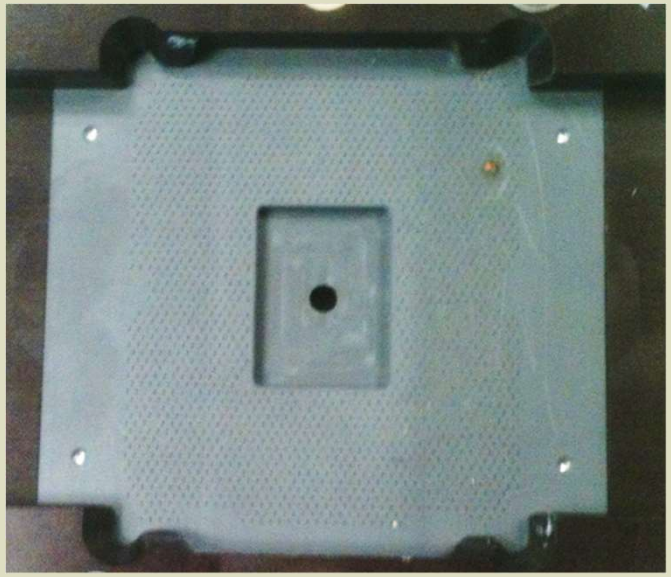


Source: Intel

Sources:

- intel.com
- M Imaninejad et al, 54th IEEE Holm Conference on Electrical Contacts, 2008

Spring Pin Socket

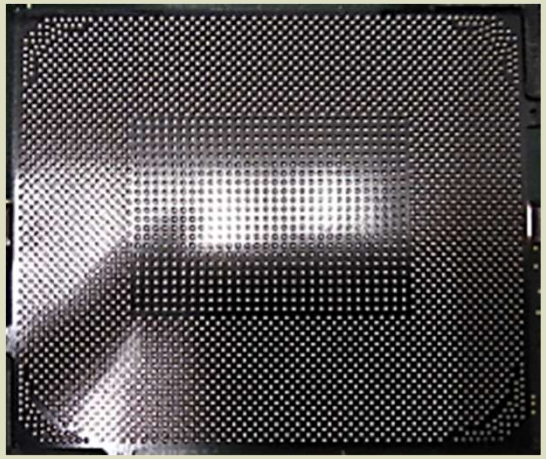


Source: Intel

Socket is not soldered to board but assembled by alignment pins

- Very high reliability (up to 500 K cycles insertion / extraction)
- Primarily used in High Volume Manufacturing Testing
- Relatively high stroke and working range

Elastomer Socket

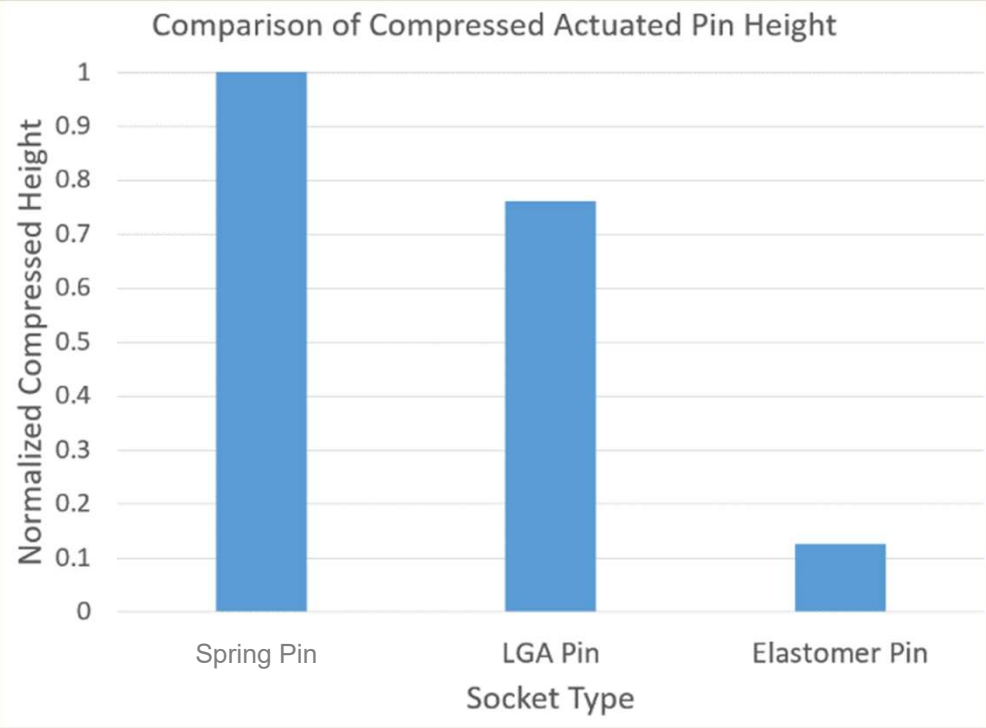


Source: Intel

Socket is not soldered to board but assembled by alignment pins

- Pins consist of metal particles in an elastomer matrix
- Relatively low cost
- Extremely low height
- Can be customized to mixed pitch
- Primarily used in post-silicon Validation

Comparison of Typical Socket Pin Compressed Height in Post-Silicon Validation



- Pin height has significant influence on electrical performance for high speed applications
  - Insertion Loss
  - Pin to Pin Cross Talk
- Pin stroke (travel) has significant influence on its ***capacity to tolerate large package warpage***
  - Low level contact resistance

Note: Elastomer pin height is close to the size of solder ball

Tradeoff: Surface Mounted vs Socketed BGA Packages for Post-Silicon Validation

Advantage (Green) / Disadvantage (Red)	Surface Mounted BGA	Socketed BGA
Swap out defective silicon	**No**	**Yes**
Swap out different steppings of silicon	**No**	**Yes**
Save costs and lead time of expensive test boards	**No**	**Yes**
Unlock silicon from the board (*important when early silicon steppings have low yield*)	**No**	**Yes**
Extra flexibility in configuration capability when using different interposers between silicon and board	**No**	**Yes**
Large socket retention forces increase with pin count	**No**	**Yes**
Large socket retention forces increase with large package warpage	**No**	**Yes**
Extra collateral needed to design socket retention mechanisms	**No**	**Yes**
High electric current capability	**Lower risk**	**Higher risk**

Introduction

POST-SILICON VALIDATION THERMAL TEST SYSTEMS

Agenda

- What is a Thermal Test System
- Thermal Test System Applications
- Examples of Thermal Test Systems

What is a Thermal Test System?

A thermal test system provides temperature margining capabilities over a temperature range to the silicon under test.

- Used for manufacturing test to capture logic, silicon, electrical defects to reduce DPM while maximizing yield
- Widely used on post silicon validation test to assure silicon functionality in its anticipated service life conditions and accelerate bugs detection in the labs ahead of silicon shipment.

Thermal Test System Applications

Thermal test system or Thermal Tool (TT) play a major role in manufacturing test and post silicon platform debug and validation

- Provides temperature control for class, burn in, Product Platform Verification (PPV) and Quality Assurance (QA) test
- Enables various post silicon validation: System Validation (SV), Electrical Validation (EV), Quality & Reliability (QnR) etc.

Examples of Thermal Test Systems

Manufacturing Test

Burn-In

Product Platform Verification

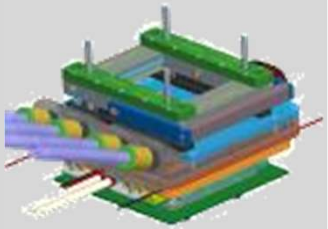
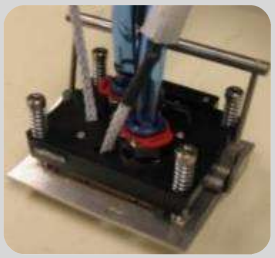
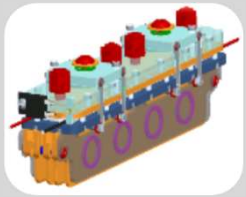
Class

Post Silicon Validation Test

Automation

Bench-top

Post Silicon Validation Thermal Hardware Scope

Power	High Power		Low power	
Thermal Head and retention				
				

Introduction

POST-SILICON VALIDATION

Types of Post-Silicon Validation

- Functional
- Electrical
- Power and Performance
- Compatibility

Functional Validation

- Objectives
  - Verify end-user Use Cases and Requirements
  - Correctness to Engineering Design Specification
  - Test to Industry Specifications

Functional Validation

- Objectives
  - Verify end-user Use Cases and Requirements
  - Correctness to Engineering Design Specification
  - Test to Industry Specifications

Goal: Ensure products meet functional design specifications

Functional Validation Hardware

Source: Intel

Reference Platform (RP)

- Runs the majority of test content:
  Use Cases; instruction set; stress testing; concurrency; some memory types and configurations
- Used for the majority of debug
- Limited memory and I/O capability

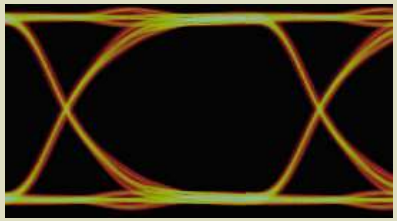
Source: Intel

Synthetic Platforms

- Additional memory, PCH, and CPU I/O configurations not covered by the RP
- Flexible PCH HSIO configurability
- Small percentage of platforms used

Electrical Validation

- Objectives
  - Characterization of I/O buffer design to specification
  - Design specifications across temperature and voltage
  - Industry specifications
  - Buffer tuning capabilities
  - System signal quality correlation to simulations
  - Measurement of interface timing and voltage margins across all HVM variables and workloads



Source: Intel

Electrical Validation Hardware

Source: Intel

I/O Characterization Board

- I/O response across temperature and voltage
- Buffer tuning functionality
- Jitter, PLL Delays
- TX eye diagrams
- Limited to TX I/O

Source: Intel

Reference Platform (RP)

- Correlation of system based measurements to simulated results
- Jitter, cross talk
- Receiver detection, Compensation, De-emphasis, RX Jitter tolerance, Rcomp/Icomp, TX eye diagrams
- Covers Rx and TX I/O

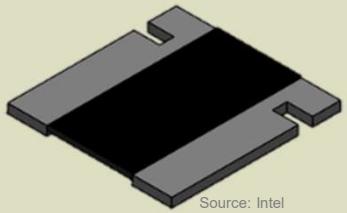
Power and Performance

- Objectives
  - Component characterization
  - Tuning of component operating parameters (voltage and frequency) to achieve performance per watt design targets
    - Idle power
    - Tune Turbo algorithm
    - Energy Star compliance

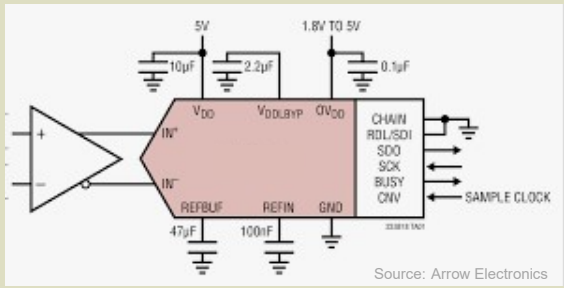
Power and Performance Validation Hardware


Source: Intel

Synthetic Platforms


Source: Intel

4-pin Sense Resistor



Differential A2D

- All component voltage rails instrumented with 4-pin current sense resistors wired out to Analog to Digital (A2D) data acquisition equipment (DAQ)
- Special power plane design to split rails as needed for sense resistor insertion

More detail on this topic later in the tutorial…

Compatibility Validation

- Objectives
  - System level testing of components
  - Complete SW stack: OS, drivers, applications, firmware (FW)
  - Memory management
  - Strategic I/O configurations
  - Platform power management

Compatibility Validation Hardware

- Off the shelf OEM and ODM platforms representative of target market segments
- Reference Platforms in their respective form factors:

Source: Intel

2U Gateway/Network Server

Source: Intel

2U Server

Source: Intel

Workstations

Source: Intel

Clients

HARDWARE SOLUTIONS

Hardware Solutions

- Legacy Post-silicon Hardware Solution
- What Changed
- Managing Scope
- Options to Manage Change
- Challenges Confronting the New Solutions

Challenges Post-Silicon Hardware

LEGACY POST-SILICON HW SOLUTION

Challenges Post-Silicon Hardware

Validation's goal:

Full functional test of silicon to its specifications

Challenges Post-Silicon Hardware

Validation's goal:

Full functional test of silicon to its specifications

A hardware solution should provide:

- Complete operational coverage of component capability
- Full temperature/thermal and voltage range
- Socket component to remain portable across test platforms
- Optimize the number of system designs
- Provide all systems at silicon power-on

CPU Hardware Solution for Functional Validation (circa 1993)

- 1 socket design, pin grid array

Source: Wikipedia
PGA Socket

CPU Hardware Solution for Functional Validation (circa 1993)

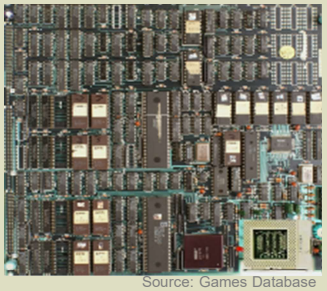
- 1 socket design, pin grid array
- Off the shelf thermal tools

Source: Wikipedia
PGA Socket

Source: Test and Measurement
Forced Air Chiller

CPU Hardware Solution for Functional Validation (circa 1993)

- 1 socket design, pin grid array
- Off the shelf thermal tools
- Two synthetic platforms
  - CPU instruction set testing* (A)
  - CPU + Chipset to cover configurations* (B)



Source: Games Database

A

Source: eBay

B

Source: Wikipedia

PGA Socket

Source: Test and Measurement

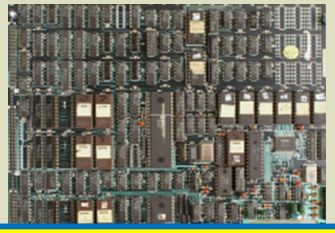
Forced Air Chiller

*Pictures are near representations only, no photographs survive

TestConX™

CPU Hardware Solution for Functional Validation (circa 1993)

- 1 socket design, pin grid array
- Off the shelf thermal tools
- Two synthetic platforms
  - CPU instruction set testing* (A)
  - CPU + Chipset to cover configurations* (B)



A

B

Source: Test and Measurement

Forced Air Chiller

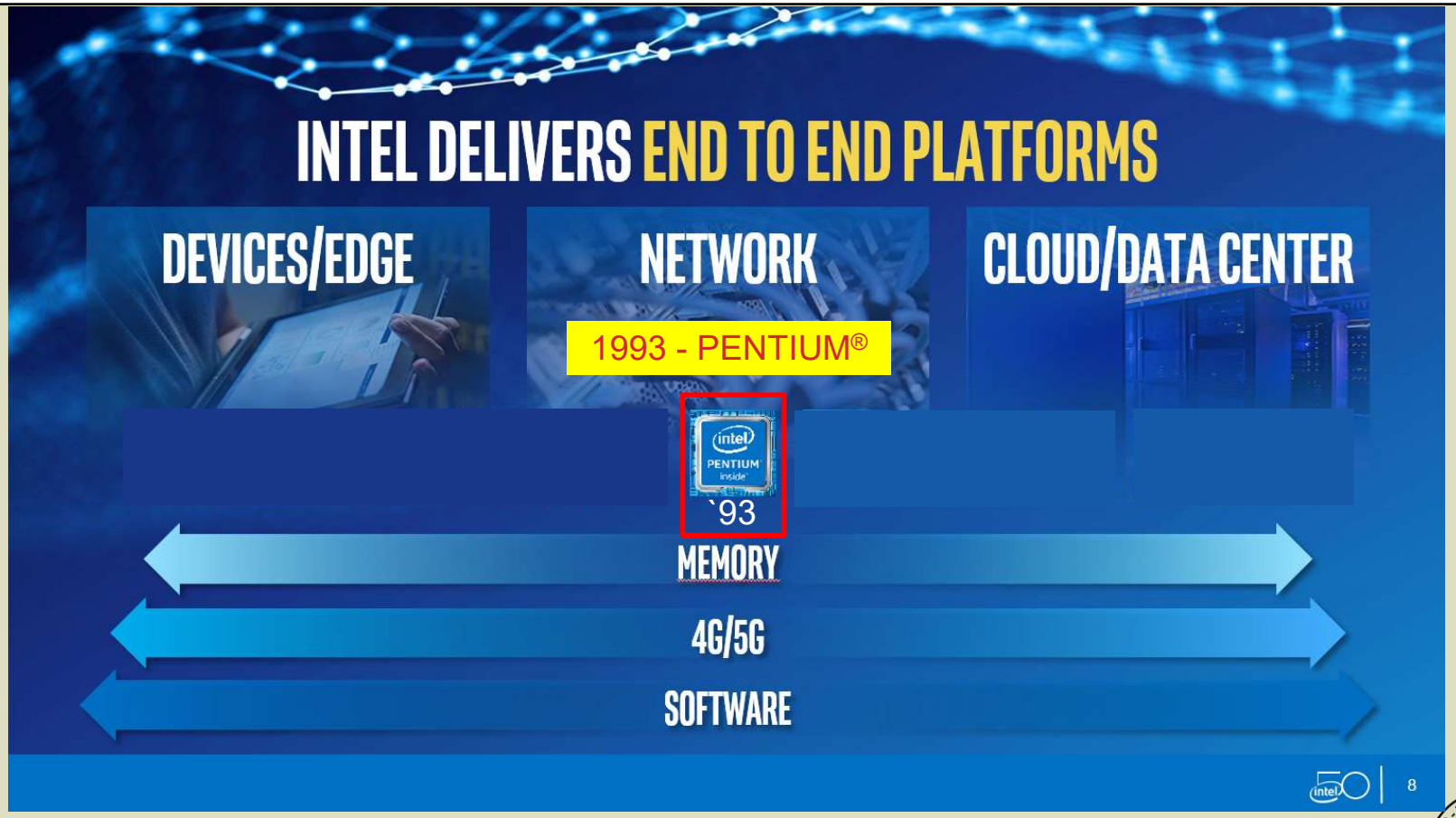
PGA Socket

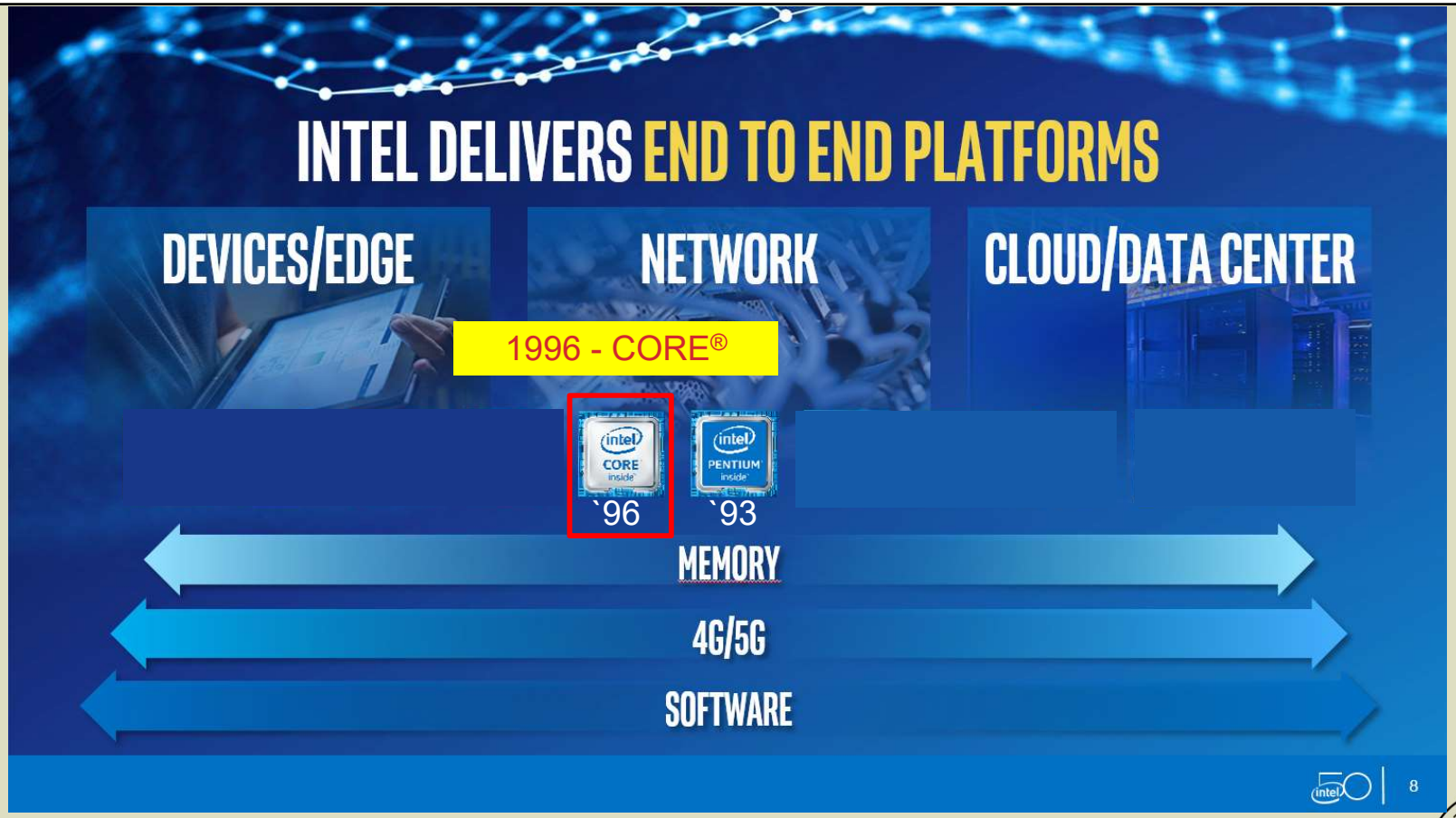
Relatively speaking, not much HW

only, no photographs survive

Hardware Strategy

WHAT CHANGED


INTEL DELIVERS END TO END PLATFORMS
DEVICES/EDGE
NETWORK
CLOUD/DATA CENTER
1993 - PENTIUM®
intel
PENTIUM
inside
`93
MEMORY
4G/5G
SOFTWARE
8
Source: Intel
TestConX™
Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy
78
2000 - 2019
20
YEARS
ANNIVERSARY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NETWORK
CLOUD/DATA CENTER
1996 - CORE®
intel CORE inside
intel PENTIUM inside
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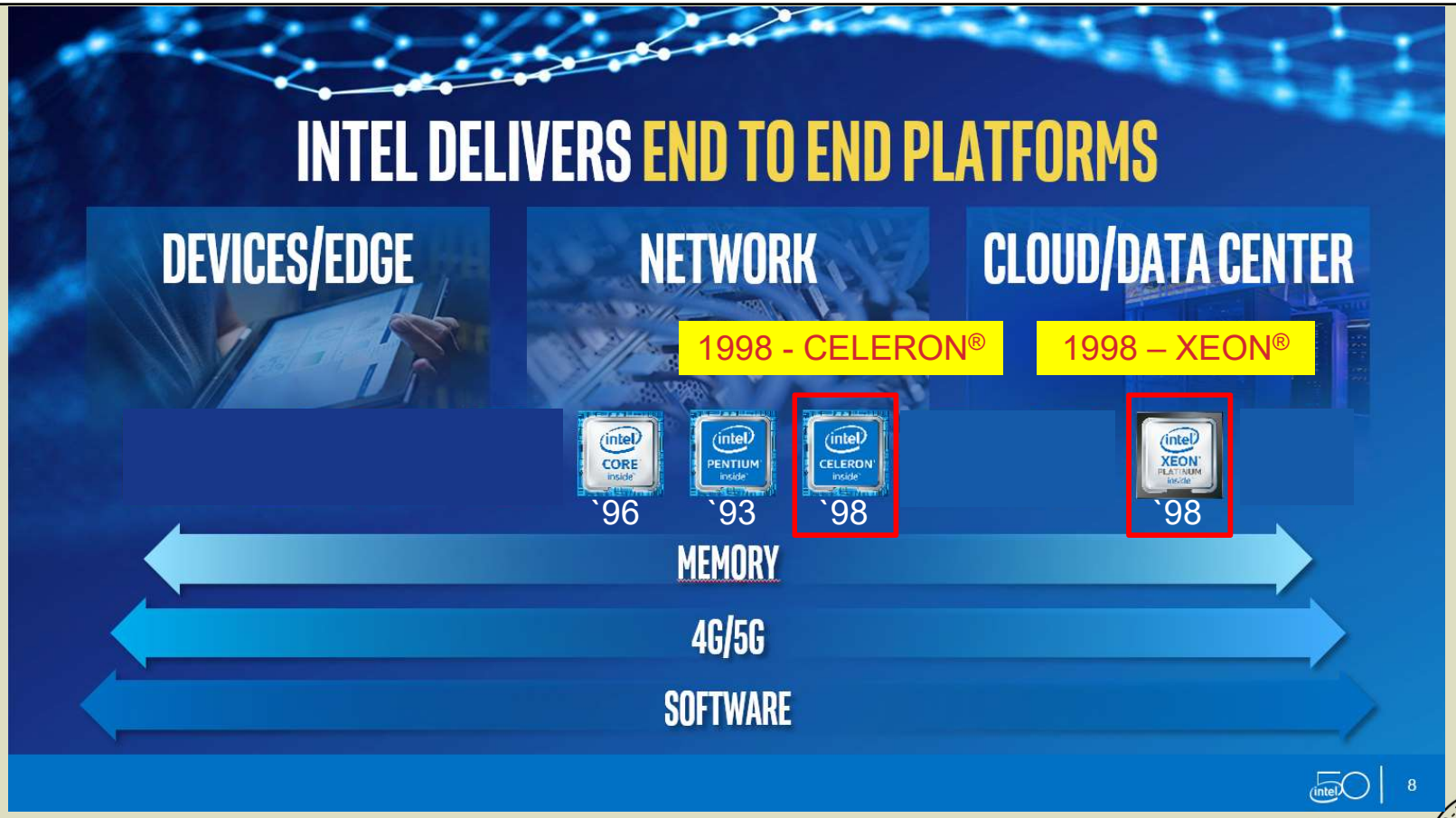
`93
MEMORY
4G/5G
SOFTWARE
8
Source: Intel
TestConX™
Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy
79
2000 - 2019
20 YEARS
ANNIVERSARY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DEVICES/EDGE
NETWORK
CLOUD/DATA CENTER
1998 - CELERON®
1998 – XEON®
CORE
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MEMORY
4G/5G
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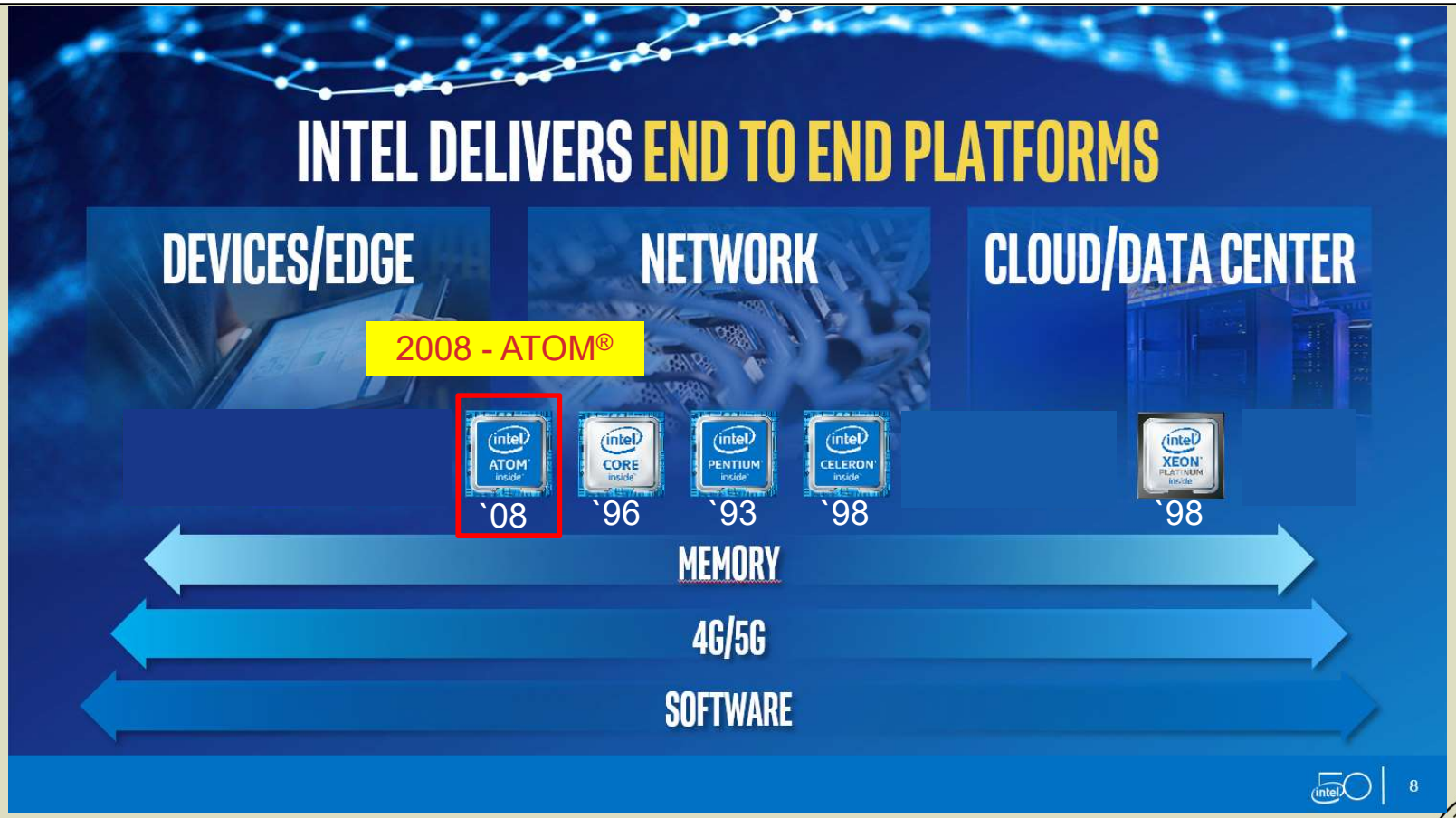
Source: Intel
TestConX™
Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy
80
2000 - 2019
20 YEARS
ANNIVERSARY

80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2008 - ATOM®
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CORE
PENTIUM
CELERON
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MEMORY
4G/5G
SOFTWARE
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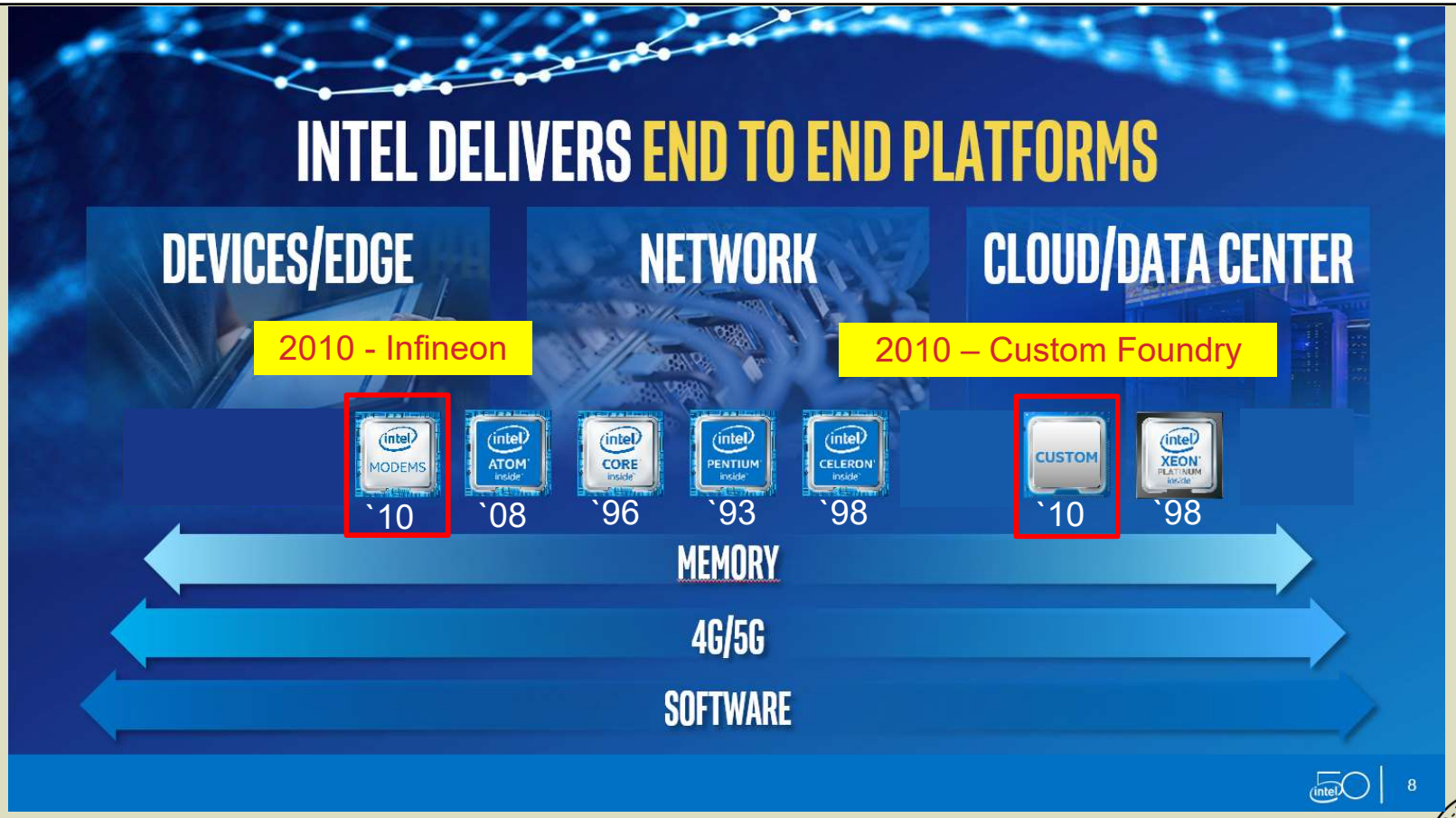
Source: Intel
TestConX
Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy
81
2000 - 2019
20 YEARS
ANNIVERSARY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DEVICES/EDGE
NETWORK
CLOUD/DATA CENTER
2010 - Infineon
2010 – Custom Foundry
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ATOM
CORE
PENTIUM
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CUSTOM
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4G/5G
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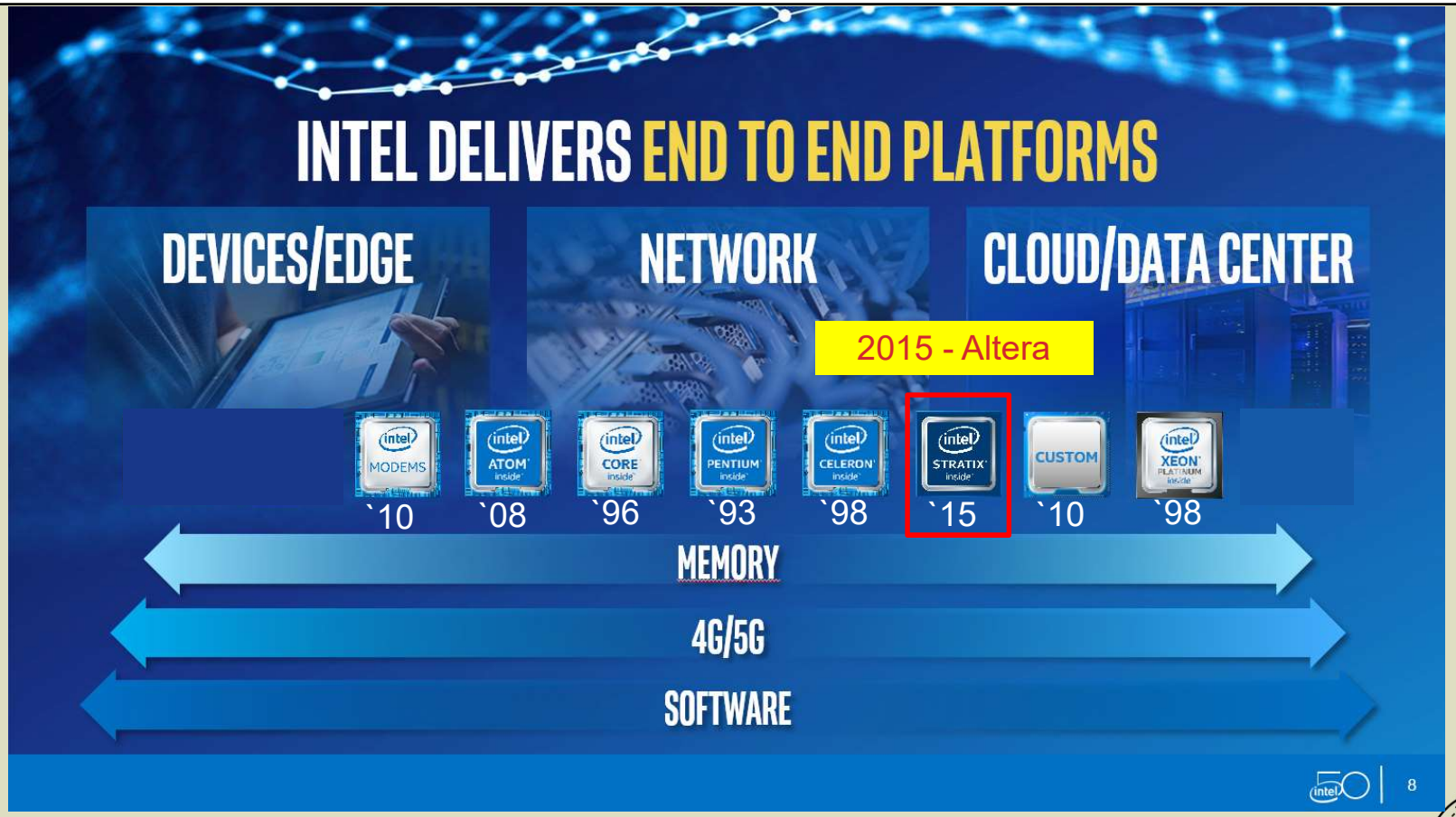
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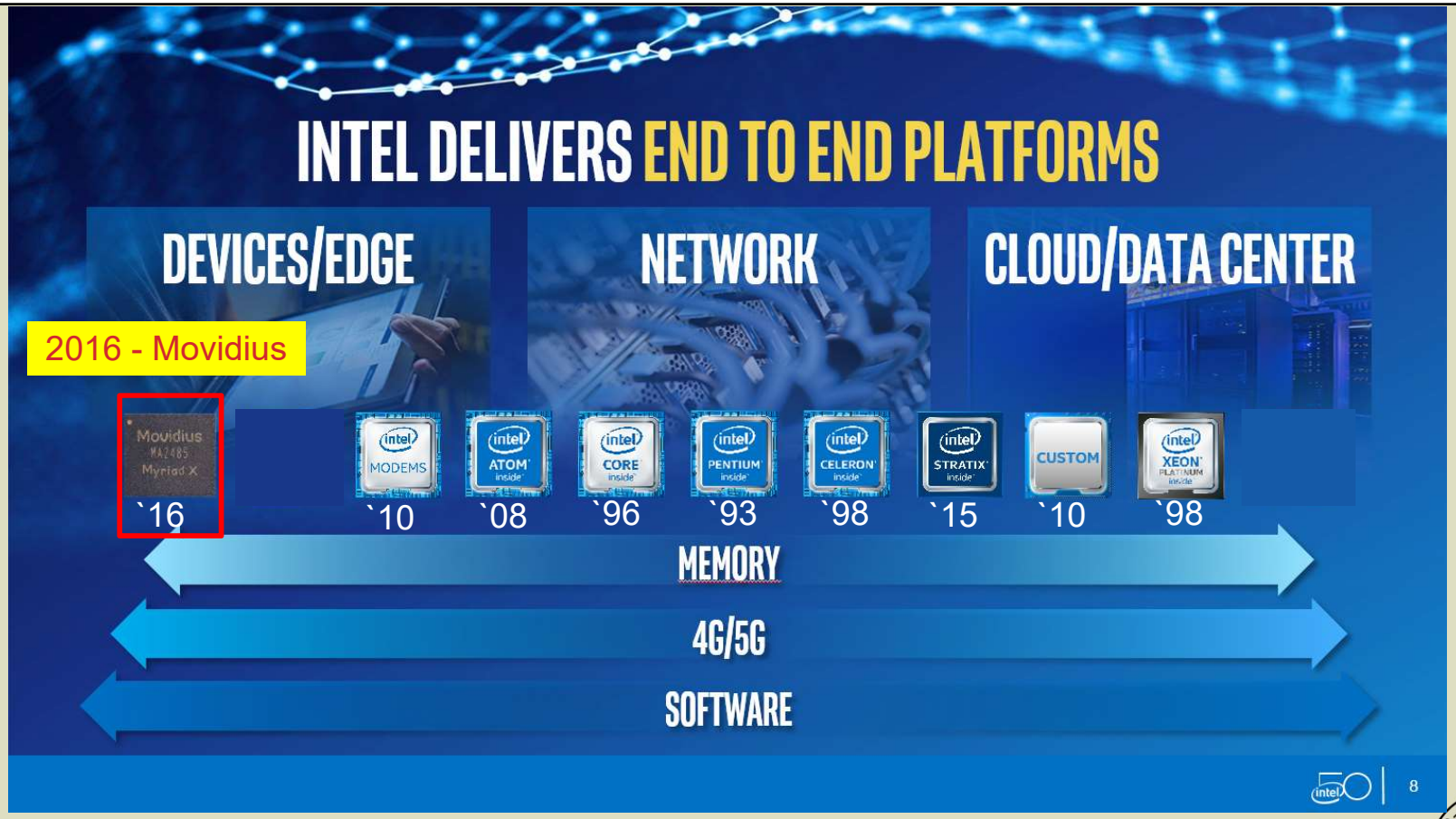
Source: Intel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2016 - Movidius
Movidius
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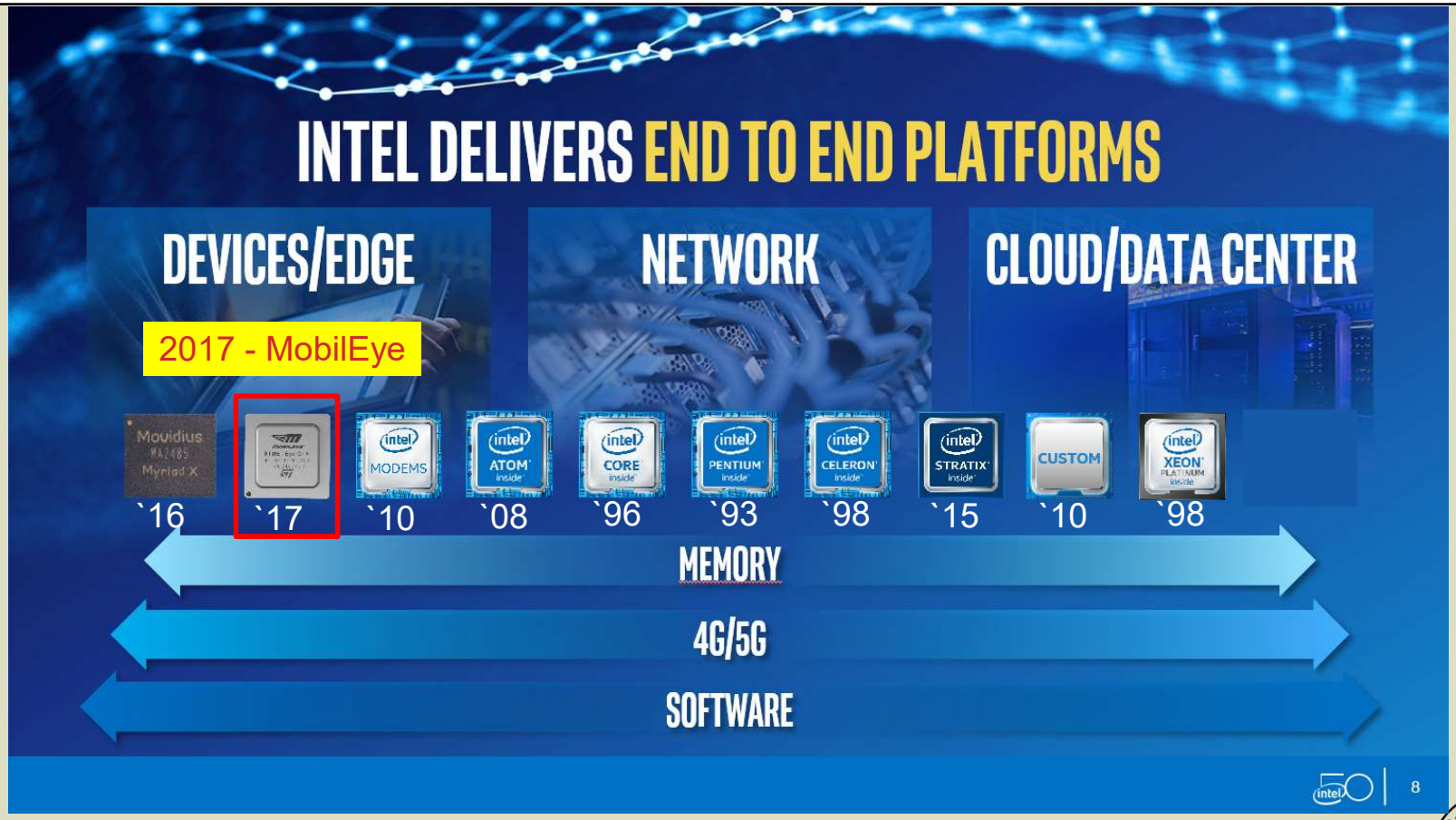
4G/5G
SOFTWARE
8
Source: Intel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2017 - MobilEye
Movidius
MA2485
Myriad X
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4G/5G
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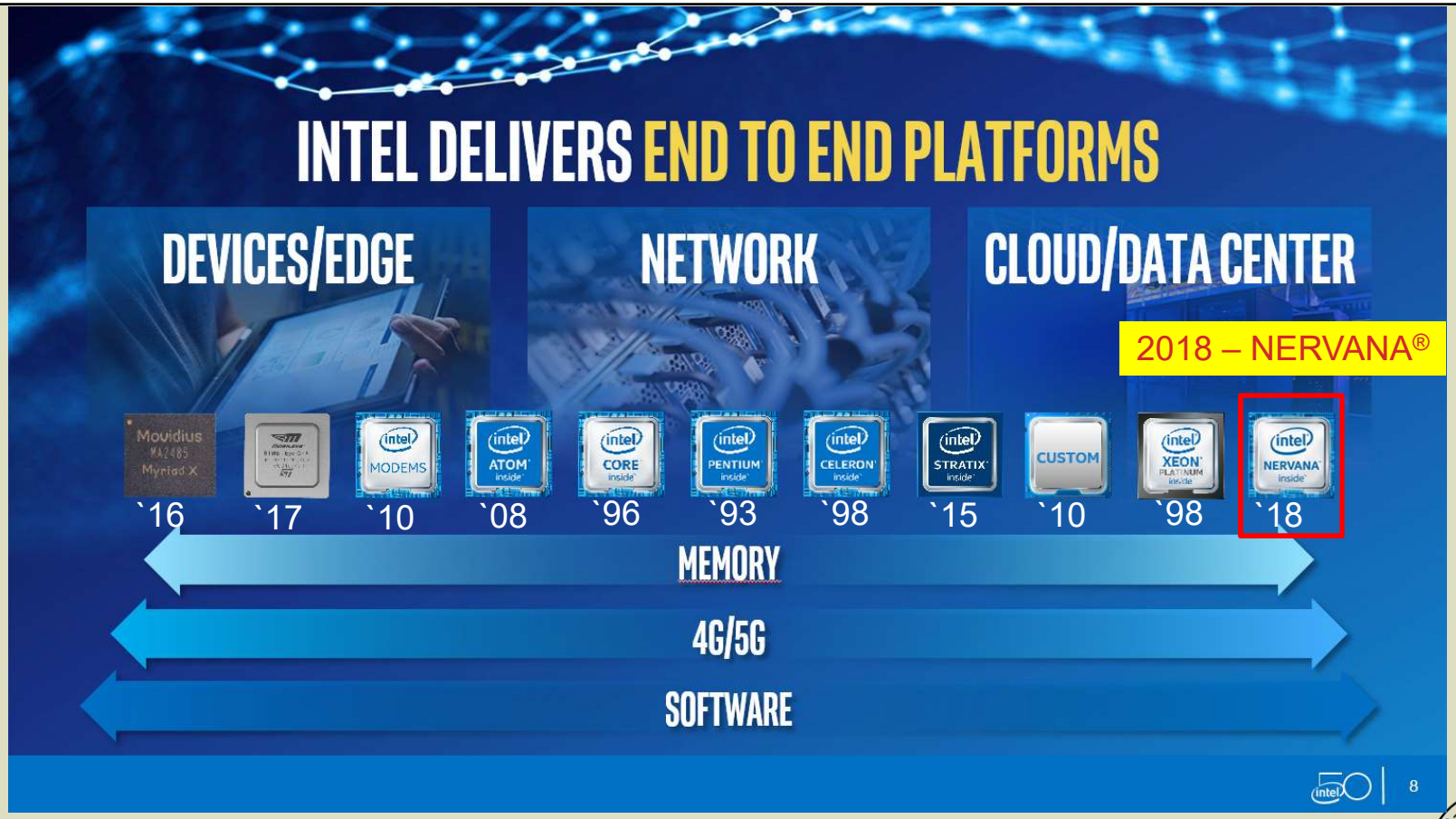
Source: Intel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MEMORY
4G/5G
SOFTWARE
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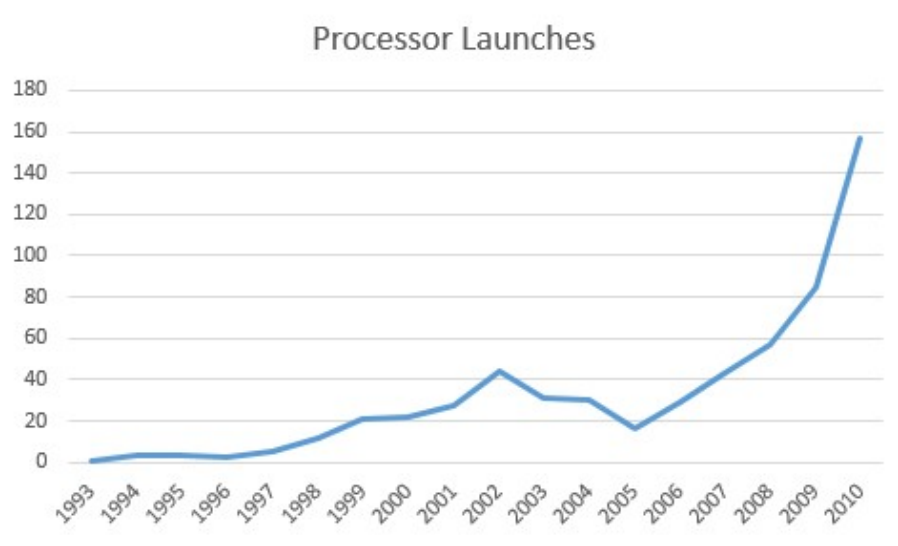
Source: Intel

More products developed and launched



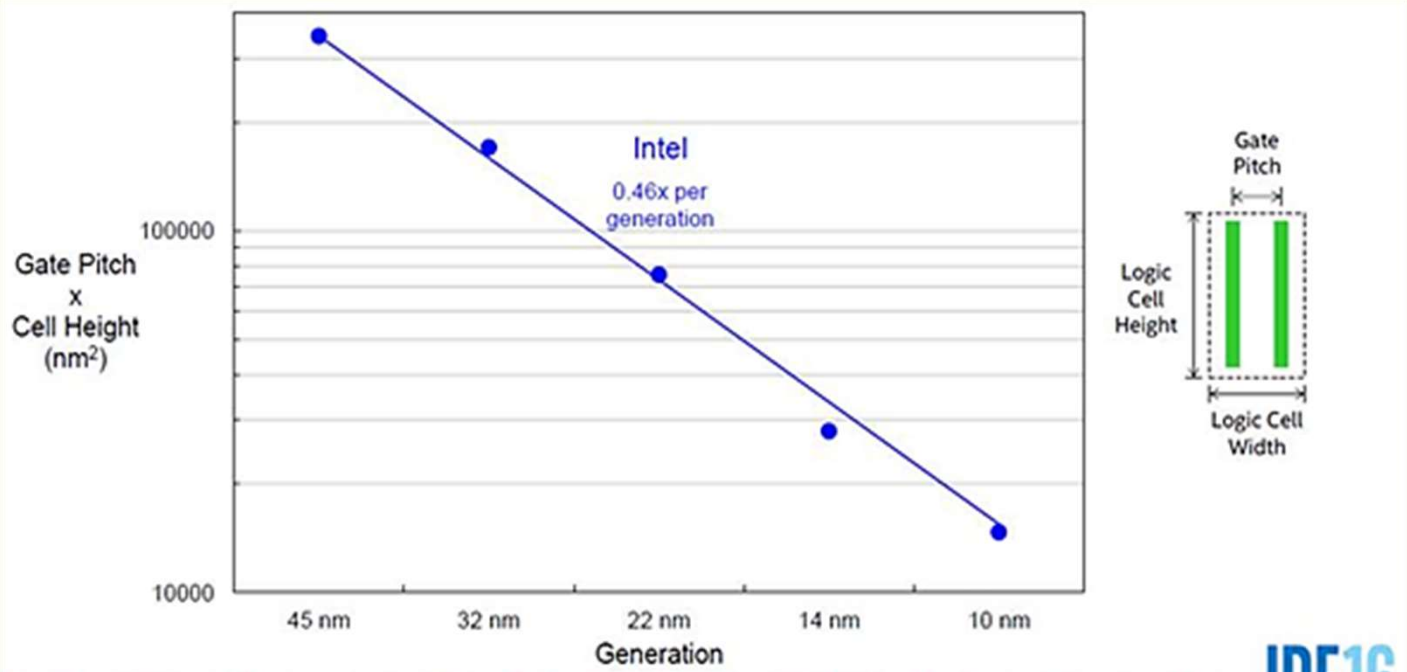
Data sources

2008-2010: https://ark.intel.com/Search/FeatureFilter?productType=processors
1993-2008: https://www.intel.com/pressroom/kits/quickrefyr.htm

Not an exact count, actual numbers are higher due to:

- Inconsistency in reporting of publicly available data
- Non-processor product not included

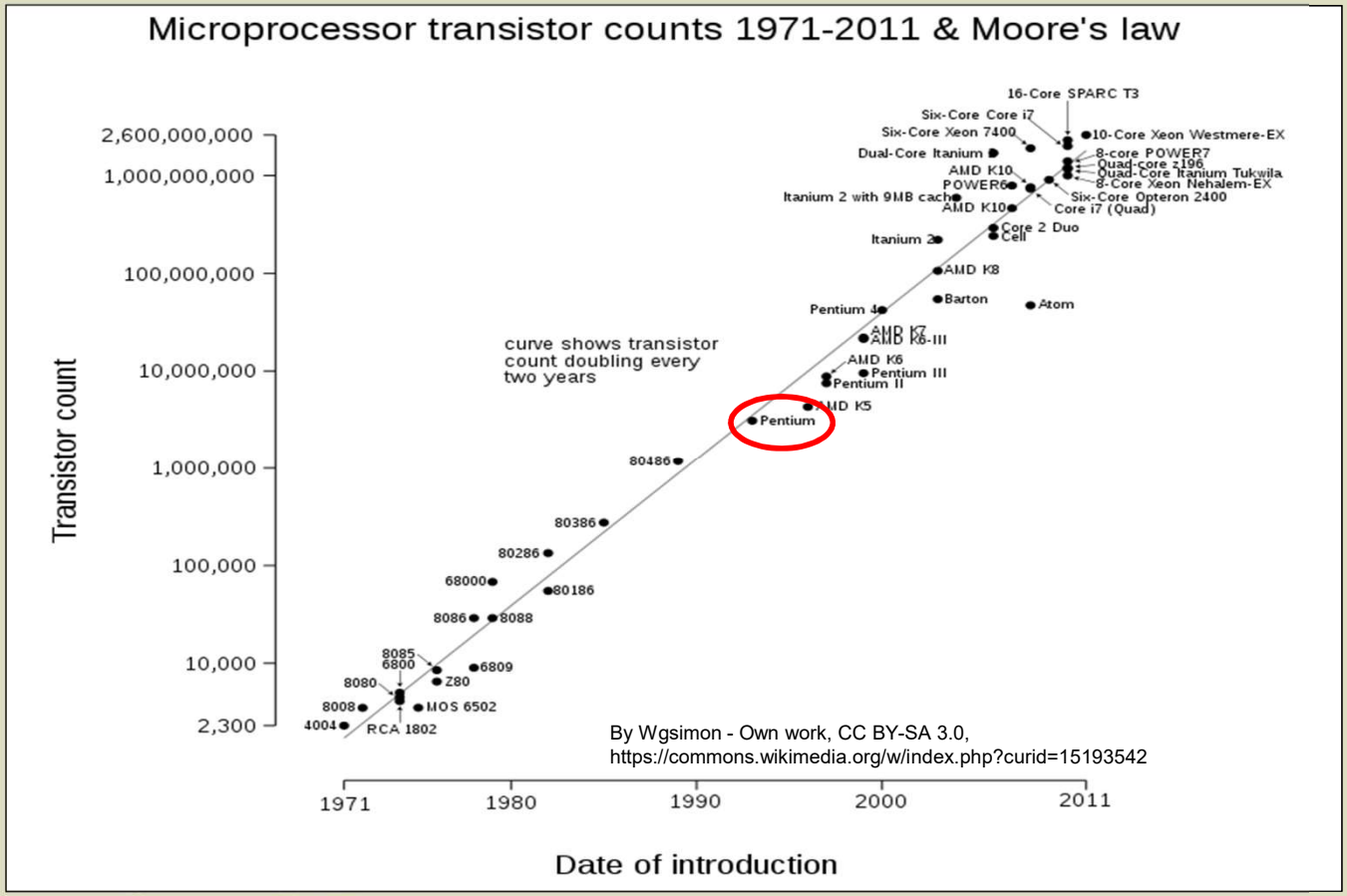
Shrinking Process



Simple gate pitch * cell height logic area metric is scaling ~0.46x per generation

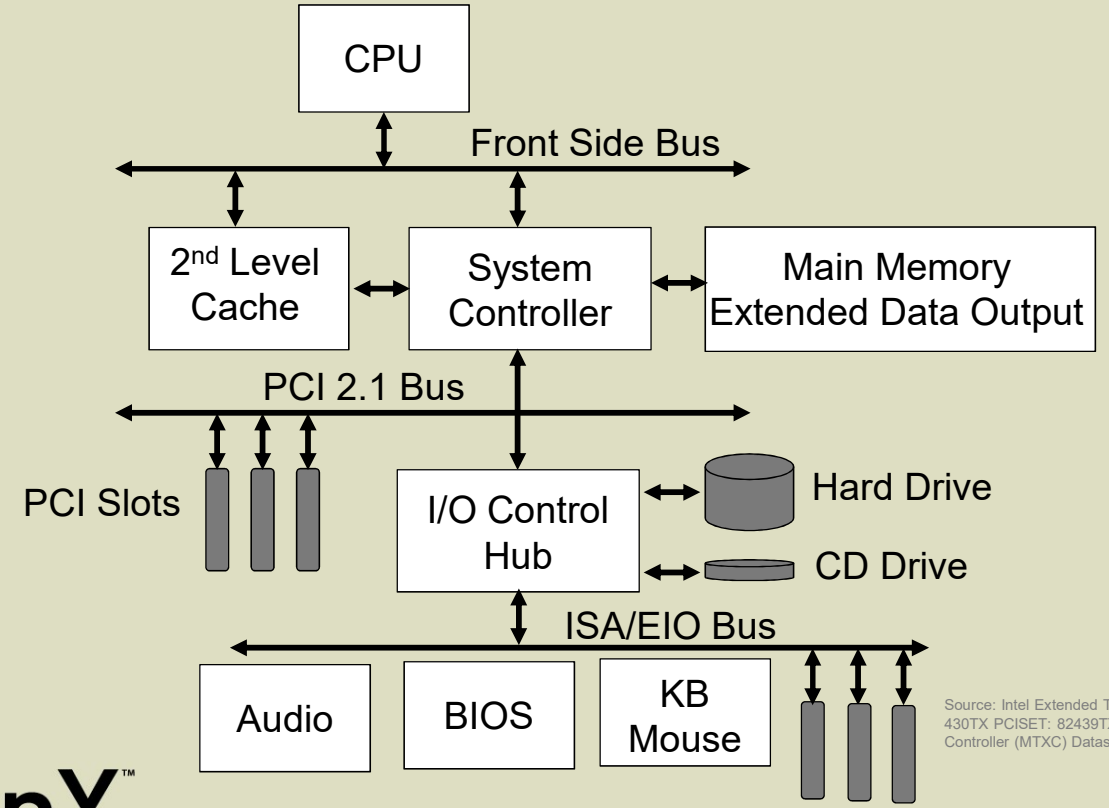
IDF16 INTEL DEVELOPER FORUM

Source: Intel



By Wgsimon - Own work, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=15193542

System Block Diagram (circa 1995)

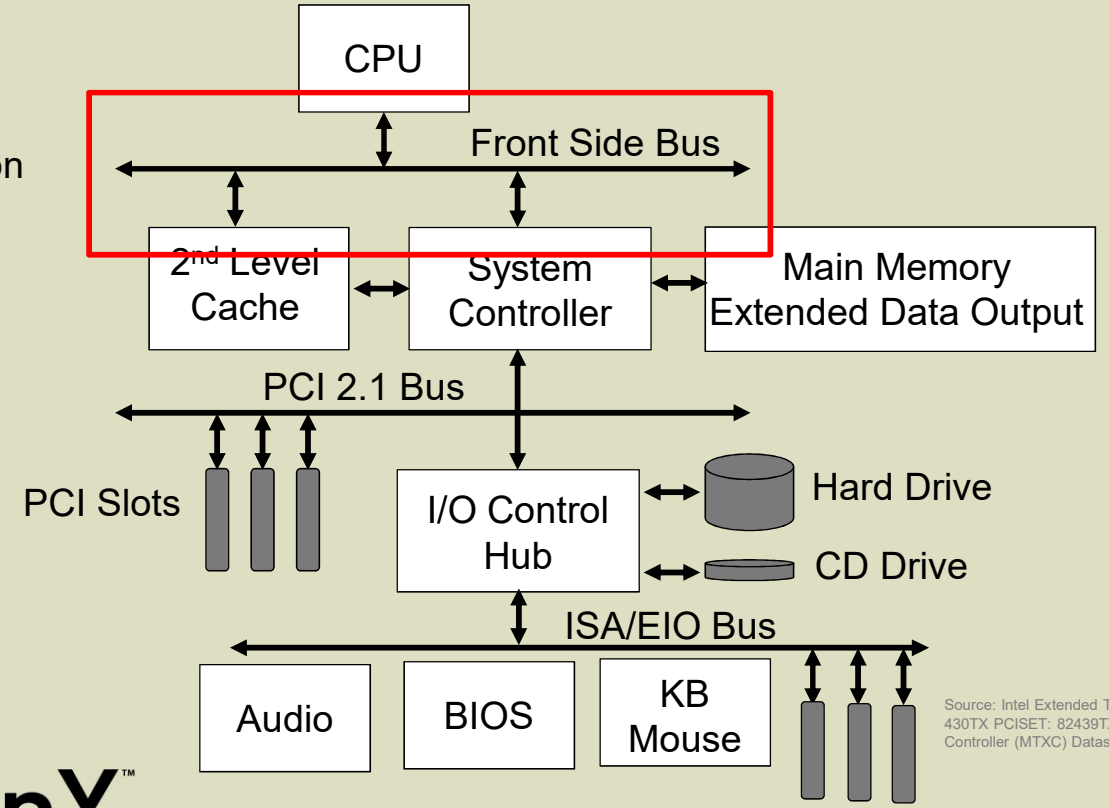


Source: Intel Extended Temperature 430TX PCISET: 82439TX System Controller (MTXC) Datasheet

TestConX™

System Block Diagram (circa 1995)

CPU, Cache, and memory controller on an external bus



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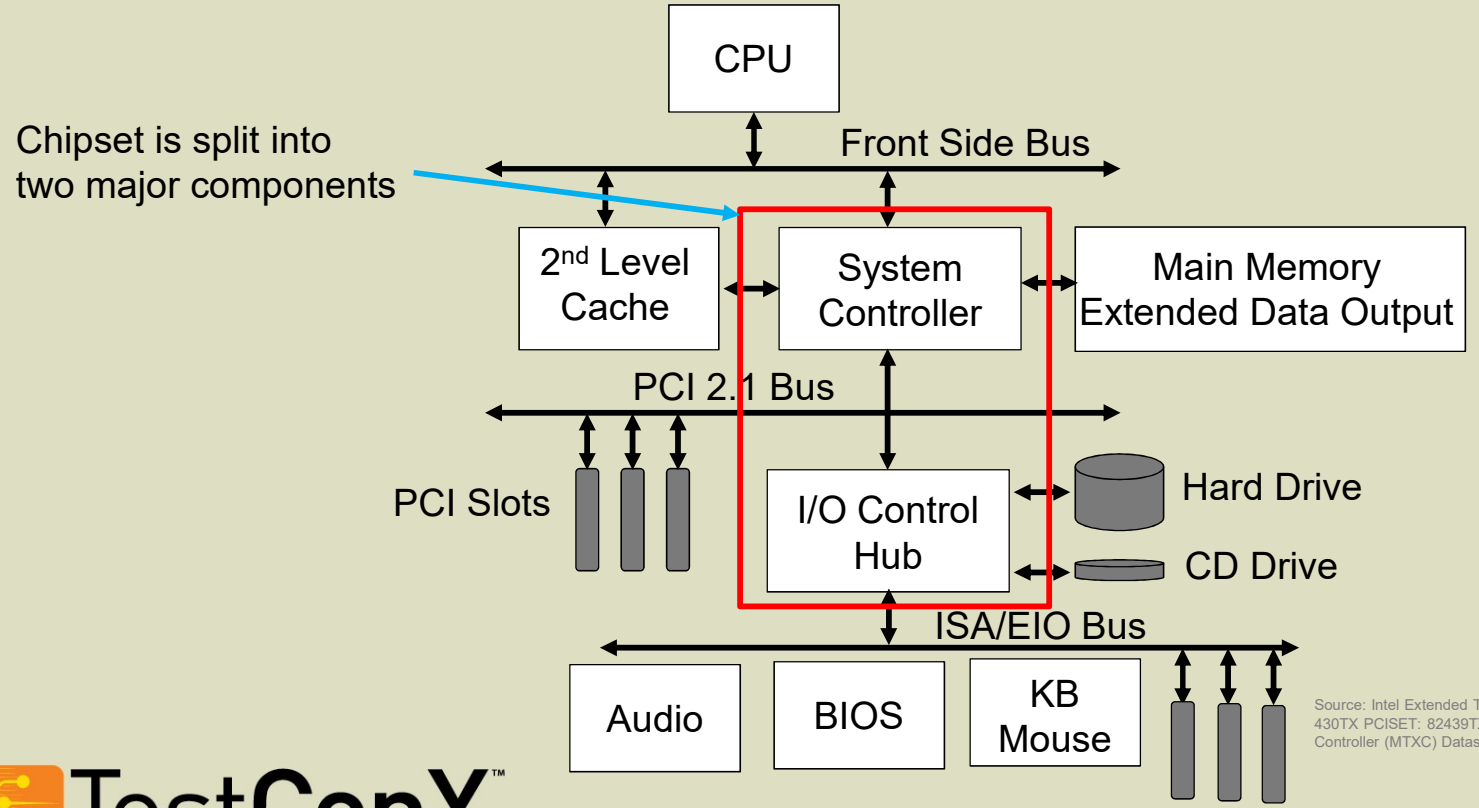
TestConX™

System Block Diagram (circa 1995)



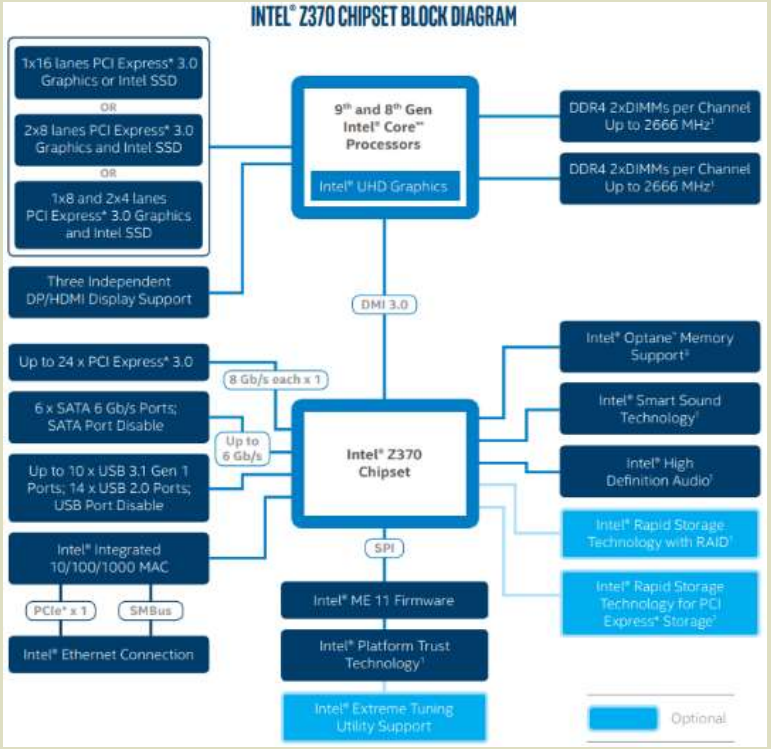
Source: Intel Extended Temperature 430TX PCISET: 82439TX System Controller (MTXC) Datasheet

TestConX™

Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy 92

92

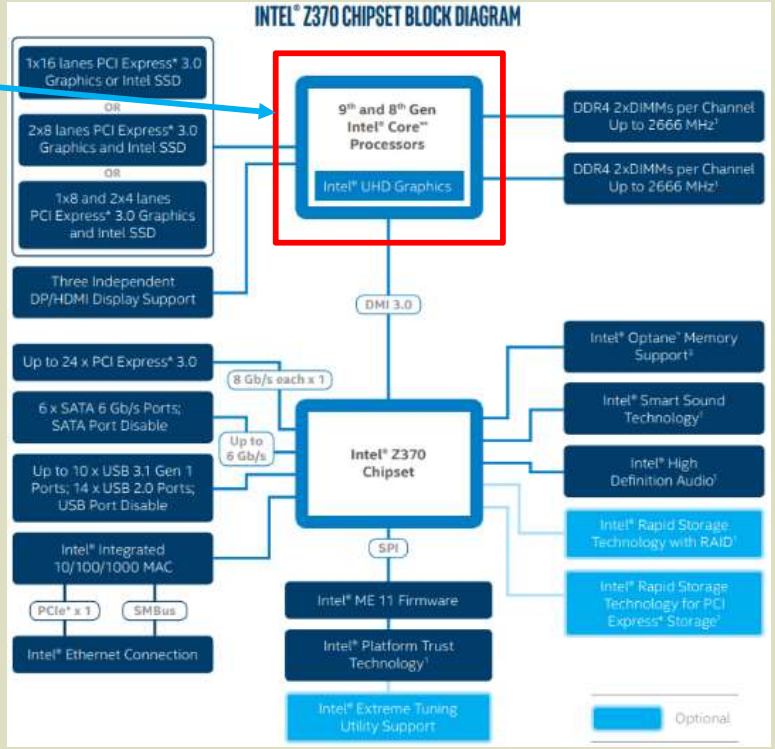
Present Day System Block Diagram



Source: Intel Z370 Product Brief

Present Day System Block Diagram

CPU

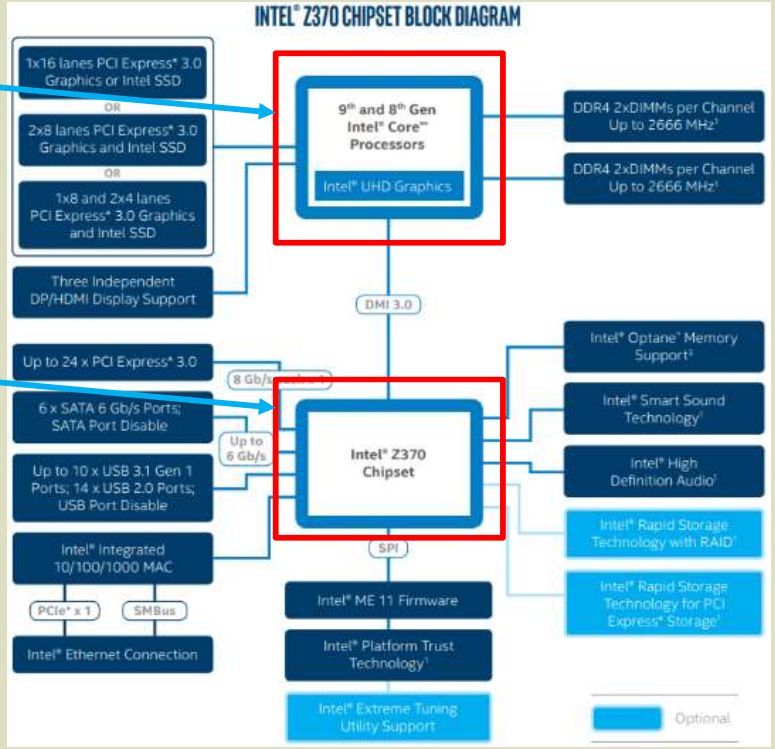


Source: Intel Z370 Product Brief

Present Day System Block Diagram

CPU

Chipset



Source: Intel Z370 Product Brief

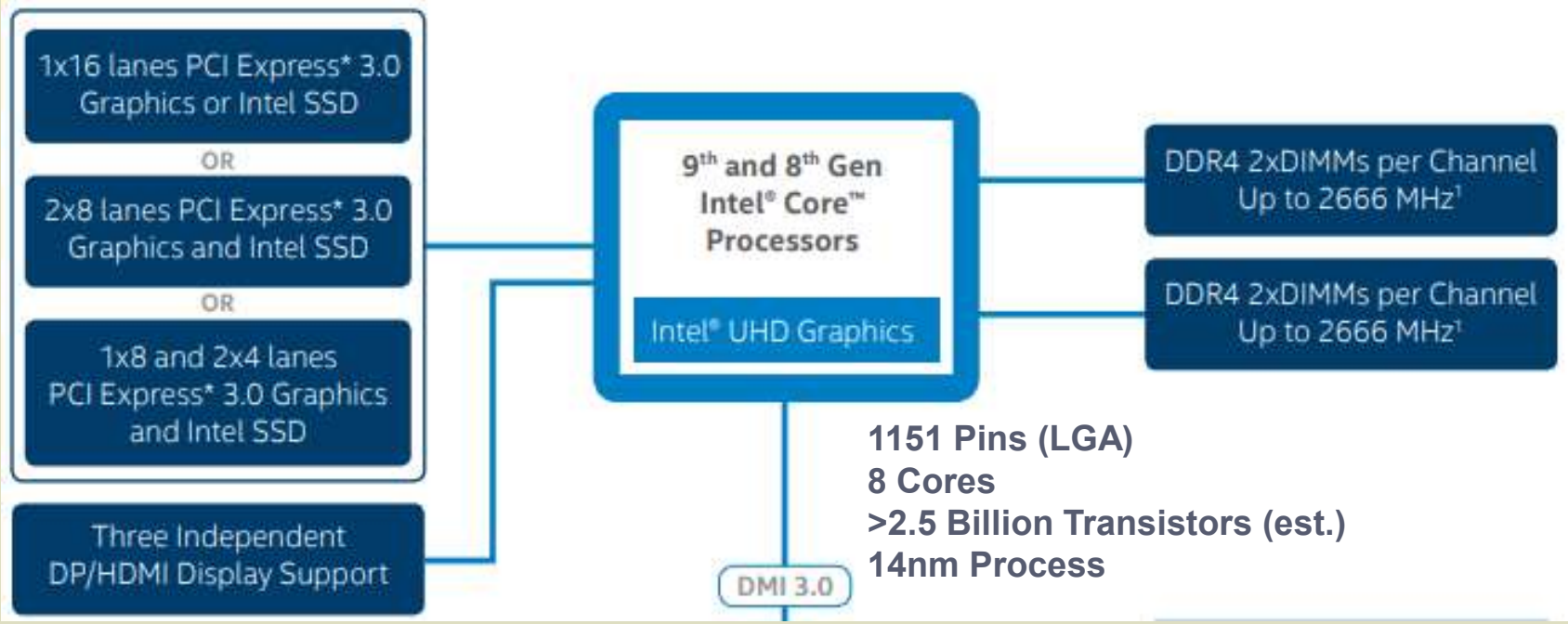
Desktop CPU Circa 1995

320 Pins (PGA)
2 ALUs
3.3 Million Transistors
0.5 µm Process

Major Interfaces
Front Side Bus
- Address
- Data
- Control

Interrupt Pins

Present Day CPU



Source: Intel Z370 Product Brief

Chipset (circa 1995)

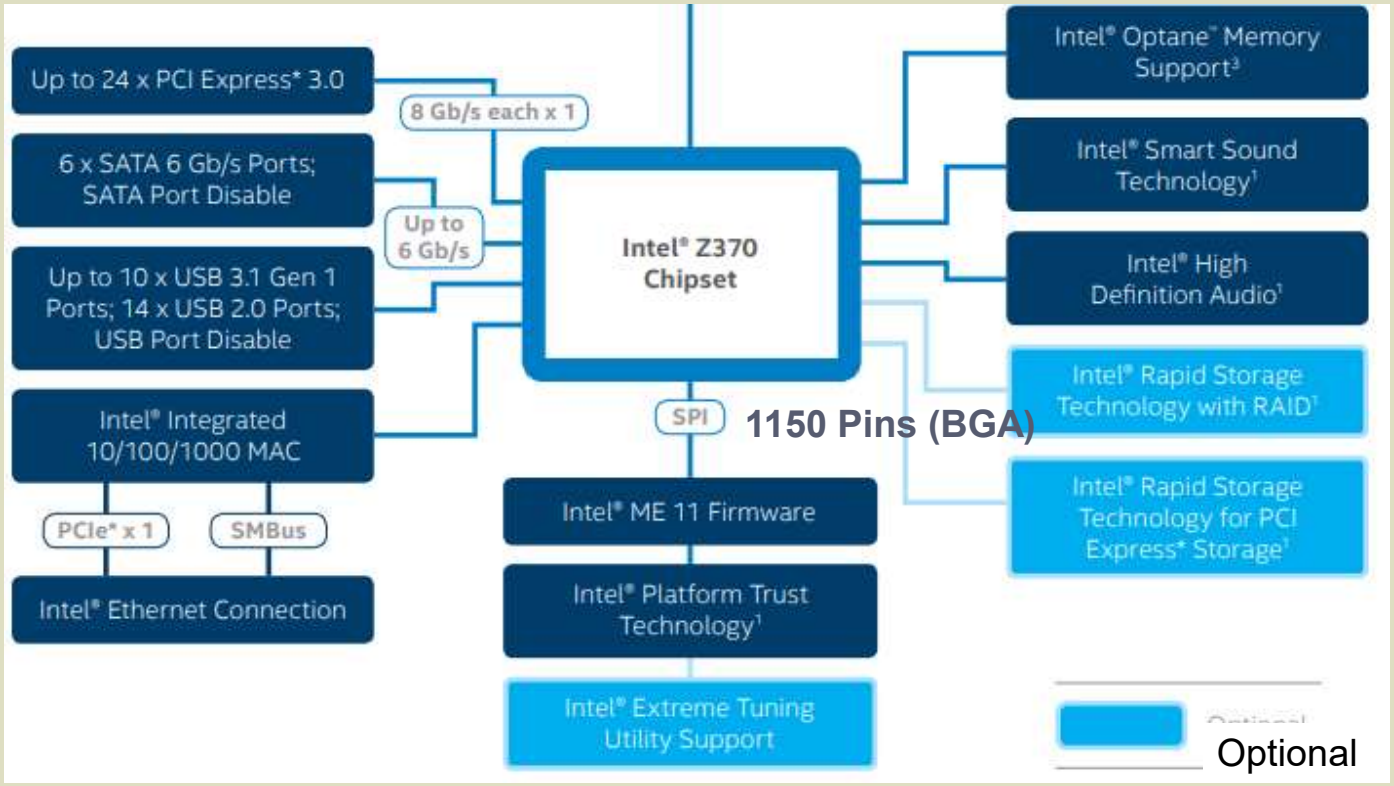
324 Pins (BGA)

Host Bus: Address, Data, Control
Memory Interface: Address, Data, Control
Cache Interface: Address, Tag, Control
PCI Interface: Address/Data, Command, Control

208 Pin (QPF)

PCI Interface: Address/Data, Command, Control
ISA Bus: Address, Data, Control
DMA, Interrupt Control, Error
Power Management Control
Hard disk
USB Controller

Present Day I/O Control Hub



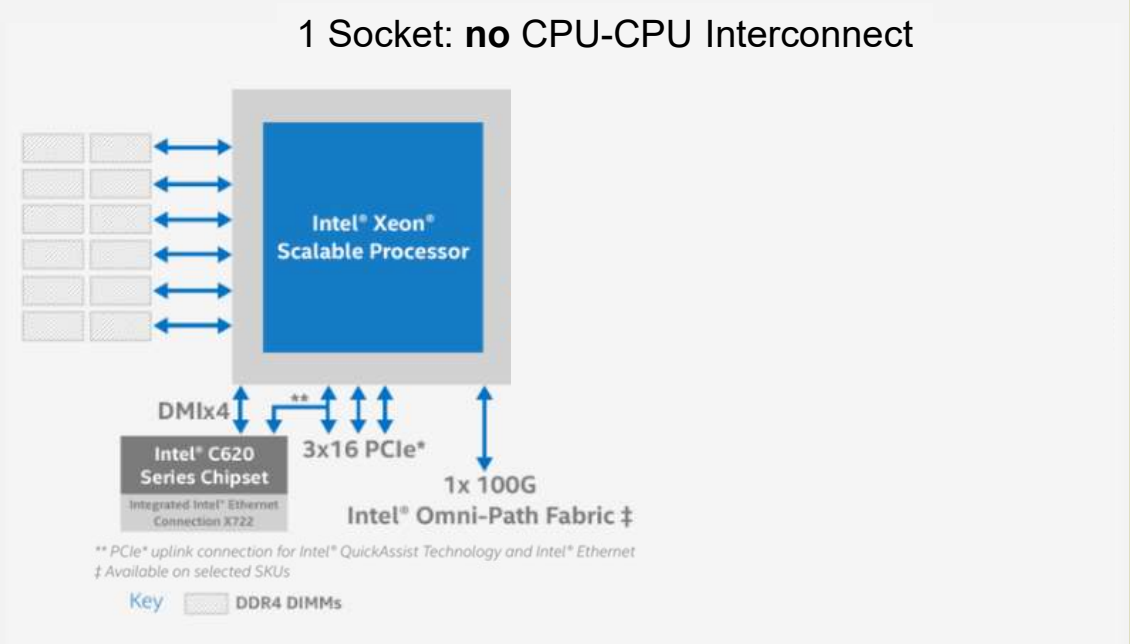
Source: Intel Z370 Product Brief

Post-Silicon Functional Validation

MANAGING SCOPE

Scope Challenge: Intel® XEON® Server Example

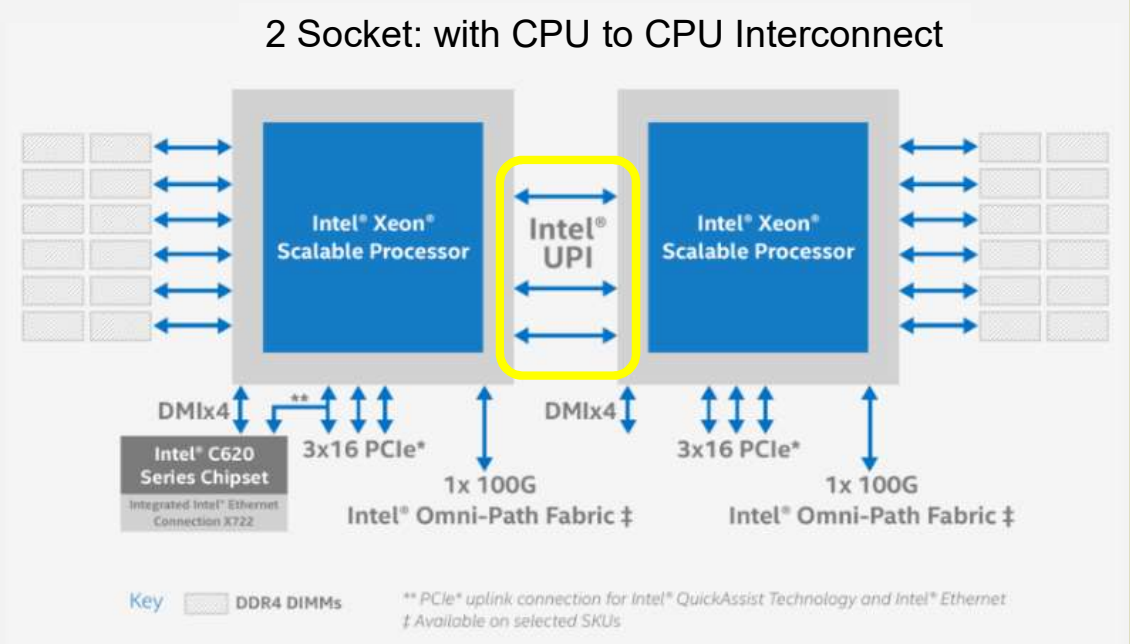
- Challenge: CPU Interconnect



Source: Intel® Xeon® Scalable Processors with Intel® C620 Series Chipsets (Purley) Overview

Scope Challenge: Intel XEON Server Example

- Challenge: CPU Interconnect



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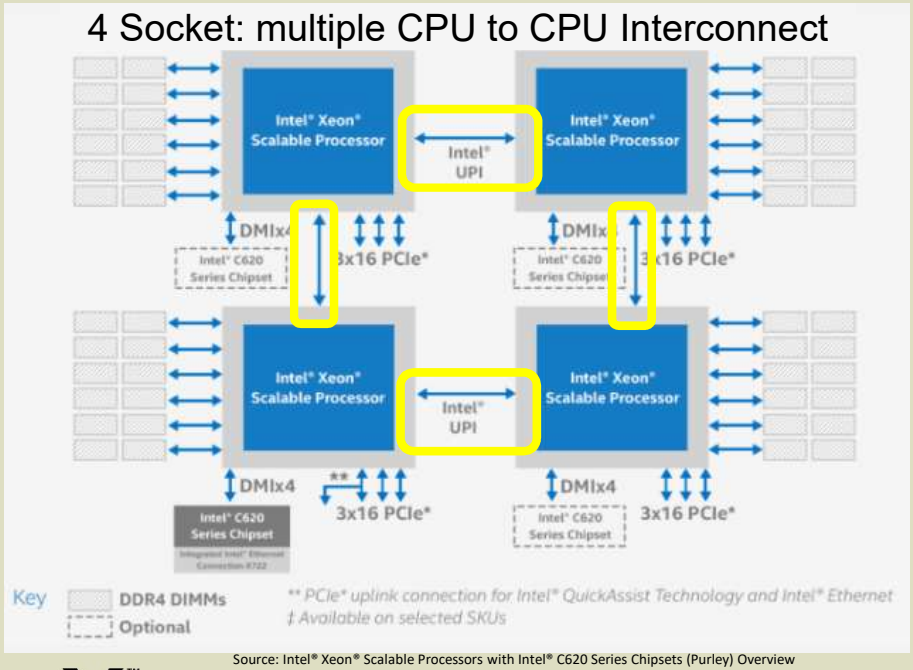
Scope Challenge: Intel XEON Server Example

- Challenge: CPU Interconnect

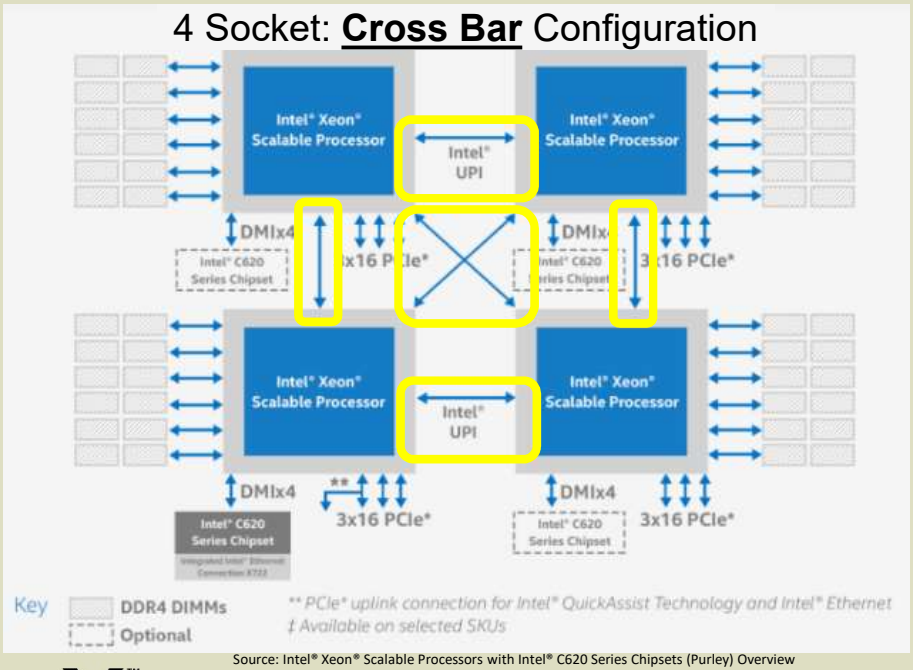


Source: Intel® Xeon® Scalable Processors with Intel® C620 Series Chipsets (Purley) Overview

Scope Challenge: Intel XEON Server Example

- Challenge: CPU Interconnect

4 Socket: **Cross Bar** Configuration



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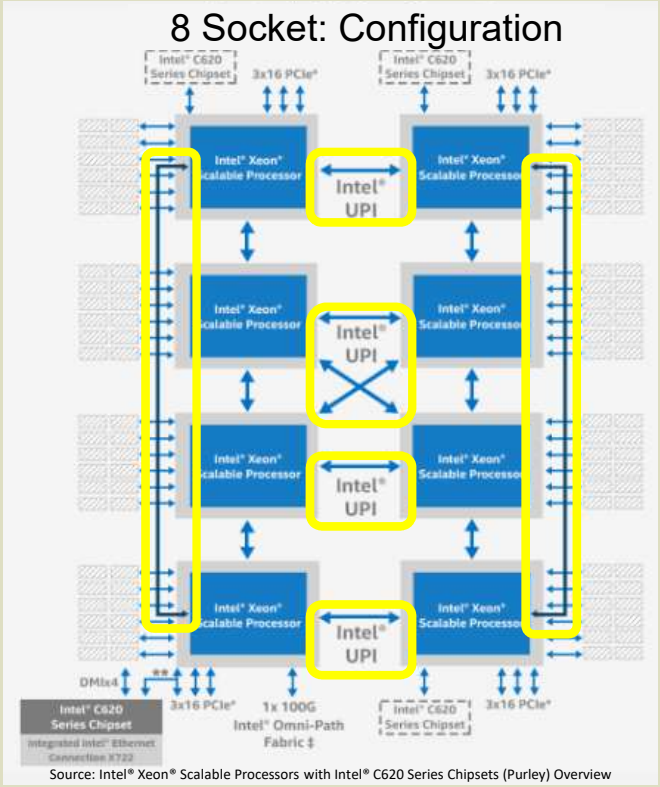
Scope Challenge: Intel XEON Server Example

- Challenge: CPU Interconnect



Source: Intel® Xeon® Scalable Processors with Intel® C620 Series Chipsets (Purley) Overview

Scope Challenge: Intel XEON Server Example

- Challenge: CPU Interconnect

5 CPU interconnect configurations requiring 4 different systems

Scope Challenge: Intel XEON Server Example

- Challenge: Memory Configurations
  - 2 physical DIMM spacing (0.4", 0.65")
  - 3 physical DIMM DQ/DQS lengths
  - 4 different memory types (UDIMM, RDIMM, LRDIMM, SODIMM)
  - 7 memory densities (4, 8, 16, 32, 64, 128, 256 GB)
  - 7 memory speeds
  - 6 memory channels
    - Configurations: 1 DIMM/ch; 2 DIMM/ch; 4 DIMM/ch

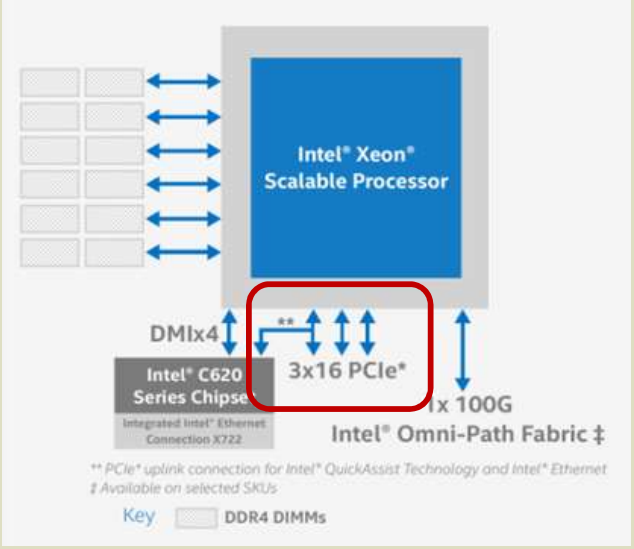
Scope Challenge: Intel XEON Server Example

- Challenge: Memory Conf urations
  - 2 physical DIMM sp ing (6 65")
  - 3 physical DIMM DC
  - 4 different me SODIMM)
  - 7 memory dens
  - 7 memory

>310 memory configurations Requiring 5 different physical systems

Scope Challenge: Intel XEON Server Example

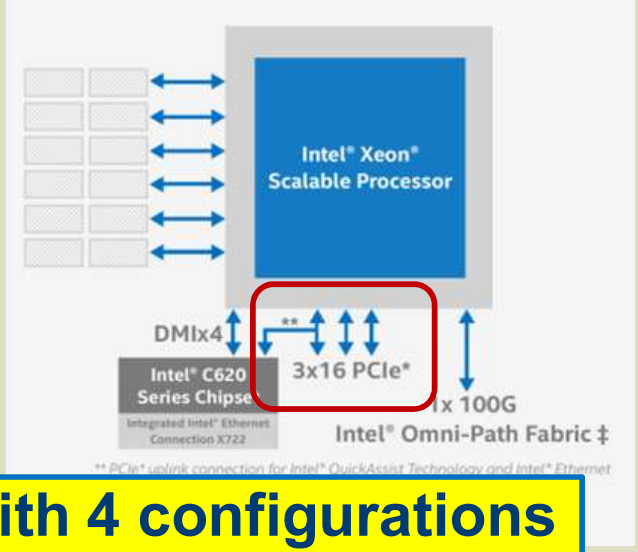
- Challenge: CPU PCIe Topologies
  - 48 PCIe lanes
    - Three, x16 ports
    - Each x16 port support bifurcation into
      - Two x8 ports or
      - One x8 + two x4 ports or
      - Two x4 + one x8 port or
      - Four x4 ports



Source: Intel® Xeon® Scalable Processors with Intel® C620 Series Chipsets (Purley) Overview

Scope Challenge: Intel XEON Server Example

- Challenge: CPU PCIe Topologies
  - 48 PCIe lanes
    - Three, x16 ports
    - Each x16 port support bifurcation into
      - Two x8 ports or
      - One x8 + two x4 ports or
      - Two x4 + one x8 port or
      - Four x4 ports



Combination of 3 ports, each with 4 configurations or 4^3 combinations

Scope Challenge: Intel XEON Server Example

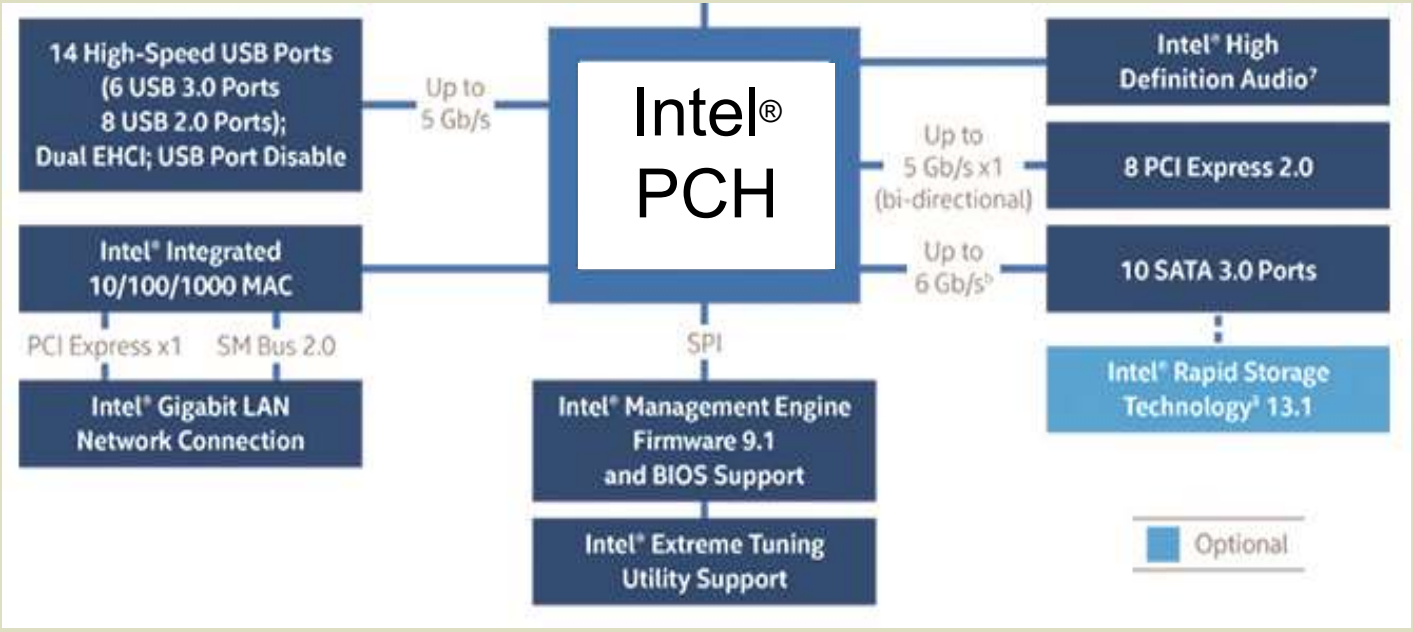
- Challenge: CPU PCIe Topologies
  - 48 PCIe lanes
    - Three, x1[illegible]orts
    - Each x16 po[illegible]
      - Two x8
      - One x8 + tw[illegible]
      - Two x4 + one[illegible]
      - Four x4 por[illegible]

64 PCIe IO configurations

Combination of 3 ports, each with 4 configurations or 4^3 combinations

Scope Challenge: Intel XEON Server Example

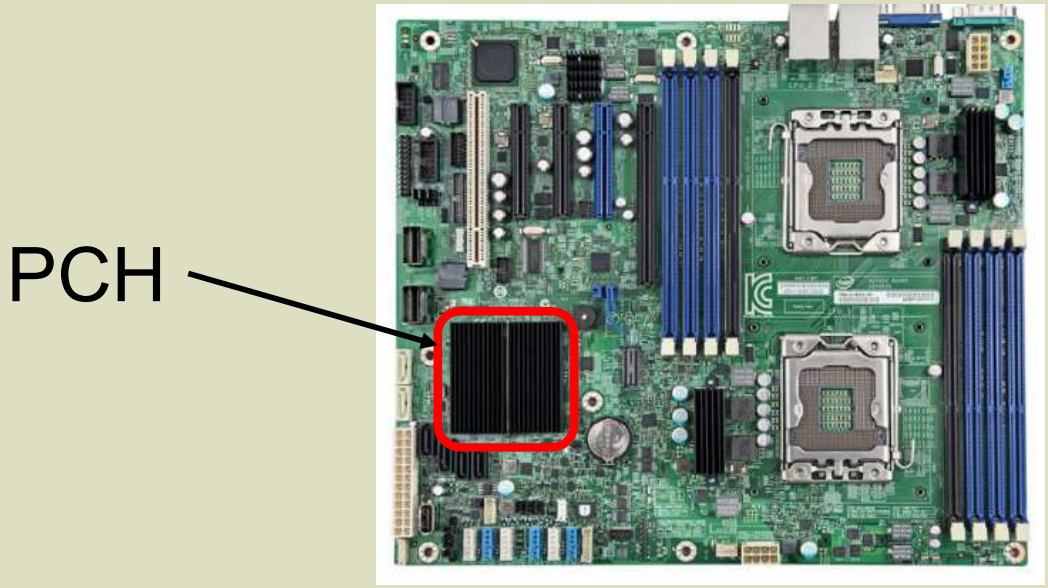
- Challenge: Platform Control Hub (PCH) IO Topologies



Source: Intel® X99 Chipset Block Diagram

Scope Challenge: Intel XEON Server Example

- Challenge: Platform Control Hub (PCH) IO Topologies



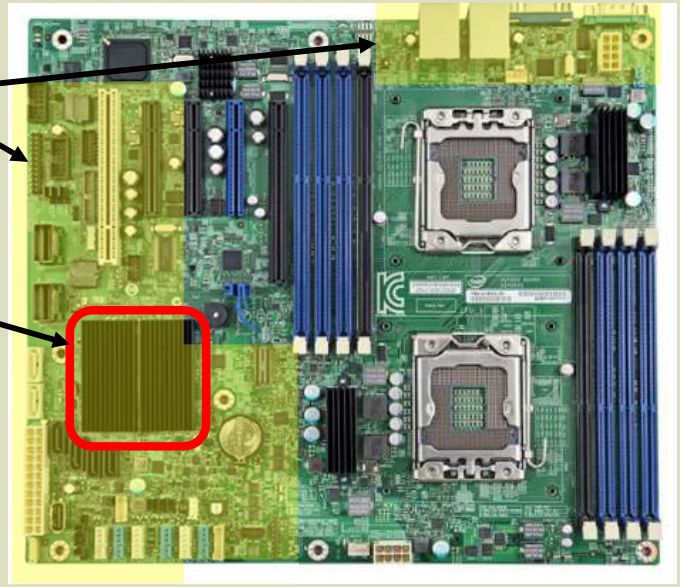
Source: Arc.intel.com

Scope Challenge: Intel XEON Server Example

- Challenge: Platform Control Hub (PCH) IO Topologies

PCH functional areas shaded yellow

PCH



Source: Arc.intel.com

Scope Challenge: Intel® XEON® Server Example

- Challenge: Platform Control Hub IO Topologies

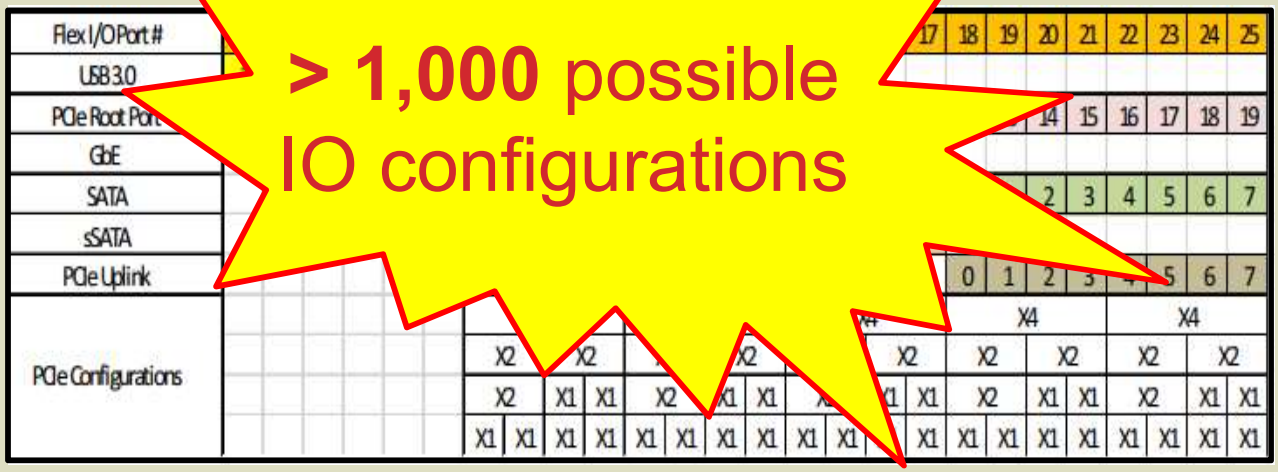
PCH Flexible I/O can be configured to meet the needs of the OEM or ODM

Flex I/O Port #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
USB 3.0	1	2	3	4	5	6	7	8	9	10																
PCIe Root Port							0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
GbE																										
SATA																			0	1	2	3	4	5	6	7
sSATA													0	1	2	3	4	5								
PCIe Uplink																			0	1	2	3	4	5	6	7
PCIe Configurations							X4				X4				X4				X4				X4			
							X2		X2		X2		X2		X2		X2		X2		X2		X2		X2	
							X2		X1	X1	X2		X1	X1	X2		X1	X1	X2		X1	X1	X2		X1	X1
							X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1

Scope Challenge: Intel® XEON® Server Example

- Challenge: Platform Control Hub IO Topologies

PCH [illegible] IO can be configured to [illegible] ODM



How Many Systems are Needed?

Scope Challenge: Intel® XEON® Server Example

- Summary:
  - CPU topologies: 5

System Count

Scope Challenge: Intel® XEON® Server Example

- Summary:
  - CPU topologies: 5 ⟶ System Count: 4

Scope Challenge: Intel® XEON® Server Example

- Summary:
  - CPU topologies: 5 → 4 (System Count)
  - Memory configurations: >310

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	1000?

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	10

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	10
– Full temperature range	
– Full frequency and voltage range	

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	10
– Full temperature range	1
– Full frequency and voltage range	1

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	10
– Full temperature range	1
– Full frequency and voltage range	1

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	
– Memory system configurations: 8	8
– CPU PCIe configurations: 64	16
– PCH Flexible I/O configurations: >1000	10
– Full temperature range	1
– Full frequency and voltage range	1
	Total: 40

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	

Number of systems to be designed and built is a judgment call based on priority, risk, schedule, and cost

– Full frequency and voltage range	1
Total:	40

Scope Challenge: Intel® XEON® Server Example

- Summary:

	System Count
– CPU topologies: 5	4
– Memory configurations: >310	

Number of systems to be designed and built is a judgment call based on priority, risk, schedule, and cost
Most likely, it is not 40 systems

Total: 40

Result

- A “build everything and anything” approach will not scale with the number of configurations a given product can support and the number of products to be launched
  - Cost:
    - Negative impact to product profitability
  - Schedule:
    - Lead time to develop and deploy validation HW was high relative to silicon product development
  - Resources:
    - Staffing for development and validation must be realistic

Options to Manage Change

- Shift efforts to pre-silicon RTL validation
- Shift efforts to Reference Platforms
- Reduce synthetic platforms

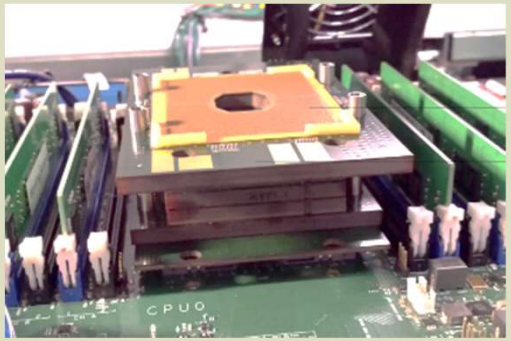

Source: www.herzing.edu
Pre-silicon RTL


Source: Intel
Reference Platform

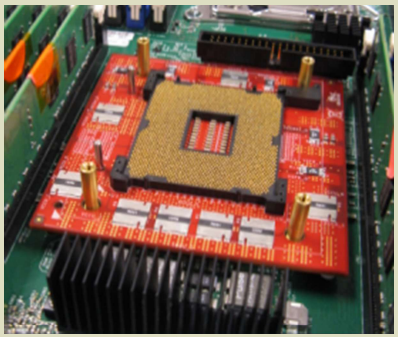

Source: Intel
Synthetic Platform

Augment Reference Platforms

- Apply new capability to augment RP with interposers that added functionality without impacting its design



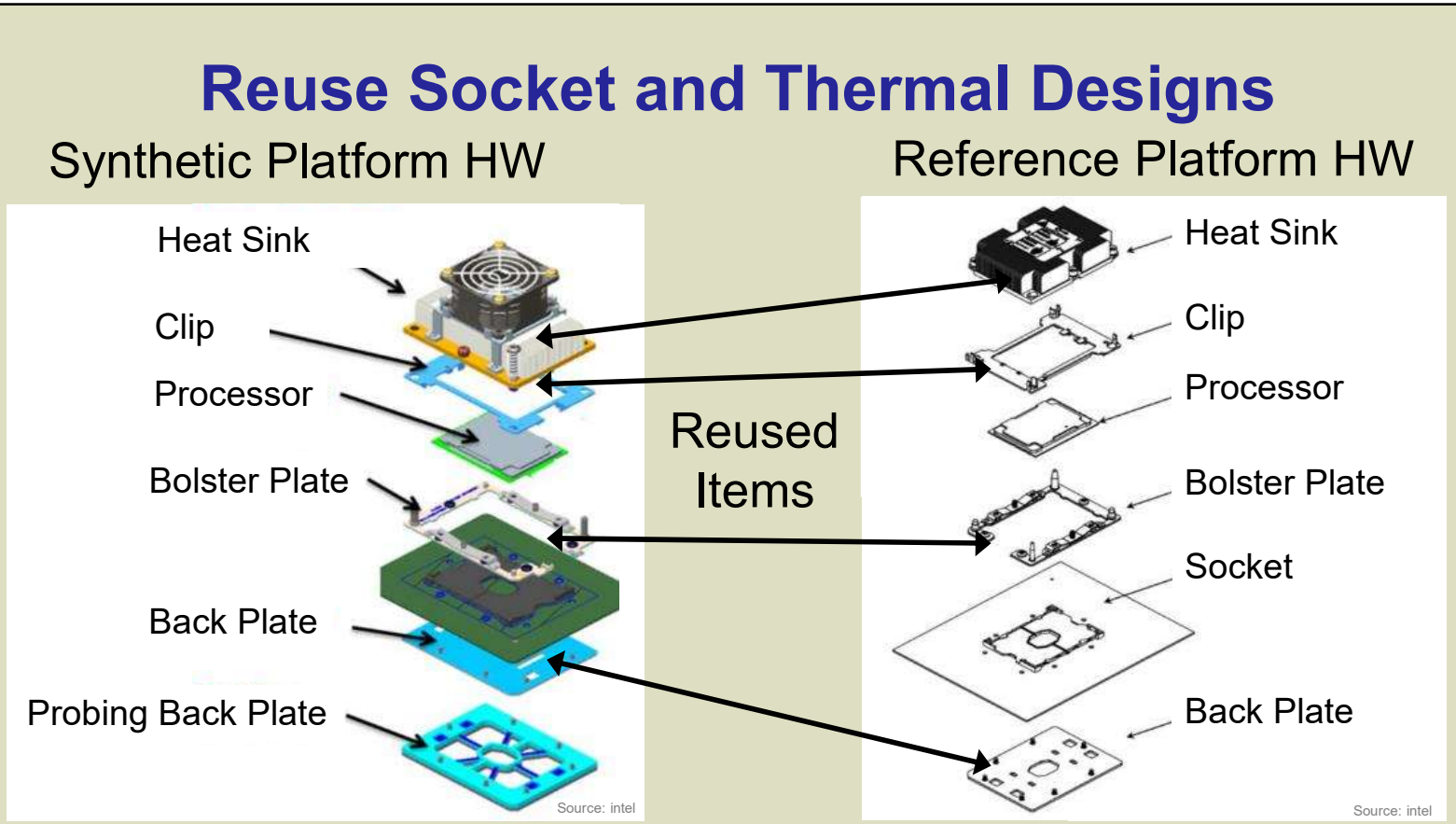
Source: intel


Source: intel

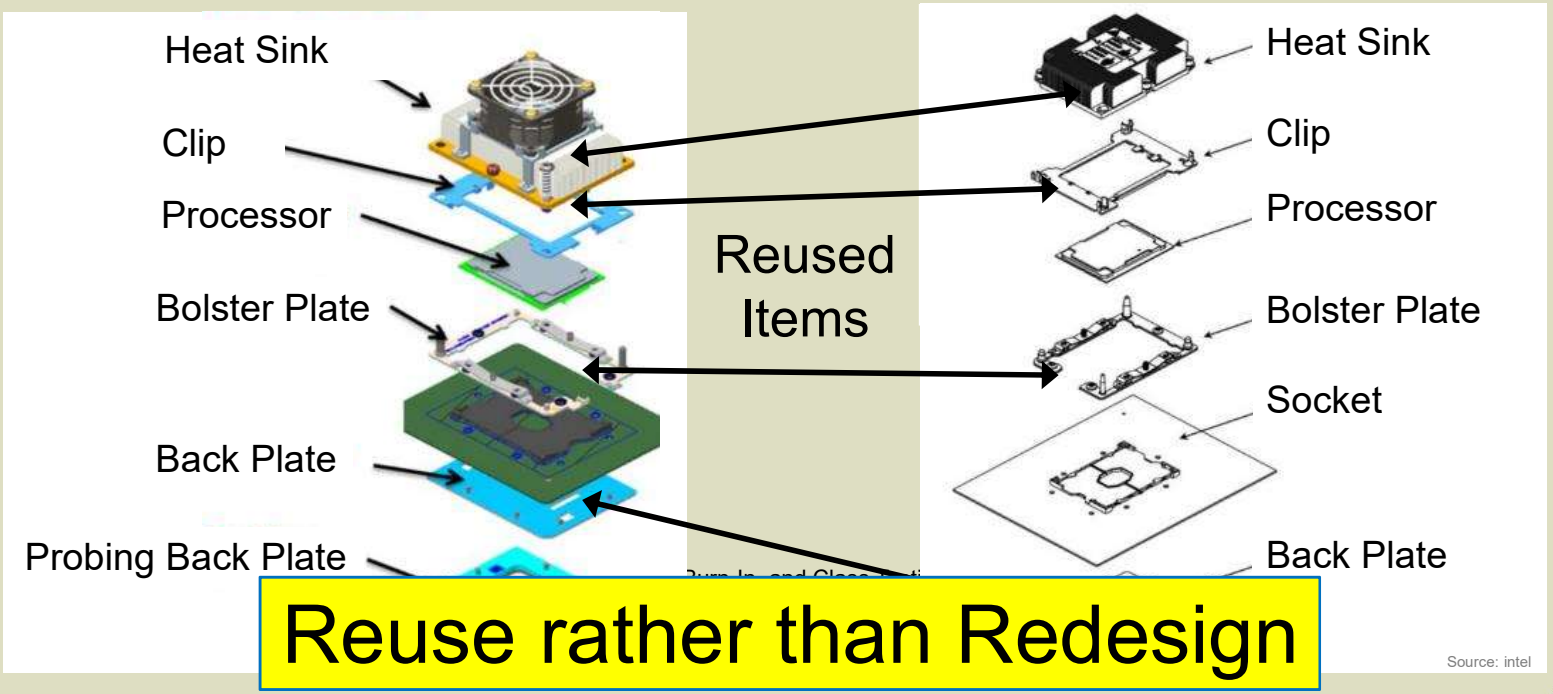

Source: intel

Purpose Built hardware to accomplish validation

Reuse Socket and Thermal Designs



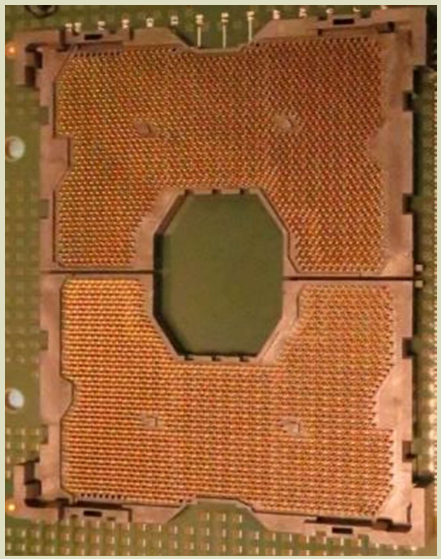
Reuse Socket and Thermal Designs



Reuse rather than Redesign

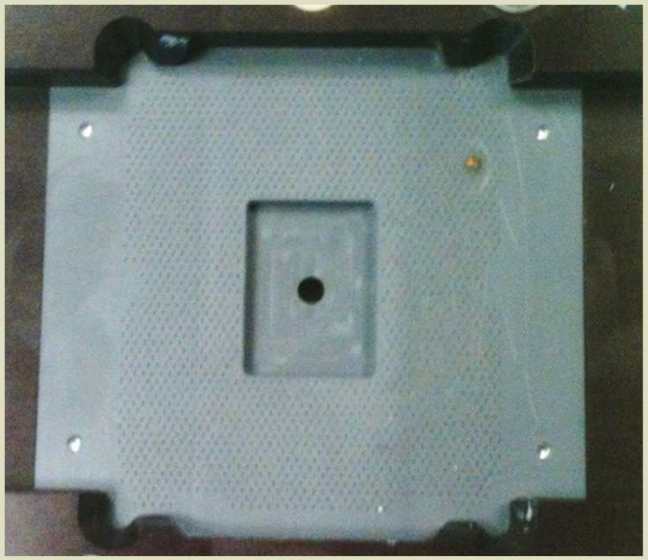
Source: intel

Typical Socket Types



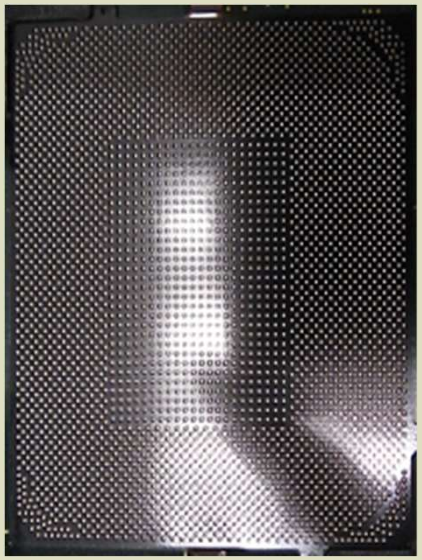
Source: intel

LGA



Source: intel

Spring Pin



Source: intel

Elastomer

Enable Modular Design

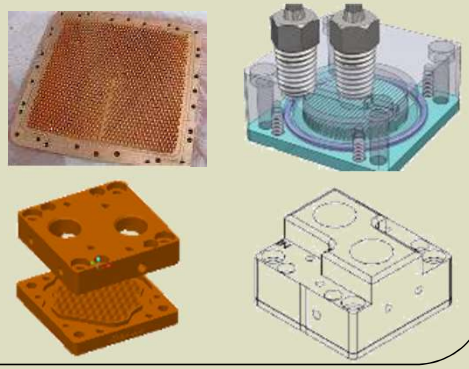
Solution Strategy: The methodology is to split up the design elements and standardize the interfaces. Modular design allows the modules within an assembly to be replaced without redesigning the assembly completely.

Benefit of modularization:

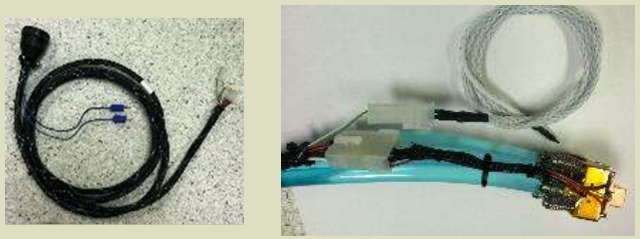
- Enable parallel work
- Eliminate waste by increasing reusability
- Reduce cost by reducing the design resource and new tools ordering
- Shorten time to market by simplifying design work to support 2x or 5x more silicon testing
- Accommodate future package derivatives

Enable Modular Design

Modular Cooling Block

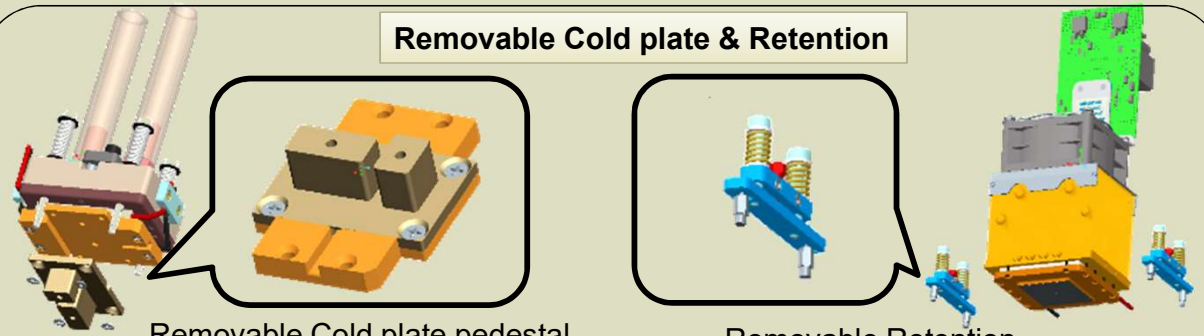


Standardized Quick Disconnect Harness



Reusable Main Harness

Removable Cold plate & Retention



Removable Cold plate pedestal

Removable Retention

TestConX™

Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy

141

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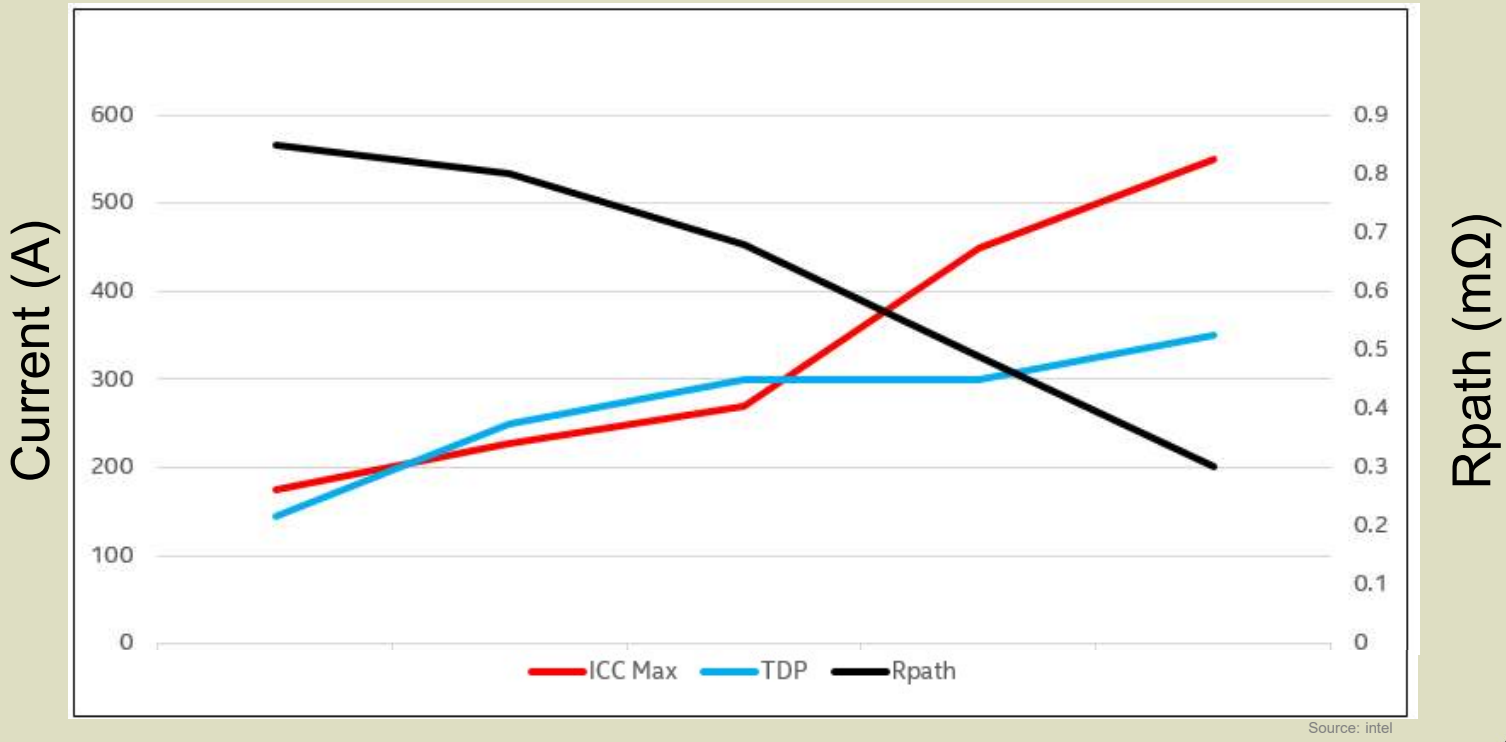
141

What Changed

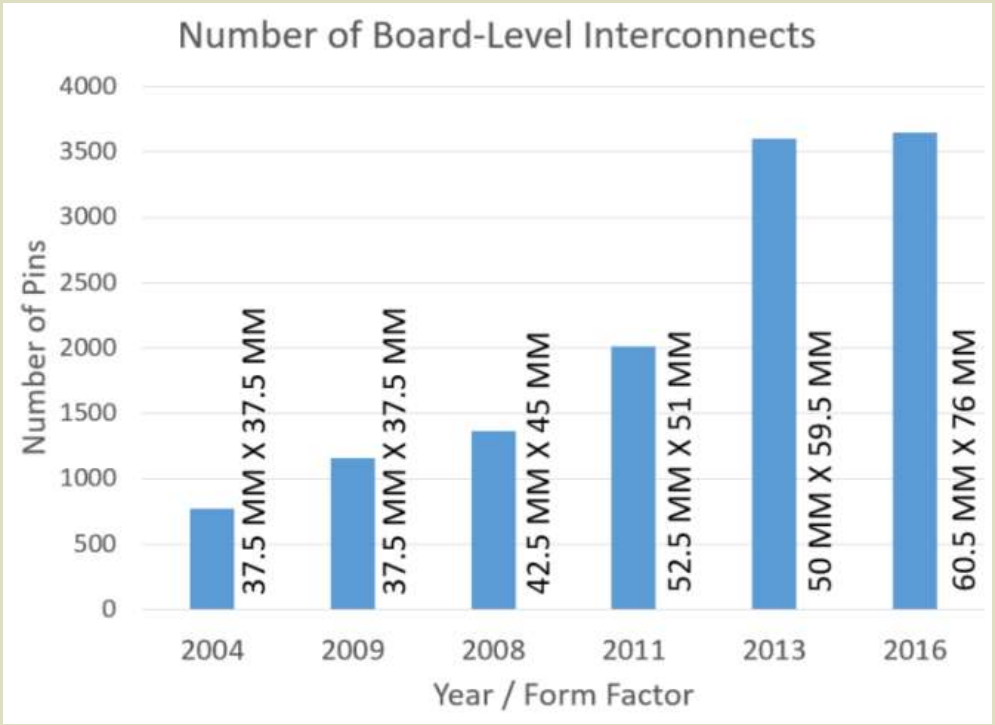
CHALLENGES CONFRONTING THE NEW SOLUTIONS

Trend: High Power, High Current, Low Rpath



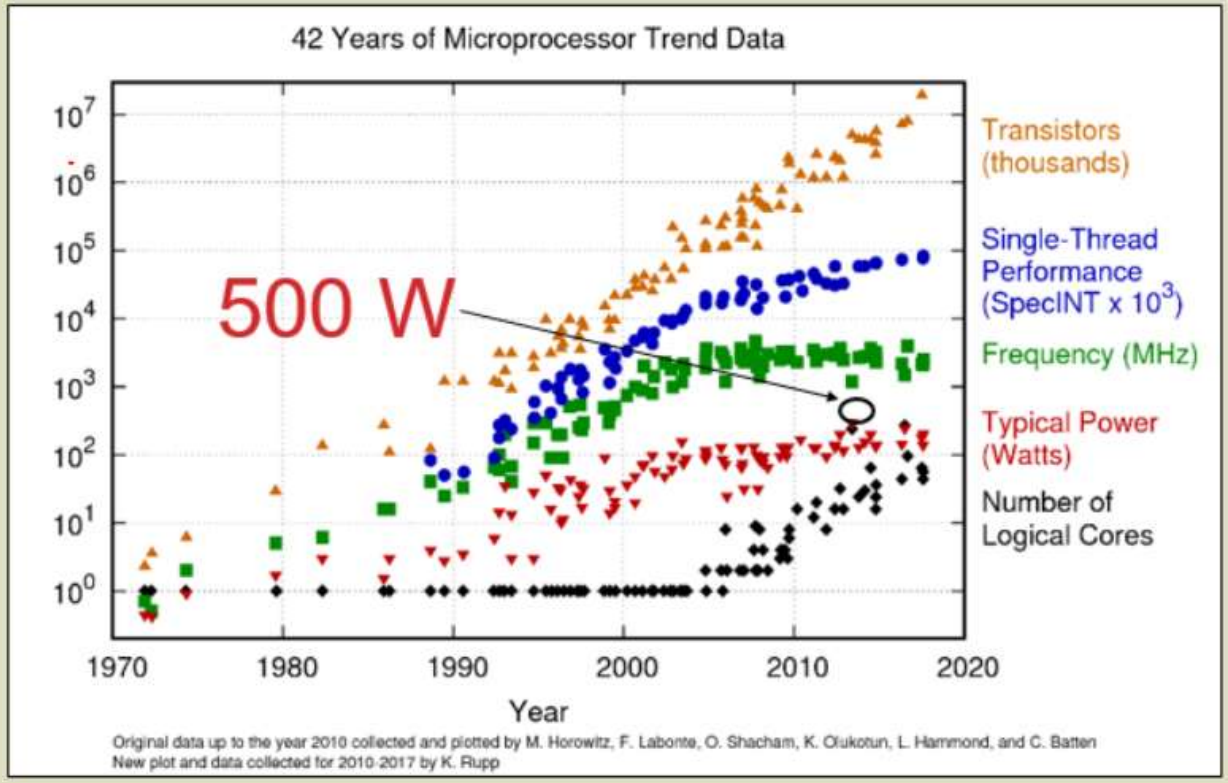
Source: intel

Chronological trend of Large Package Form Factor vs pin count



Source: ark.intel.com

High Power Products Challenge Cooling Technologies

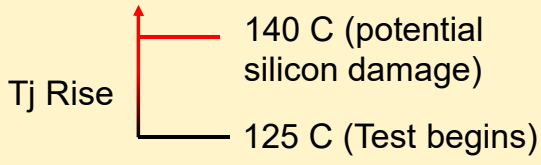


New Markets, Large Thermal Test Range

- ADAS products require broad operating environment (AEC-Q100 grade 2: Tj -40 C ~ 125 C) and long lifetime expectation, typically in the range of 15+ years.

Ambient Operating Temperature Range	Junction Temperature Range
–40° C to 105° C	–40° C to 125° C

- -40 C Tj means Tc should be much lower than -40 C which challenges the TT cooling capability
- 140 C is silicon safety temperature limit



- Condensation management is critical for -40 C test

Summary

- We have looked at how an expanding product portfolio and shrinking process have made legacy hardware methodologies obsolete for Post-Silicon Functional Validation
- The higher levels of integration, enabled by shrinking process, have demanded a shift in hardware strategies that support today's silicon products
- While HW strategies have become more efficient, the continuing trend of higher current, higher power, and larger packages have brought a new set of challenges which will be explored through case studies that follow.

Case Study

POWER MEASUREMENT AND CHALLENGES OF >340 A

Agenda

- The Importance of Power Measurement
- Ideal Solution
- Initial Strategy Recap
- Interposer Approach
- Trends and Challenges to >340 A
- Exploratory Solution
- Summary

Goal

Deliver Industry Leading Performance per Watt across the product portfolio

Goal

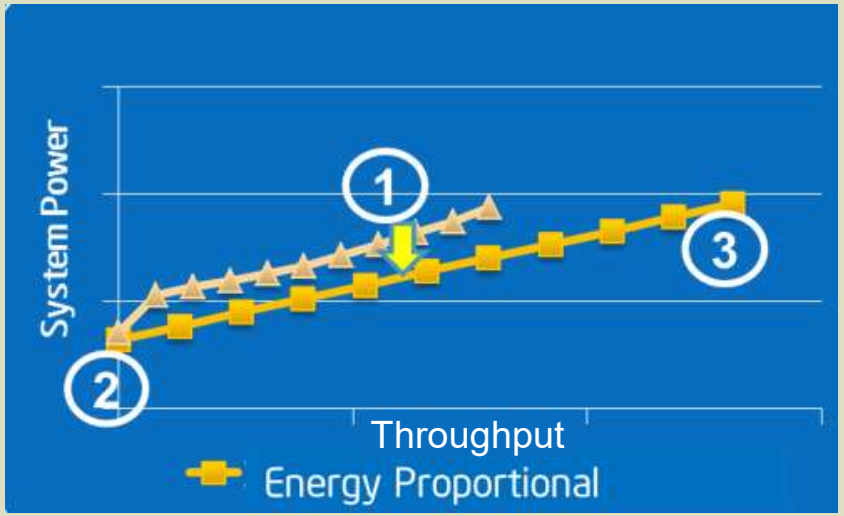
Deliver Industry Leading Performance per Watt across the product portfolio

Requires measuring component supply current from leakage to max TPD, a range of *single digit Amps* to *hundreds of Amps*

Power Measurement is Important

- Device characterization
- Tuning of component operating

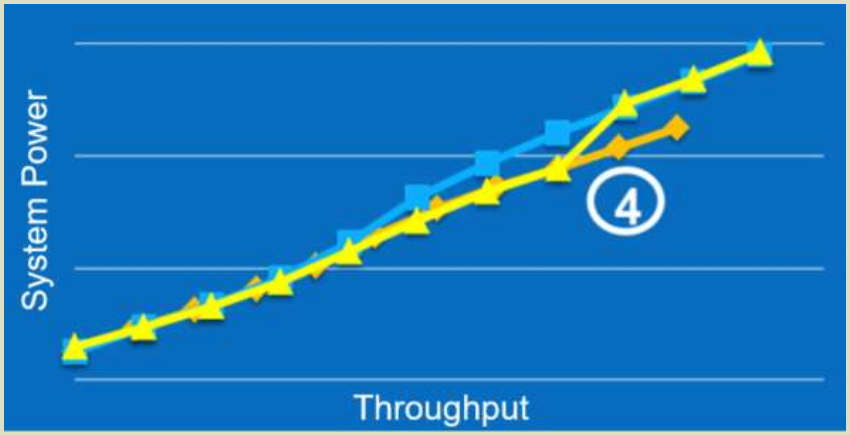
1. Shape loadline
2. Meet Idle power targets
3. Tune Turbo algorithm



Courtesy: Sundar Iyengar

Power Measurement is Important

- Tune loadline to align with platform power delivery design requirements

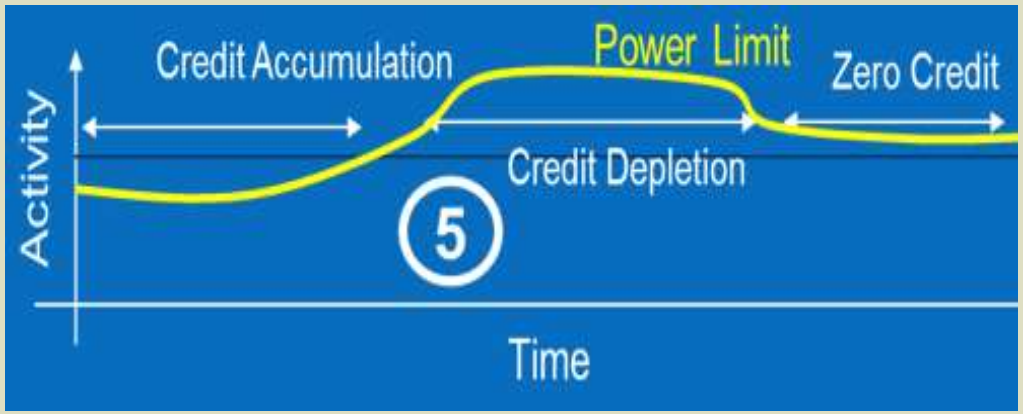


Courtesy: Sundar Iyengar

4. Meet loadline requirements

Power Measurement is Important

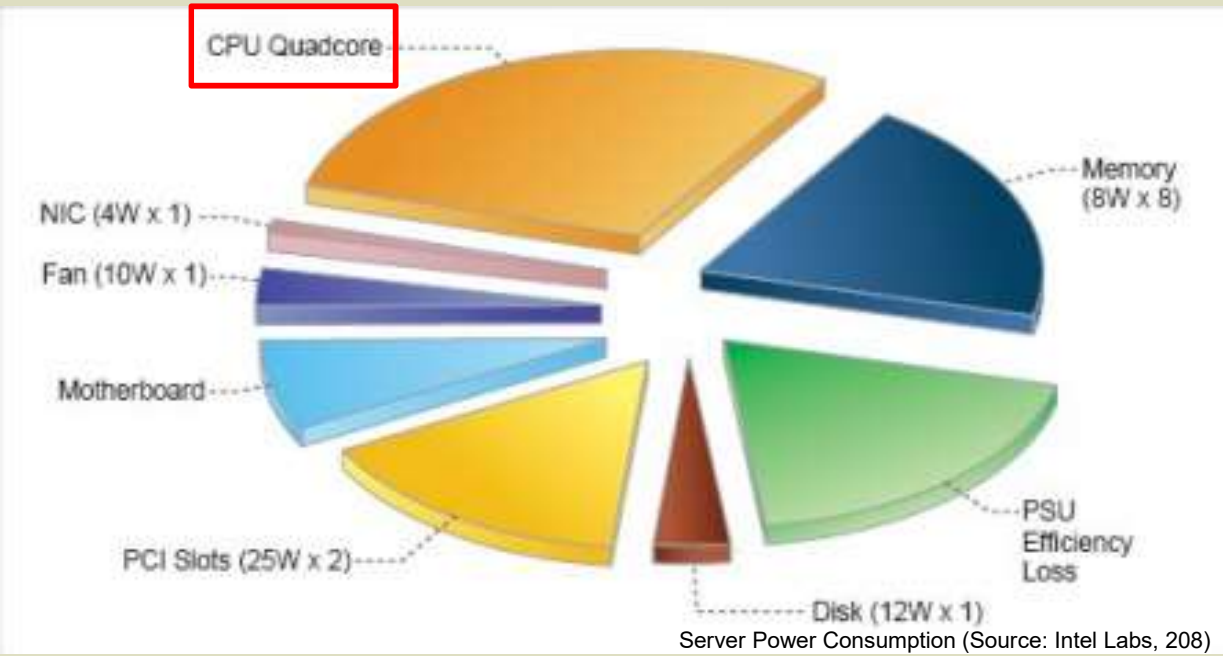
- Tune Running Average Power Limit (RAPL)



Courtesy: Sundar Iyengar

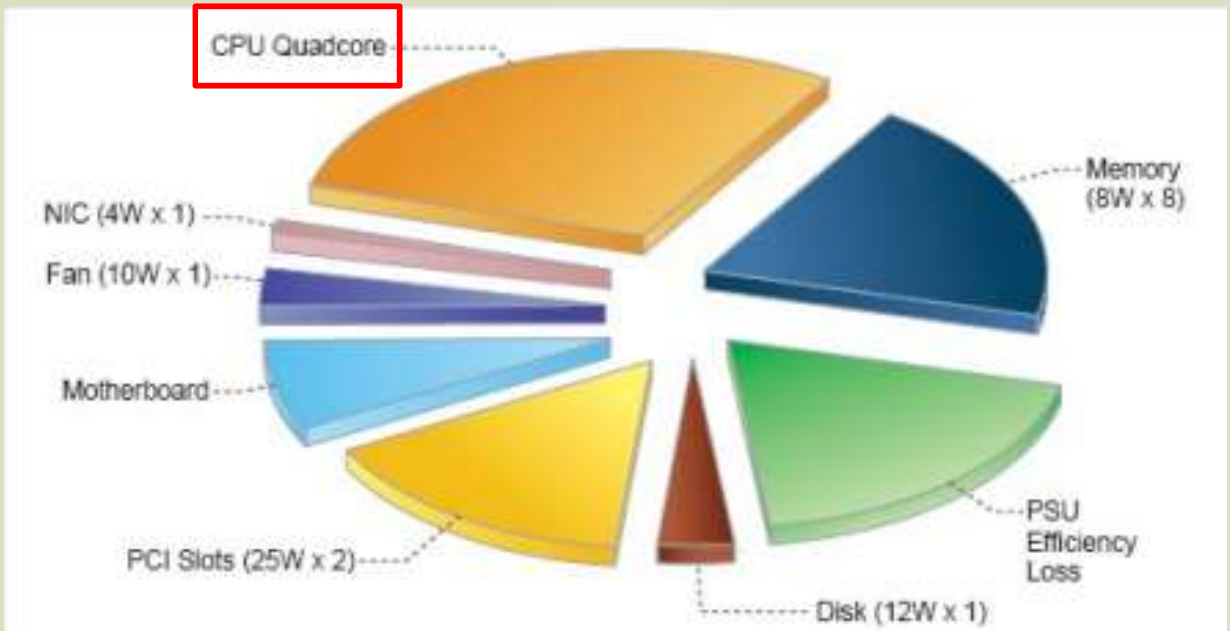
5. Tune RAPL algorithms

CPU Major Power Consumer



Server Power Consumption (Source: Intel Labs, 208)

CPU Major Power Consumer



Measuring CPU Power is Critical to Validation

Most Visible Impact

Source: Digital Trends

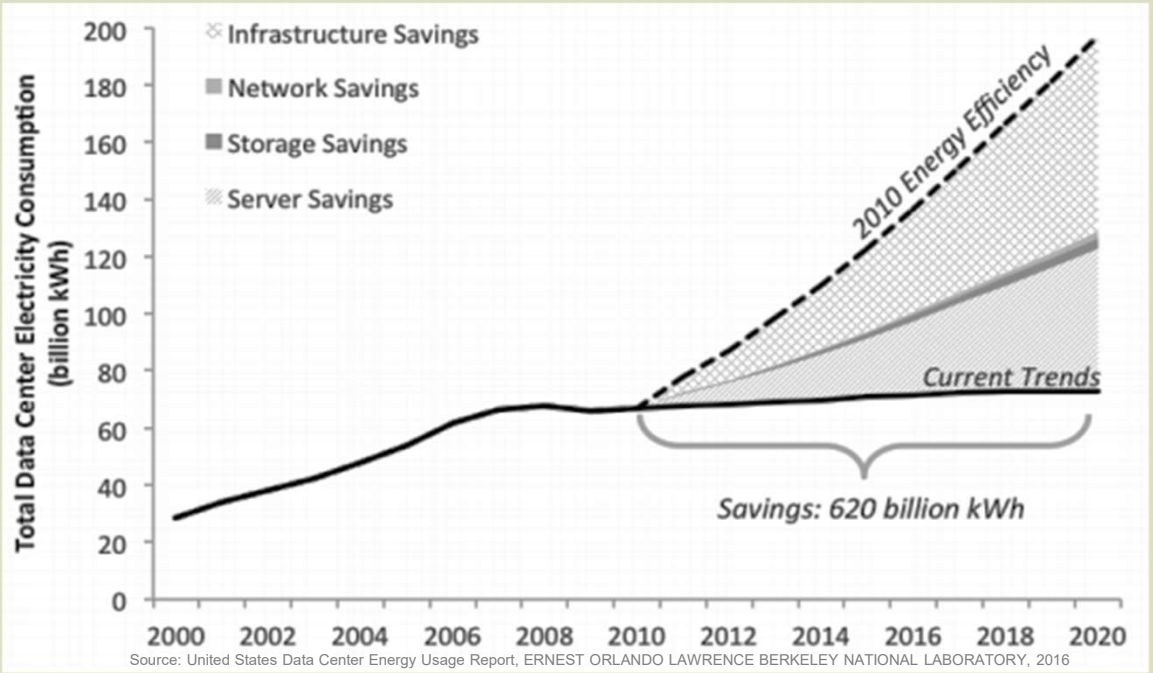
Laptop Battery Life

Most Visible Impact

Longer battery life contributes to better user experience

Laptop Battery Life

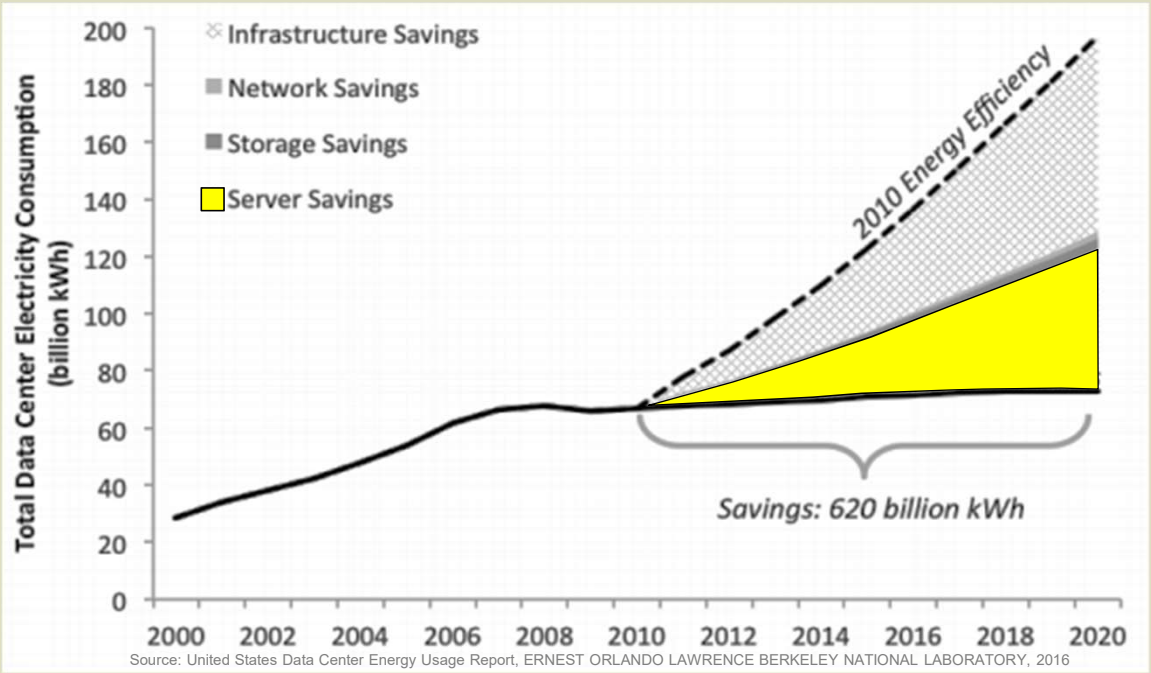
Enterprise Impact



Source: United States Data Center Energy Usage Report, ERNEST ORLANDO LAWRENCE BERKELEY NATIONAL LABORATORY, 2016

Data Center Electricity Consumption in Current Trends and 2010 Energy Efficiency Scenarios

Enterprise Impact



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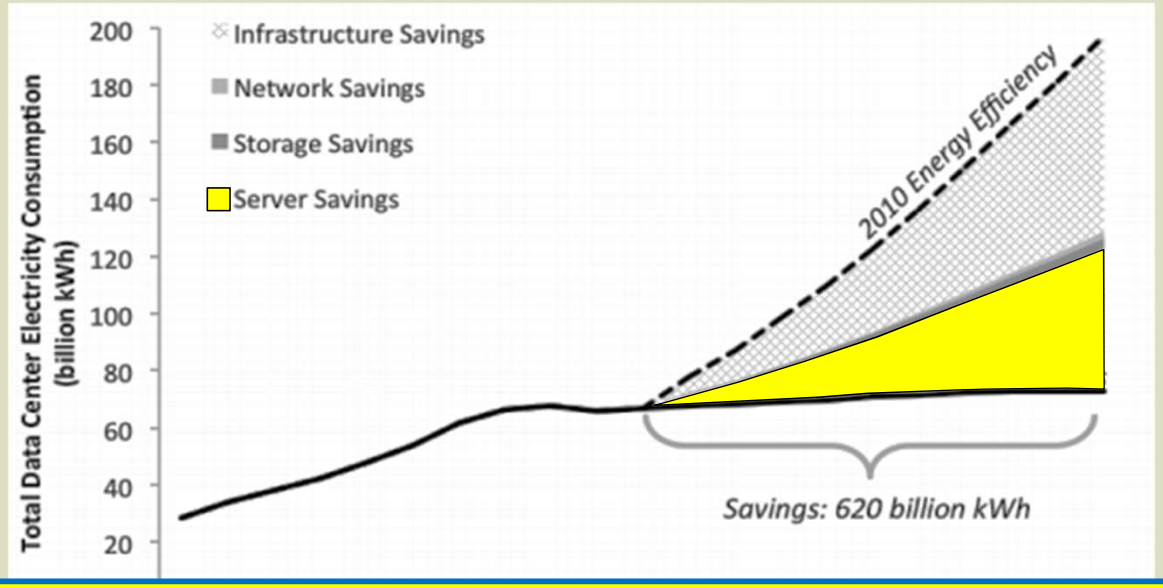
Data Center Electricity Consumption in Current Trends and 2010 Energy Efficiency Scenarios

Enterprise Impact



Lower energy consumption = lower operating costs

Data Center Electricity Consumption in Current Trends and 2010 Energy Efficiency Scenarios

Power Measurement Ideal Hardware Solution

- Fully integrated into the component power delivery solution of a Reference Platform (RP)
- Require no special components added to a RP
- Accuracy of 1% or better 0 A to 100's A
- Zero added error from 0 C to 100 C
- No added mechanical complexity
- Adds no additional system BOM cost

Source: Intel

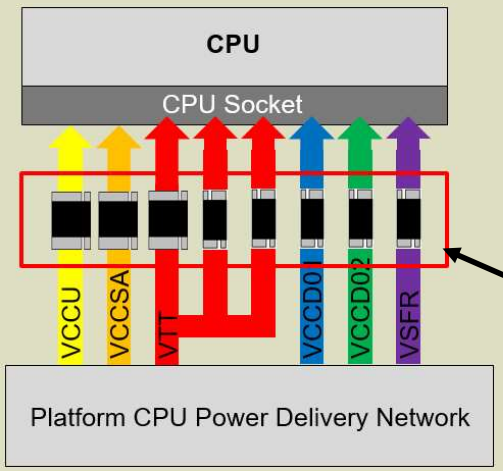
Reference Platform

Synthetic Platform Recap

- Build platform for power measurement
  - Re-engineer power delivery solution
  - Insert sense resistors, tune layout

Source: Intel

Synthetic Platforms

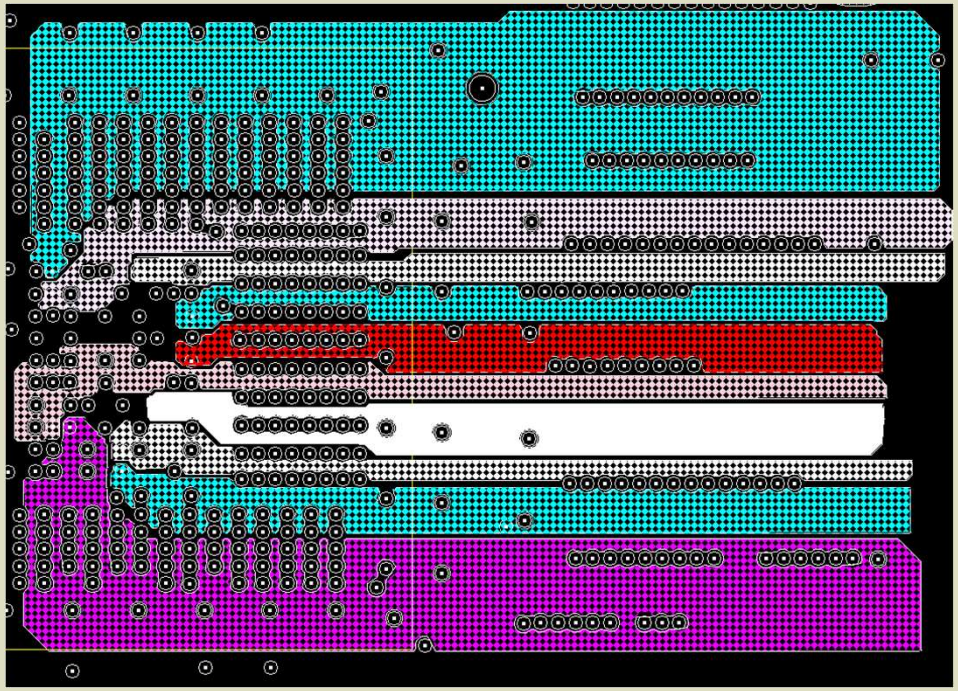


4-pin sense resistors
Inserted into power
delivery network

Resulting Power Delivery Design

Power plane cuts for Synthetic Platform design

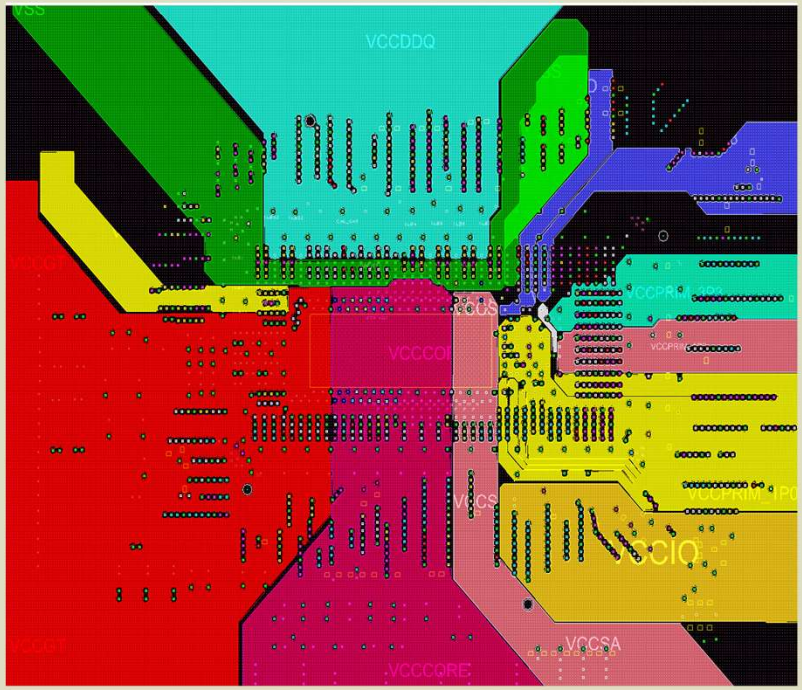
Design does not meet all power delivery specifications for R-path and impedance



Source: Intel

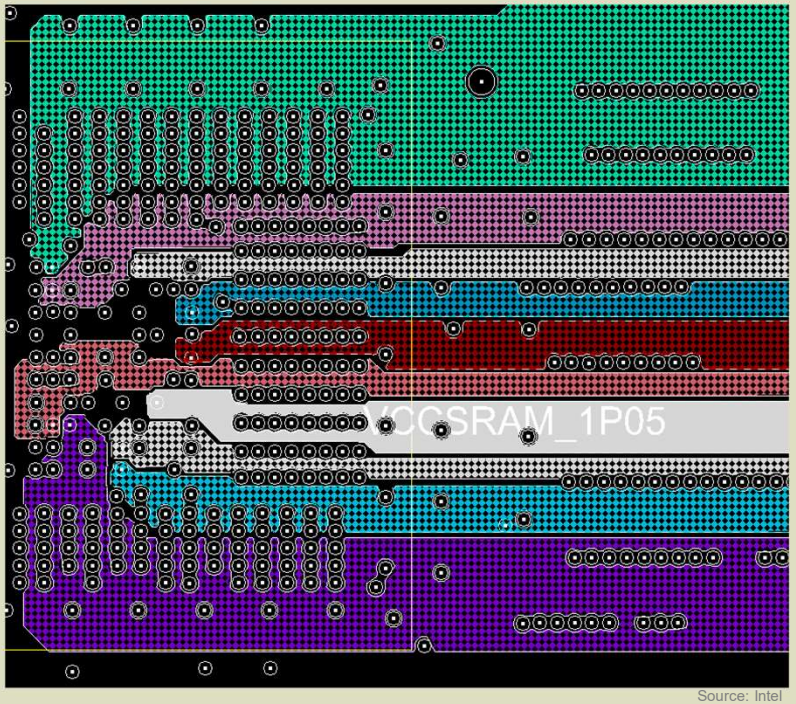
Synthetic Platform Power Shapes

Power Delivery Design Differences



Source: Intel

Reference Platform Power Shapes



Source: Intel

Synthetic Platform Power Shapes

Result

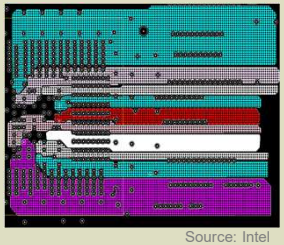

Torch wielding mob from Frankenstein

No one was happy…

Result

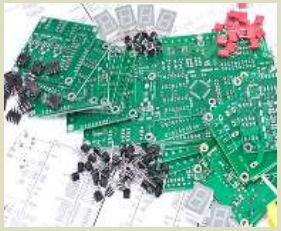
- Cost too much
- Fully redundant product development and manufacturing teams

Architecture and Design



Source: Intel

Layout



Procure Materials

Source: Intel

Assembly Integration & Test

Deploy to Customer

Result

- Cost too much
- Fully redundant product development and manufacturing teams
- Customer not happy with lack of correlation to real systems

Source: Intel

Reference Platform (RP)

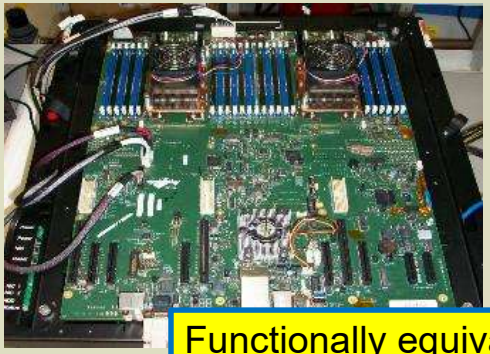
≠

Source: Intel

Synthetic Platforms

Result

- Cost too much
- Fully redundant product development and manufacturing teams
- Customer not happy with lack of correlation to real systems



≠

Functionally equivalent but not identical electrical or BIOS

Reference Platform (RP) **Synthetic Platforms**

Current Measurement Options

Criteria (High->Low Priority)	RP with VR I-Mon	Synthetic Platform (Power Plane Splits)	Power Interposer
Cost	Excellent	High	Low
Sub-Rail Measurement	No	Yes	Yes
Leakage Current Error	Poor	Good	Good
Max TDP Current Error	Good	Good	Good
Power Integrity Impact	None	Low	Med
Signal Integrity Impact	None	Low	Med
Test Correlation	Good	Poor	Good
Mechanical complexity	None	Low	High
Customer Usability	Good	Good	Good
Scaling with Current	Excellent	Good	Med

Grading Relative Reference Platform

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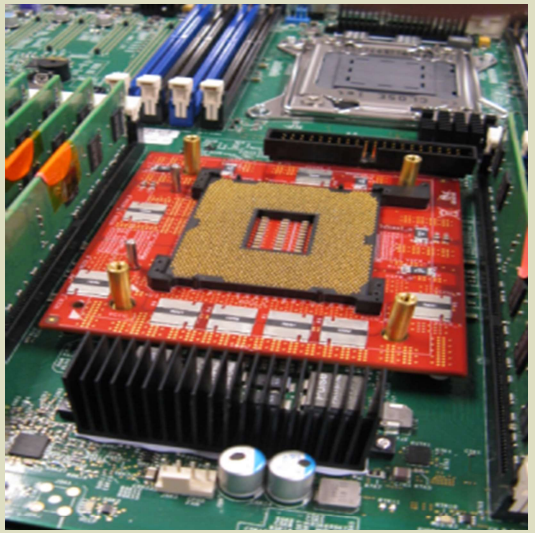
Power Interposer became the new path of investigation

Grading Relative Reference Platform

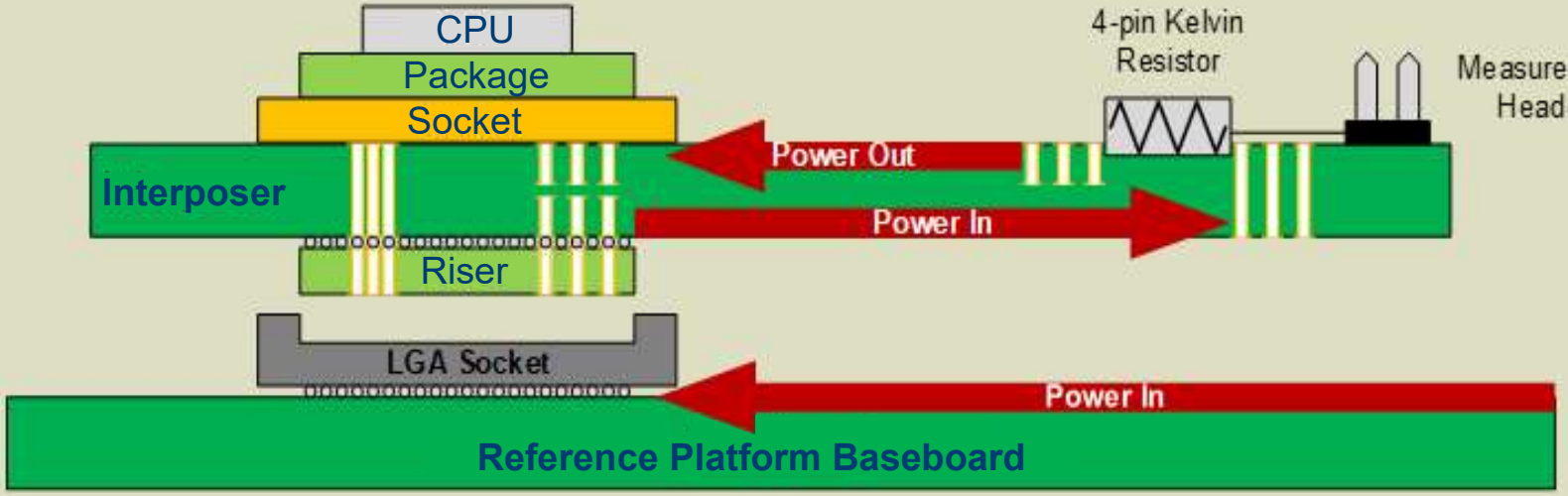
Interposer Option for Current Measurement

- Overall lower cost
- Easier to design than full system
- Met customer key criteria
  - Low error from 0A-200A
  - Plug and play in Reference Platform
  - No special accommodations needed



Source: Intel

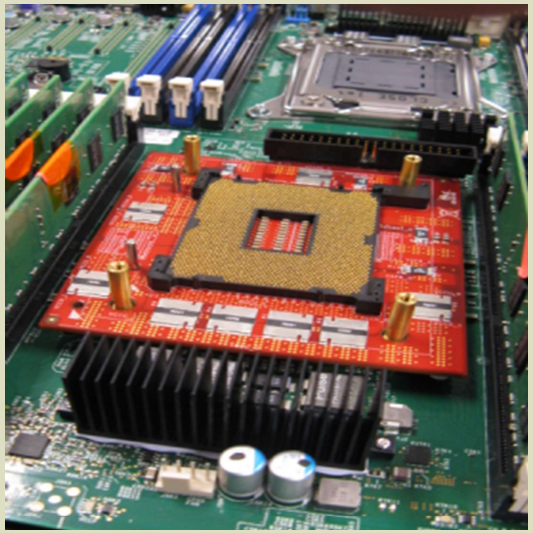
Power Measurement Interposer Current Flow



Source: Intel

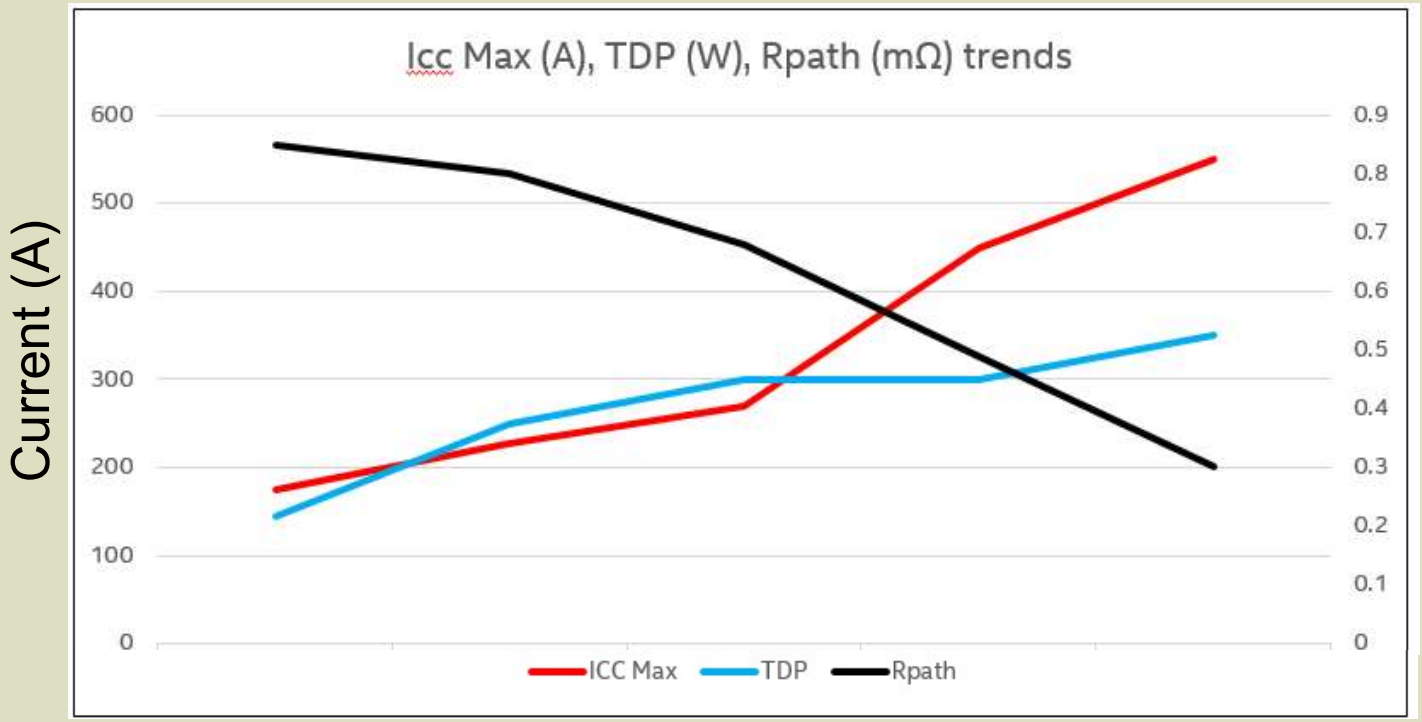
Interposer for Current Measurement

- Overall lower cost
- Easier to design than full system
- Met customer key criteria
  - Low error from 0A-200A
  - Plug and play in Reference Platform
  - No special accommodations needed
- However, not without negative impacts
  - Power and signal integrity
  - Mechanical complexity



Source: Intel

Trend: High Power, High Current, Low Rpath



Source: Intel

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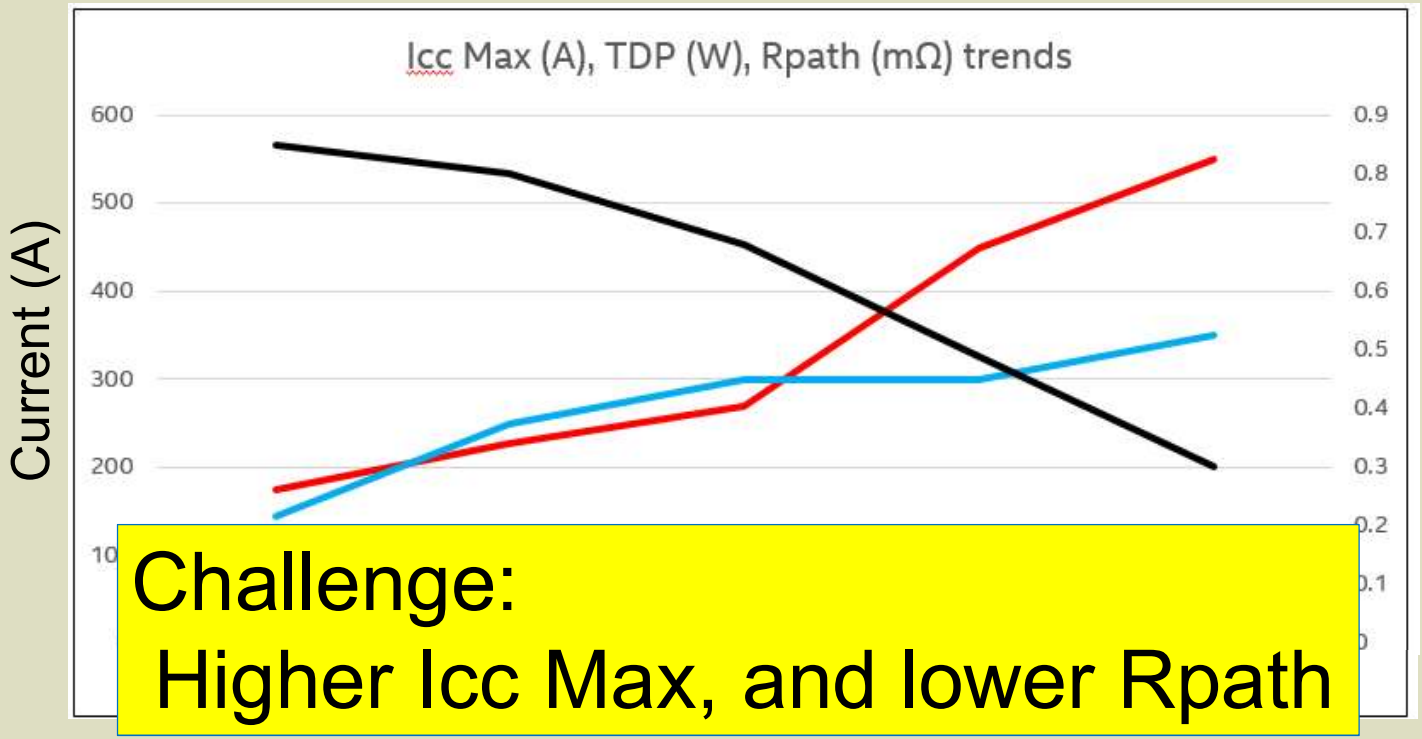
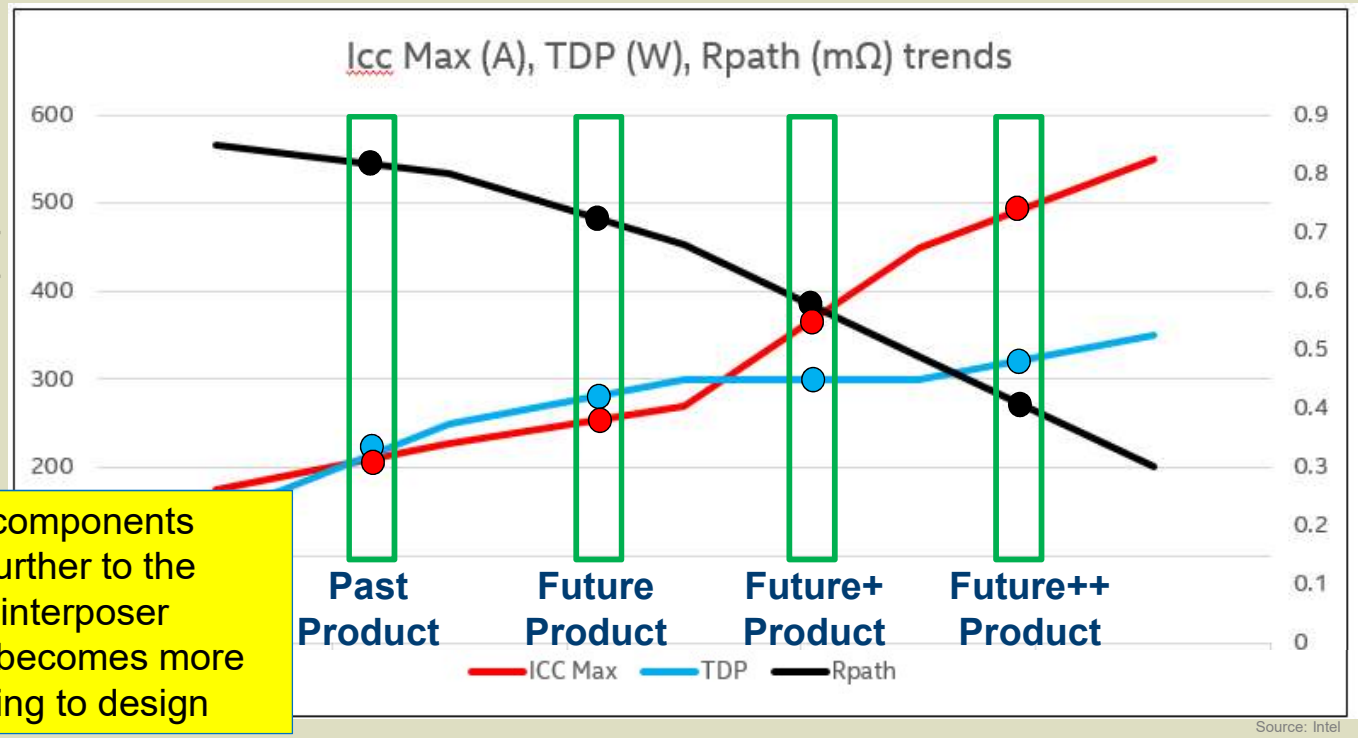


Challenge:
Higher Icc Max, and lower Rpath

Trend: High Power, High Current, Low Rpath



As new components appear further to the right, an interposer solution becomes more challenging to design

DDR Memory Trend

Standard	Bus Clock (MHz)	Data Rate (MT/s)
DDR	133-200	266-400
DDR2	266-400	533-800
DDR3	533-800	1066-1600
DDR4	1066-1600	2133-3200
DDR5	1600-3200	3200-6400

DDR Memory Trend

Standard	Bus Clock (MHz)	Data Rate (MT/s)
DDR	133-200	266-400
DDR2	266-400	533-800
DDR3	533-800	1066-1600

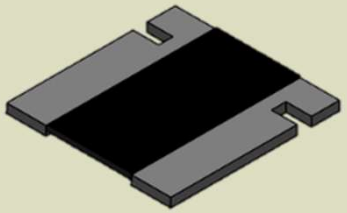
Challenge:

- Higher frequency single ended signals, such as DDR, are more sensitive to vertical coupling
- DIMMs moving closer to CPU to shorten routing length results in less area for a power interposer

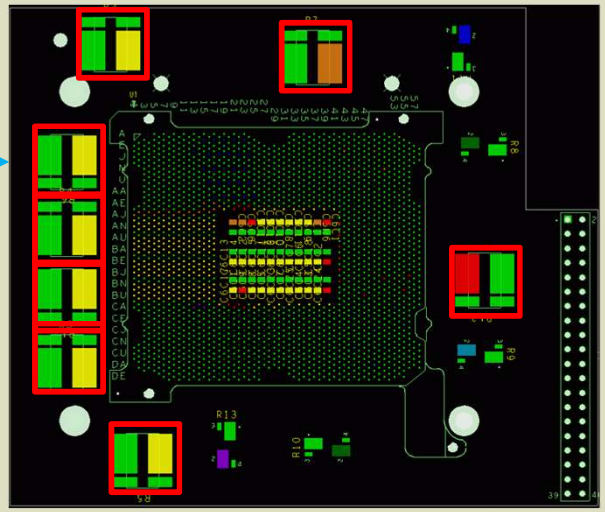
Interposer Challenges due to Trends

- ICCmax Increasing
  - Requires more sense resistors -> more space
  - Require more copper layers to carry more current

Generally using one per every 33 A of ICC -> ~10 for 340 A ICC Max



4-pin Sense Resistor
0.001Ω, 3W
0.370” x 0.360”



Source: Intel

Interposer Challenges due to Trends

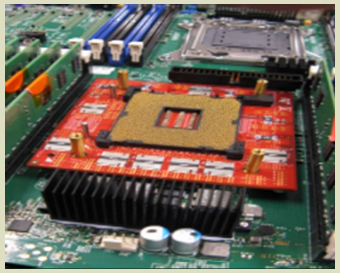
- Dropping Rpath – greater impact to Power Integrity
  - Can never fully compensate across full AC response
  - More copper layers needed to lower Rpath

More copper layers -> thicker Printed Circuit Board (PCB) which could lead to using more expensive manufacturing such as moving from Type3 to Type4 PCB

Source: Intel

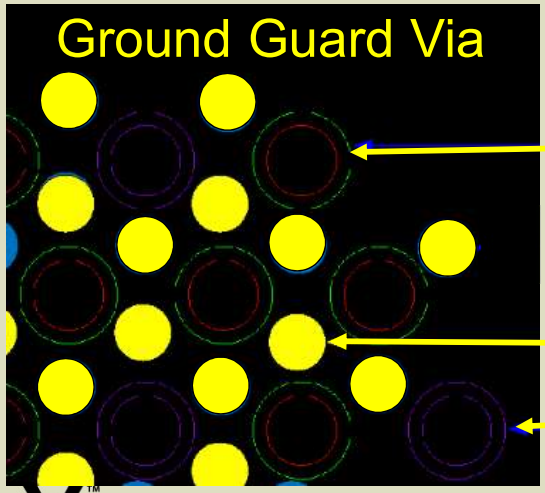
Interposer Challenges due to Trends

- Number and speed of I/O increasing
  - Leading to tighter pitch -> more vertical coupling
  - Higher speed I/O -> more sensitivity to coupling

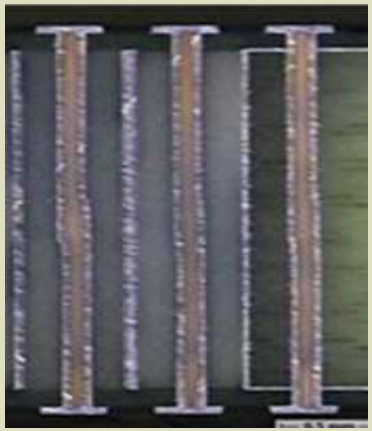


Source: Intel

Critical to reduce vertical coupling and moving from inexpensive guard via to coax via



Source: Intel

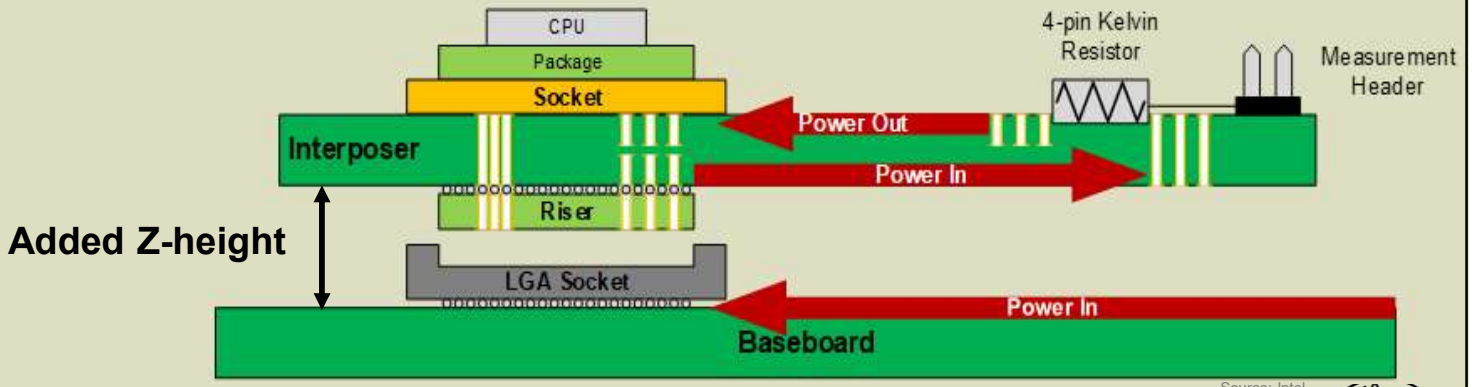


Source: Intel

Coax Via

Z-Height

- Minimizing added height is a challenge and trade off of area vs height vs signal integrity impact
  - As Z↑, *interposer area increases*, *signal coupling increases*
  - As Z↓, *interposer area decreases, signal coupling decreases*

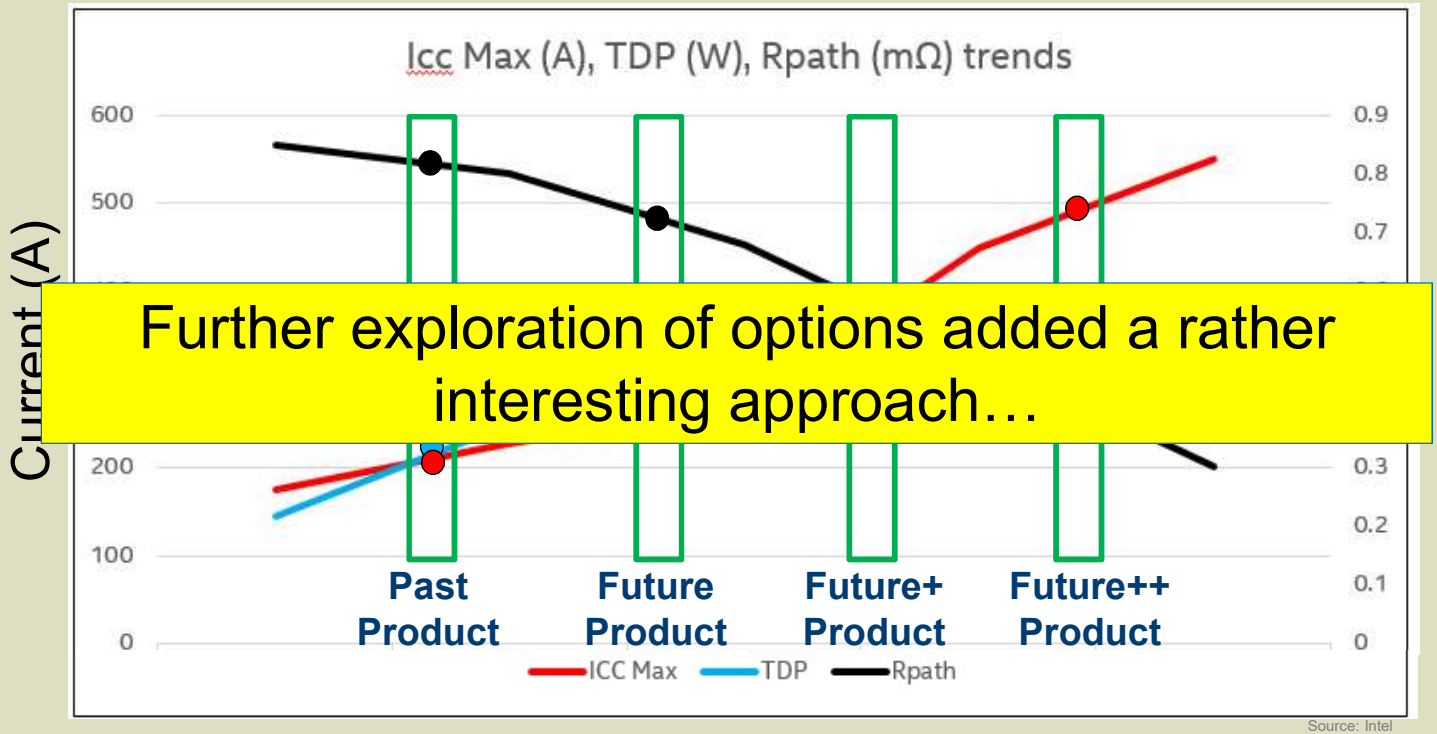


Scaling Power Interposer to beyond 340A

- With higher current will come:
  - Lower R-path -> more sensitivity to power routing
  - Higher speed I/O -> more sensitivity to vertical coupling
  - DIMMs placed as close to the CPU as possible -> limiting interposer growth area
  - More voltage regulator phases will be needed -> cutting off interposer growth area formally available

Another approach is needed for measuring currents beyond 340A with high accuracy (+/-0.5%)

Trend: High Power, High Current, Low Rpath



Further exploration of options added a rather interesting approach…

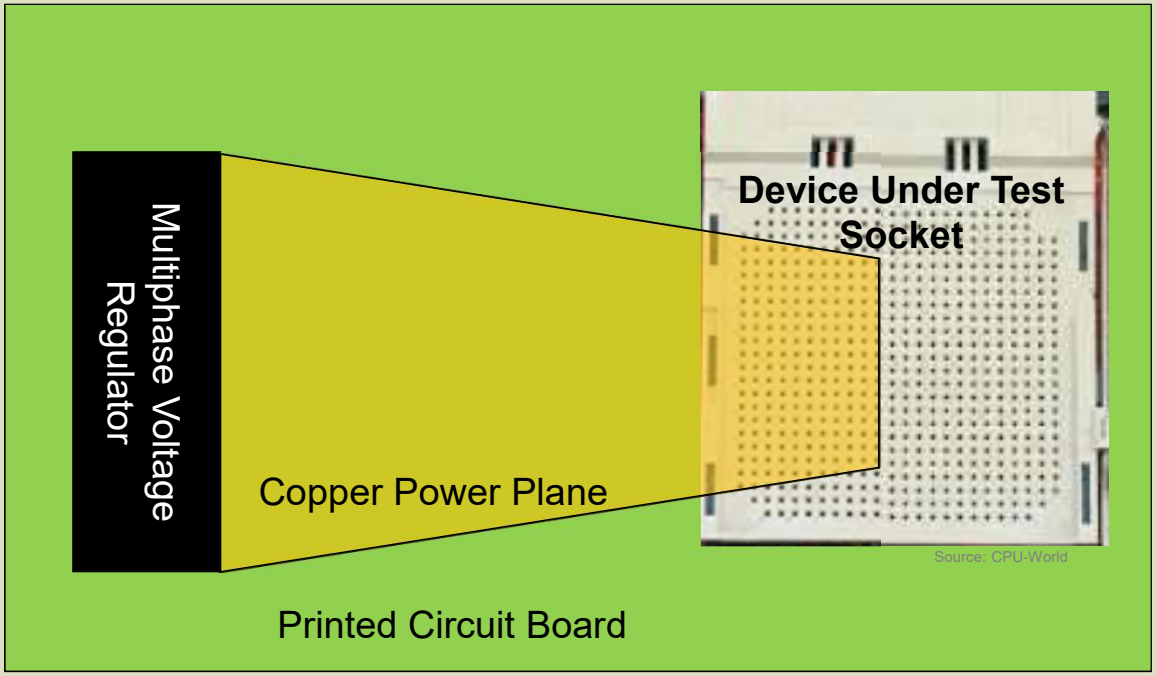
Power Measurement

EXPLORATORY SOLUTION
UTILIZE COPPER SHAPE AS SENSE

Ideal Scenario

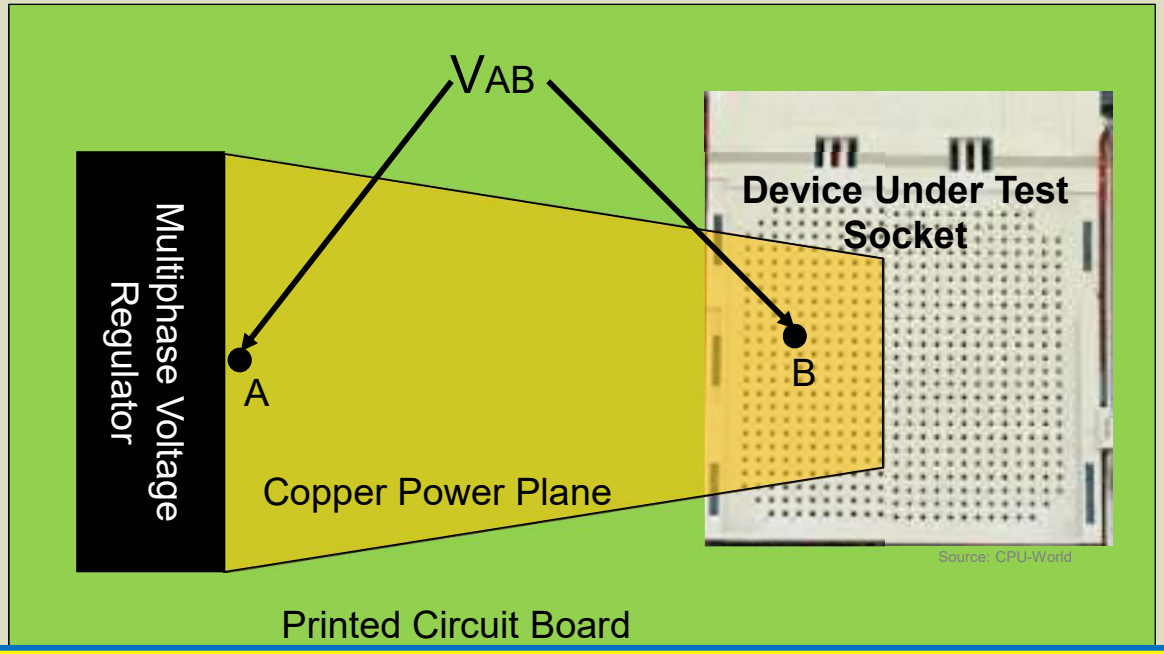
Measure current without adding additional components or complexity to the system

Using Power Plane



2 oz Cu general rule has 0.25 Ω per square

Using Power Plane as "Sense Resistor"



2 oz Cu general rule has 0.25 Ω per square

Ohm's Law applies: there is a voltage difference across the copper power plane induced by the current flow from the voltage Regulator to the Device Under Test

Copper Shape as Sense Resistor Results

- Successfully tested to 350 A (power supply limited)
- High accuracy results can be obtained
  - Error of <1% from 0 A to 350 A
- Challenges exit
  - Compensation for copper's change in resistivity over temperature
    - Left as an exercise for the curious…

Current Measurement Options

Criteria (High->Low Priority)	RP with VR I-Mon	Synthetic Platform (Power Plane Splits)	Power Interposer	Copper Shape
Cost	Excellent	High	Med	Very Low
Sub-Rail Measurement	No	Yes	Yes	No
Leakage Current Error	Poor	Good	Good	Good
Max TDP Current Error	Good	Good	Good	Good
Power Integrity Impact	None	Low	Med	None
Signal Integrity Impact	None	Low	Med	None
Test Correlation	Good	Poor	Good	Excellent
Mechanical complexity	None	Low	High	None
Customer Usability	Good	Good	Good	Good
Scaling with Current	Excellent	Good	Med	Excellent

Grading Relative Reference Platform

Summary

- Higher integration and frequency has led to a rise in ICC and corresponding drop in Rpath
- While the power interposer approach has been proven to work at currents exceeding 300 A, there are significant pressures leading to challenges and difficulties continuing with this strategy
- Less intrusive solutions are needed that can provide high accuracy from 0 A to ICC Max

Case Study

SOCKETING LARGE BGA PACKAGES

Socket Challenges in Post-Silicon Validation for Large BGA

- Agenda
  - Socket Introduction
  - Case Study:
    - Scope
    - Case Study: 1st Gen Intel Xeon Phi
    - Physics and control of package warpage
    - Finite Element Analysis to analyze socket pin deflection including large package warpage
    - What can the socket retention designer do to mitigate socket connectivity risk (sensitivity studies)

Large BGA challenges in Post-Silicon Validation

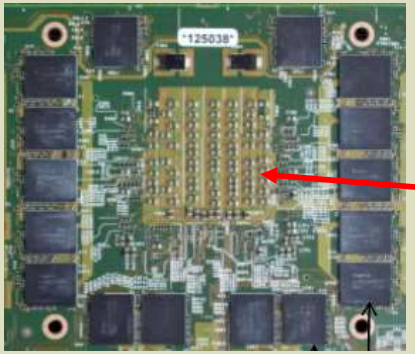
- Large number of pins (>3000) require large socket actuation forces
- Large package form factors (>60 mm X 60 mm) and large die cause significant end-of-assembly package warpage
- Stiff packages due to thick substrates, presence of an Integrated Heat Spreader (IHS), or stiffeners cause packages to be extremely difficult to flatten with socket retention loads
- Warped packages lead to critical pins at risk of receiving inadequate stroke
  - Packages go through temperature cycles (from sub-zero C to over 100 C) during post-silicon validation testing and change shape

Scope of the Problem in Case Study

- Failure mode of interest: Low level contact resistance (LLCR)
- Effect: System instability during post-silicon validation
- Form factor: Large package
- Pin: BGA
- Socket: Elastomer

Drivers to LLCR Risk

- Large package warpage
  - No accurate Daisy Chain Test Vehicle (DCTV) to mimic package warpage
  - Supplier package warpage may be exceeding spec without warning
- Tiny keep out zone (KOZ) on PCB
  - Very little to no area allowed on the board (primary and secondary side) due to densely populated components needed for power delivery and integrity
  - No touch-down area provided for robust structural support and flattening the board



Densely populated components on secondary of board may limit real estate for backing plate touch-down

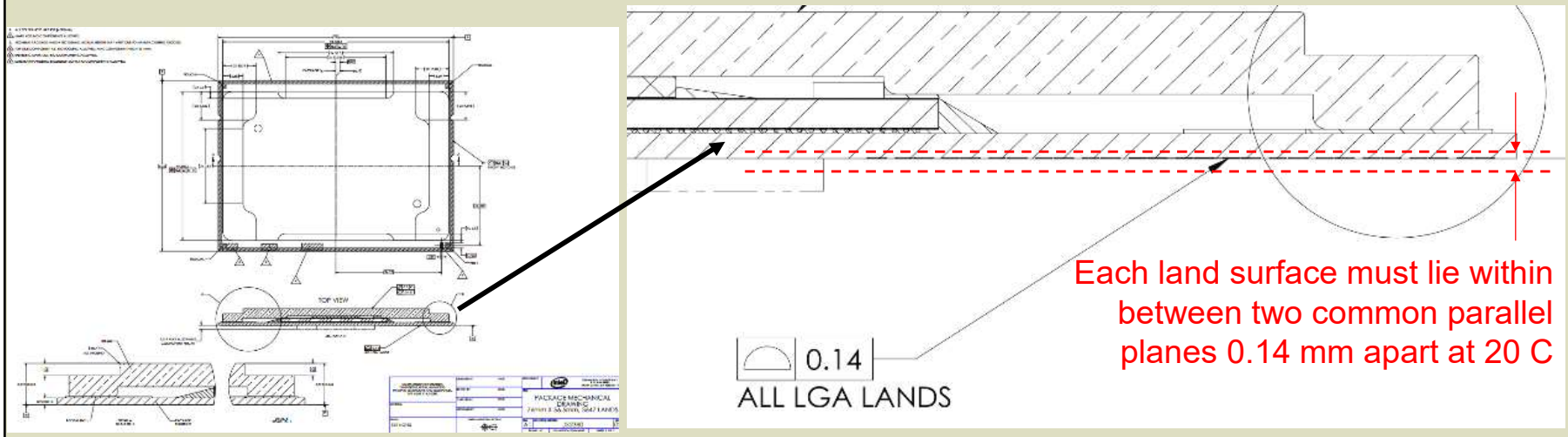
What's the current Best Known Method (BKM)?

- BKM for socket retention design
  - Assumes package is initially flat (both in modeling and in most daisy chain test vehicles)
  - Modeling does not compute pin deflection
  - Metric:
    - Minimize board deflection under retention load FEA modeling
- BKM is good for >95% of our products; but may not be good enough for products with substantial warpage risk
- Need to use better methods to quickly risk assess using FEA
  - Incorporate large package warpage
  - Compute the actual pin force distribution in the BGA to identify the highest risks for LLCR

Interpreting Warpage in Package Drawings: Geometric Dimensioning and Tolerancing according to ASME Y14.5

- All package drawings are controlled by Y14.5 standard
- Spec is at 20 C
  - Parts are inspected and screened at 20 C, not room temperature
- Flatness
  - "…is a condition of a surface… having all elements in one plane… tolerance zone defined by two parallel planes within which surface… must lie"
- Coplanarity
  - "…is the condition of two or more surfaces having all elements in one plane…may be used where it is desired to treat two or more surfaces as a single interrupted or noncontinuous surface…similar to flatness"
- There is a coplanarity spec for every BGA for each package drawing
- Note that there is no single "standardized" coplanarity value in industry
- BGA coplanarity spec is usually optimized for SMT (soldered down) applications (high volume), not so optimized for socketed post-silicon validation testing (low volume)

Example: Interpretation of Package Coplanarity



Sources:

- intel.com
- Geometric Dimensioning and Tolerancing according to ASME Y14.5 2009 Standard

Simplest Case: Bi-Material Warpage Driven by CTE Mismatch and Temperature Change

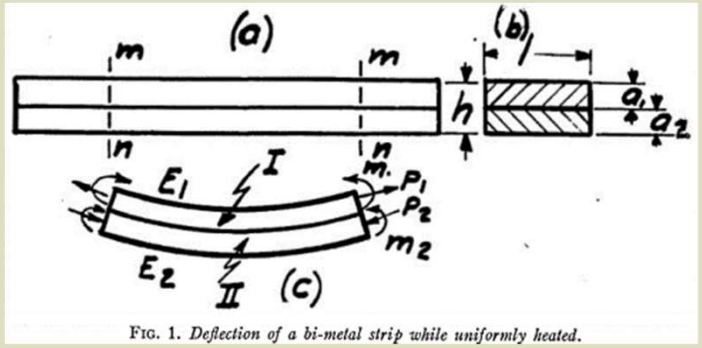


FIG. 1. *Deflection of a bi-metal strip while uniformly heated.*

Salient Features

- Shape and magnitude of warpage can be modeled
- Warpage scales
  - Linearly as CTE mismatch
  - Linearly as temp change
  - ~Inversely as the flexural rigidity
  - Nonlinearly as size

Warpage

Total length

$$\delta = \frac{l^2}{8\rho}$$

Radius of curvature

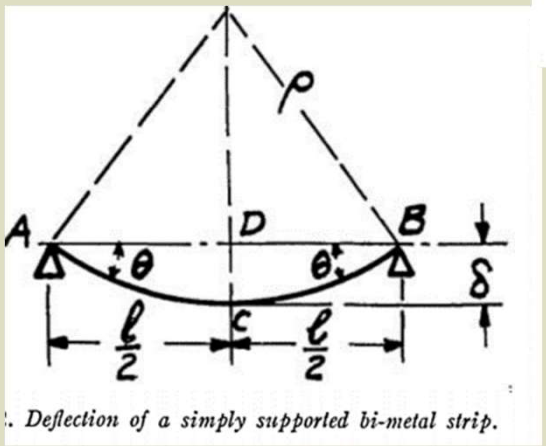
Coefficient of thermal expansion (CTE) mismatch

Temperature change

Radius of curvature

$$\frac{1}{\rho} = \frac{(a_2 - a_1)(t - t_0)}{\frac{h}{2} + \frac{2(E_1 I_1 + E_2 I_2)}{h}\left(\frac{1}{E_1 a_1} + \frac{1}{E_2 a_2}\right)}$$

Flexural rigidity



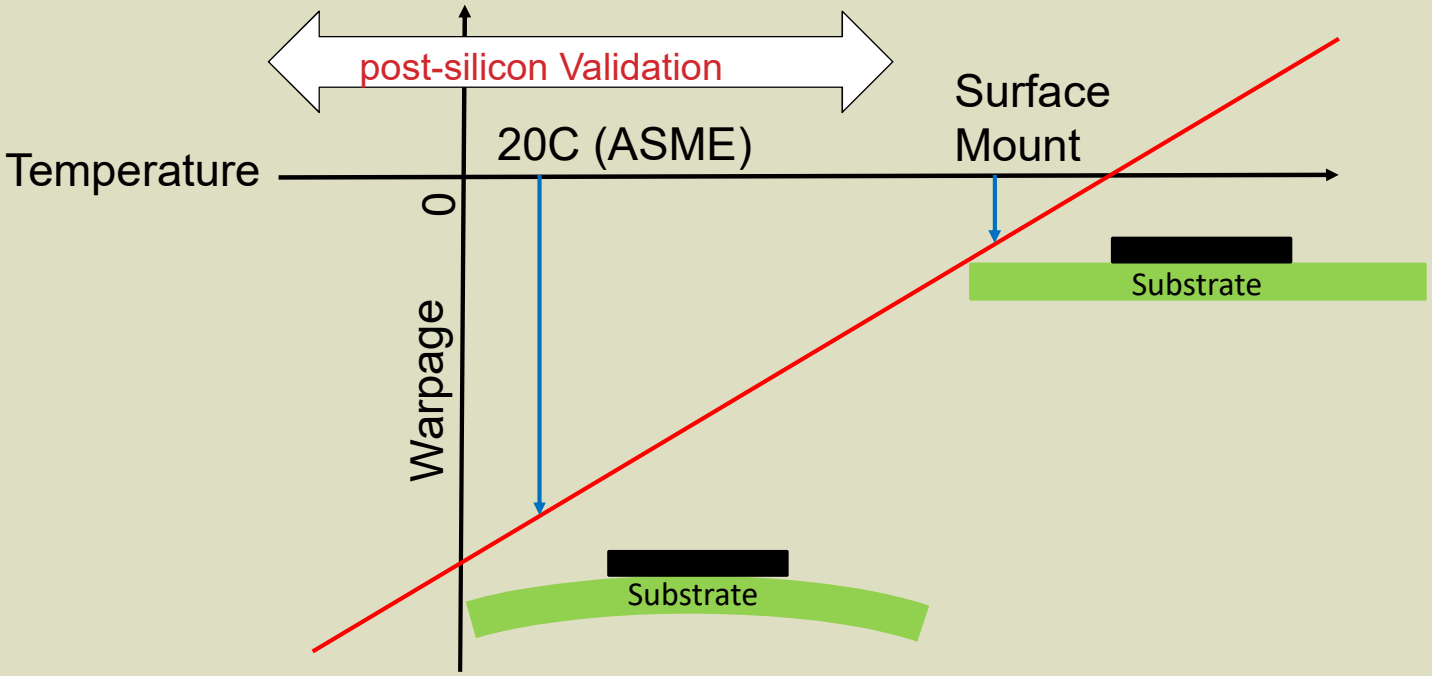
. *Deflection of a simply supported bi-metal strip.*

Source: Timoshenko, 1925

Origins of Package Warpage

- Flip chip package assembly process
  - Silicon is attached to the substrate at elevated temperatures followed by a cool down
  - Due to CTE mismatch and temperature changes, the package warps
  - A much more complicated scenario compared to the classic thermostat
- Package will be optimized to be flat at solder reflow temperature and warped at room temperature
- Can we accurately predict package warpage?
  - Definitely--only if we have accurate geometry, good material properties, knowledge of the manufacturing process
- Lack of predictability and visibility into package warpage ahead of time increase post-silicon validation risks

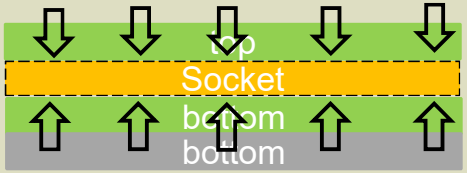
Package Warpage vs Temperature



Desired vs Actual Boundary Condition

Desired boundary condition for evenly distributed contact resistance

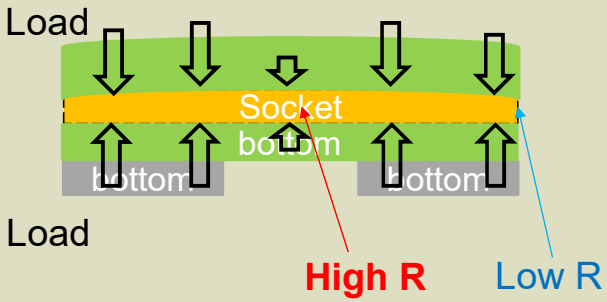
Evenly distributed loading



Evenly distributed loading

In order to achieve evenly distributed loading, top and bottom has to be perfectly flat

Actual boundary condition for unevenly distributed contact resistance



Unevenly distributed loading due to warping on the top and uneven support on bottom

Case Study

Objective:

- Bring out the influence of package warpage to socket connectivity risks in post-silicon validation
- Highlight key parameters that govern socket connectivity risks and impact system stability

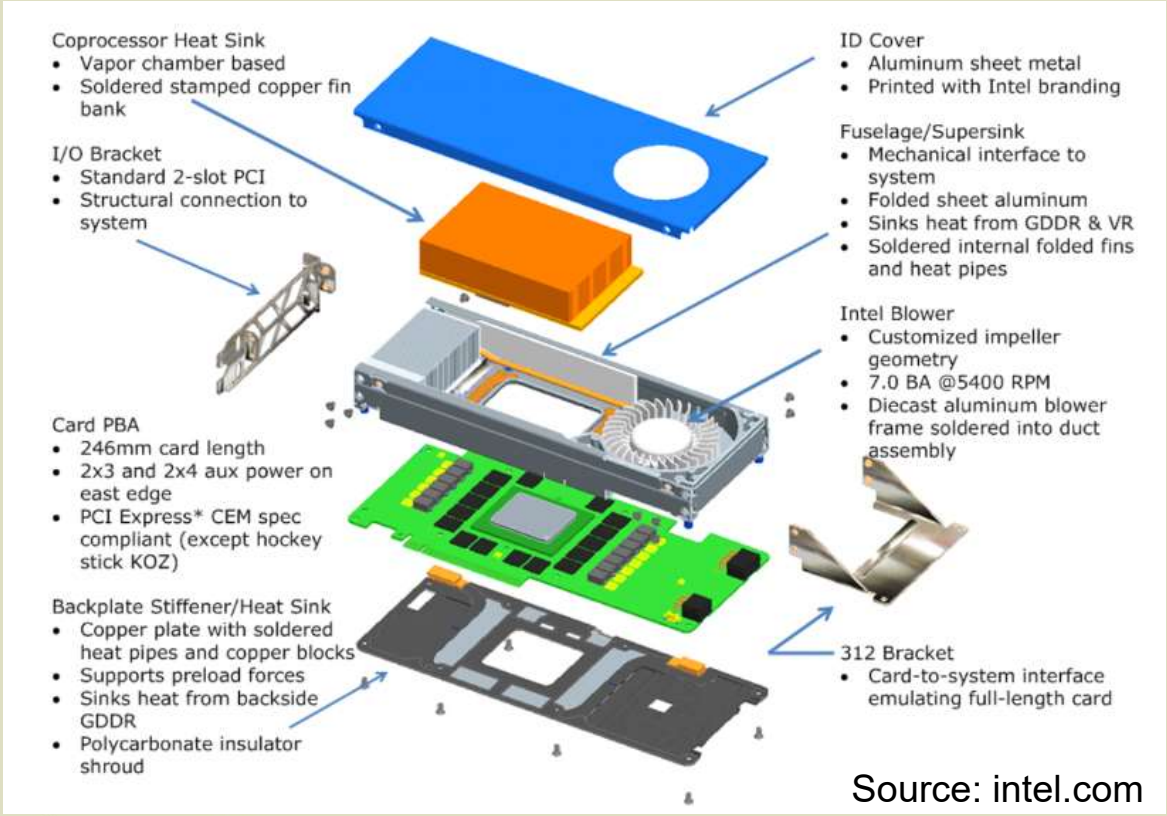
Large BGA Package Case Study: Knights Corner (1st Gen Intel Xeon Phi Co-Processor)

- First in industry: >1 TFLOP of performance in one single silicon
- Launched Q4'2012
- Powered the fastest supercomputer on TOP500 list and stayed #1 for 2.5 years
- >3000 BGA pins

Sources:
intel.com, ark.intel.com, top500.org

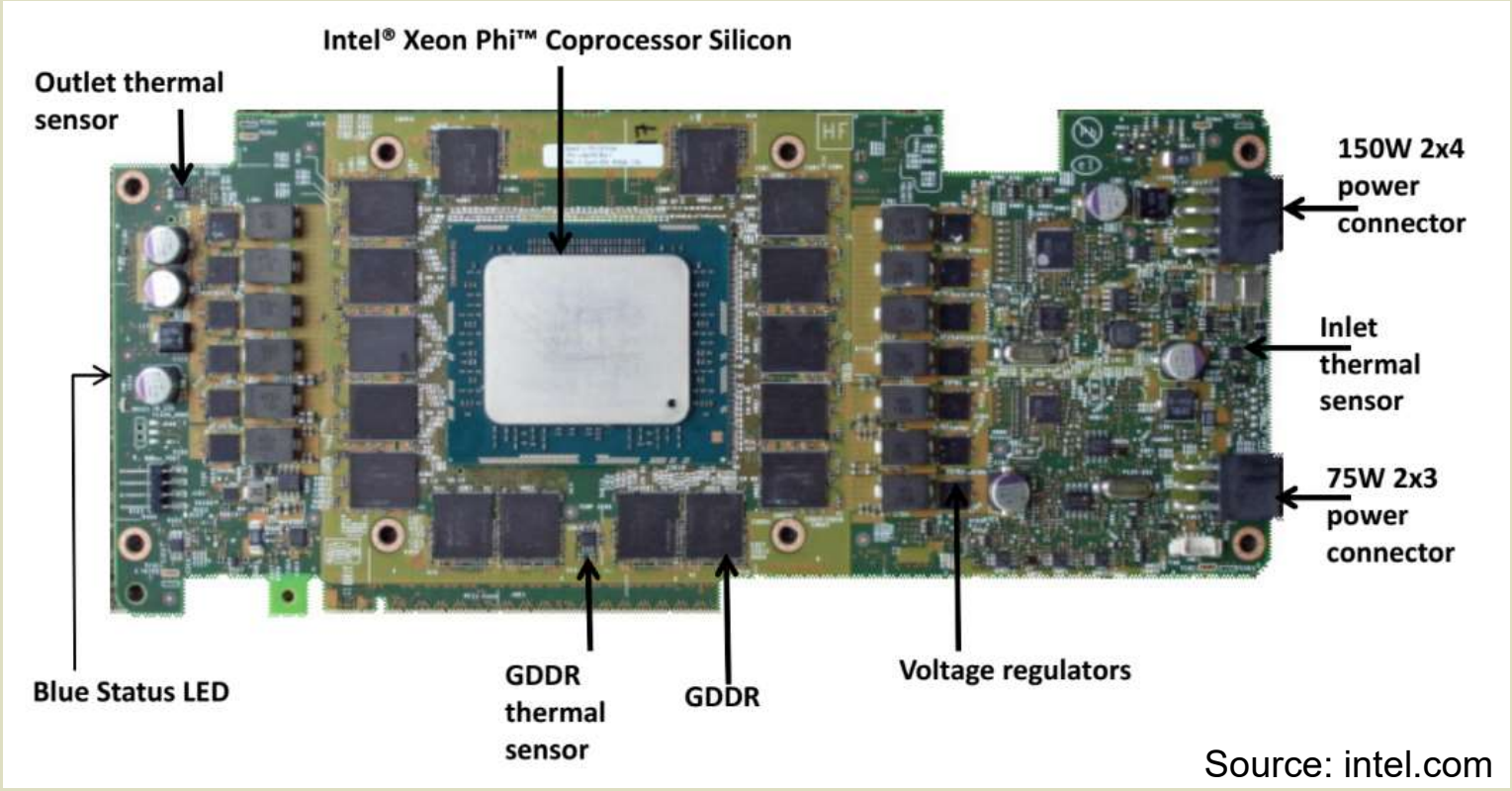
TestConX™

Case Study: Knights Corner Card Exploded View



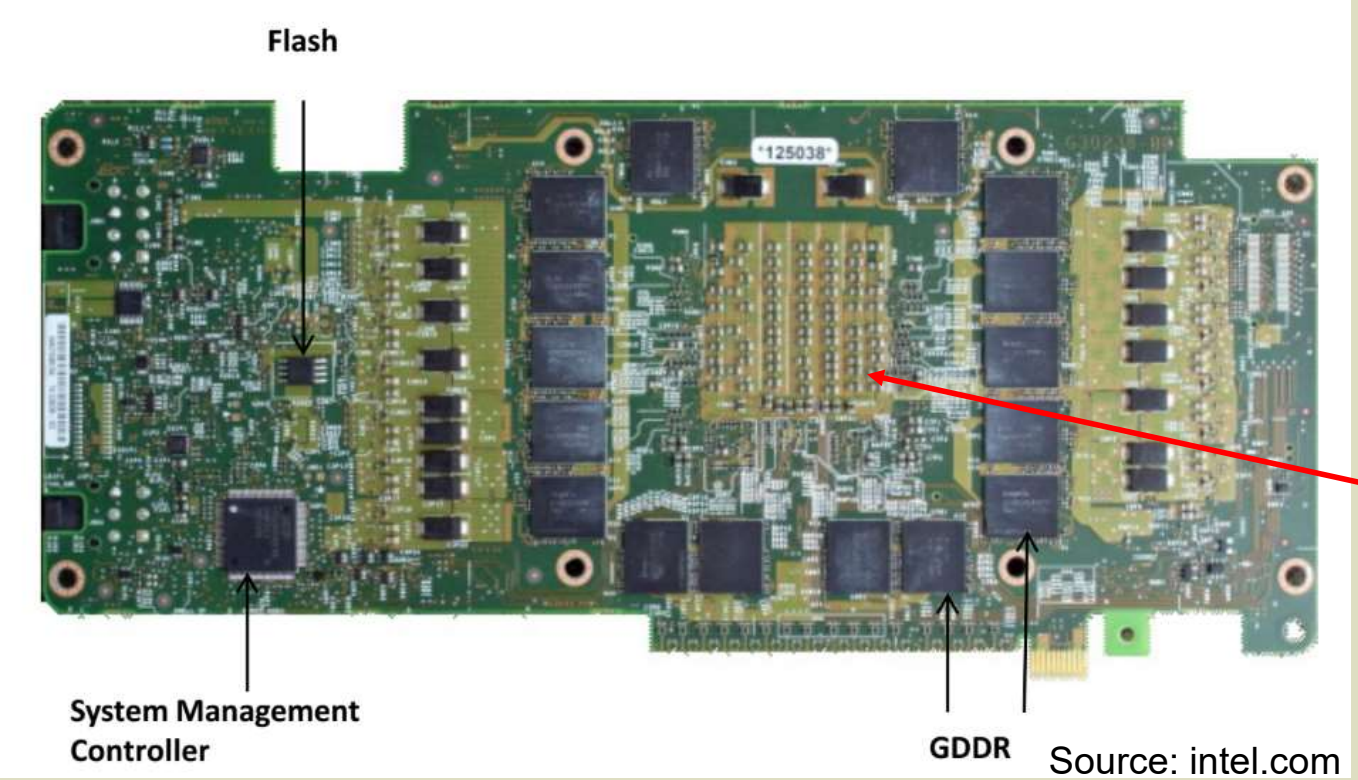
Source: intel.com

Case Study: Knights Corner Package/Board View



Source: intel.com

Case Study: Knights Corner Package/Board View



Complicates socket retention mechanism

Dense and small components on secondary side

The Elastomer Socket for post-silicon Validation

- Pin properties are temperature and time dependent
- Relation between contact resistance, deflection, and contact force
- The ideal boundary condition on the socket?
- Main challenges for FEA: lack of material constitutive properties (stress strain curves, etc) to model the individual pin

What is the "Ideal" Package for Socket Design?

- If the package is perfectly flat and free of residual stress throughout all temperature change and time of the assembly, test, and life cycle, this could reduce electrical failures
- But this ideal package violates basic physics as there will always be CTE mismatch between dissimilar materials
- Real package is never flat

The Mechanical Retention

- The typical retention and board design
  - Versus the “ideal retention and board design”
- Constraints due to component placement on the board on structural support

Putting it together

- The contact force distribution is not even over the entire BGA pin field
- Hence, the contact resistance is not even over the BGA field
- The socket retention designer has two objectives
  - Make sure all pins are compressed to at least a certain amount
  - Try to have the pin compression as even as possible
- The socket retention designer must assess or depend on
  - Retention force distribution (die vs stiffener etc)
  - Package initial warpage
  - The coplanarity of the pins (BGA and socket pins)
  - Board warpage
  - Primary side bolster plates and secondary side backing plates
    - Location and size of KOZ available for structural support

Finite Element Model

- Assumptions
  - Alter the initial (high) temperature of the package model to obtain variation in the package warpage
    - Actual initial temperature at chip attach is unknown
  - From variation in package warpage obtain variation in pin contact forces
- Trends
  - Warpage induced
  - Backing induced
  - Bolster induced
  - Force distribution induced
- Risk assessment
- Knobs to turn

Knobs to Turn for FEA

- Total actuation force
- Force distribution (% die vs substrate)
- Bolster plate (yes/no)
- Backing plate
  - Extra pushing from the back (varies)
- Package warpage (varies)

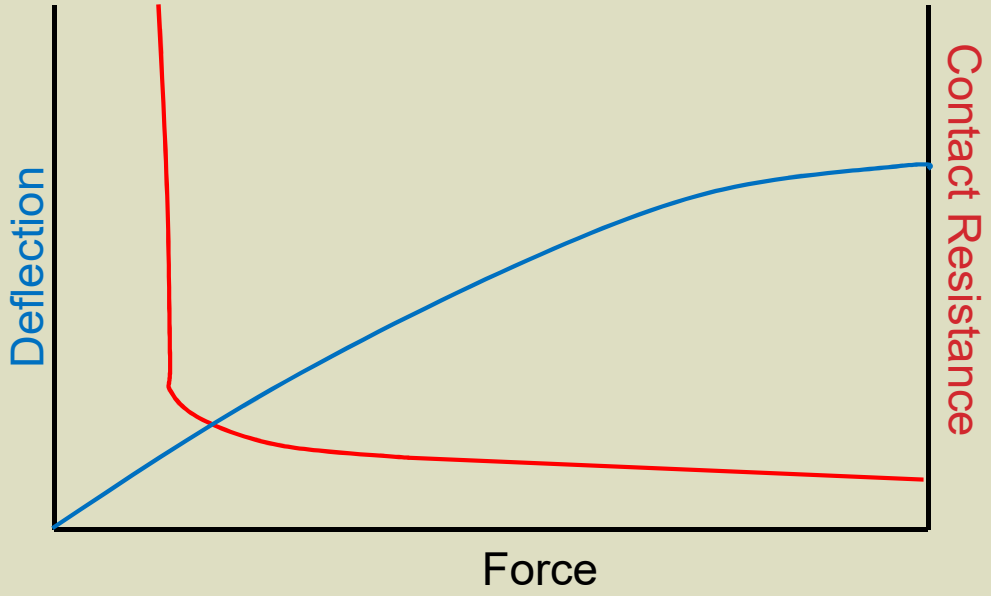
FEA Package Warpage Simulation

- Package properties and manufacturing process may not be known due to confidential IP
- Best guess could be made to properties and manufacturing process to best match Test Vehicle package warpage and shape measurements
- Therefore, not really a package warpage "prediction" per se, if we have little to no visibility into properties and processes
- Use package warpage as a variable knob to turn to find out the sensitivity of package to warpage

Using Pressure Overclosure Law to Simulate the Socket

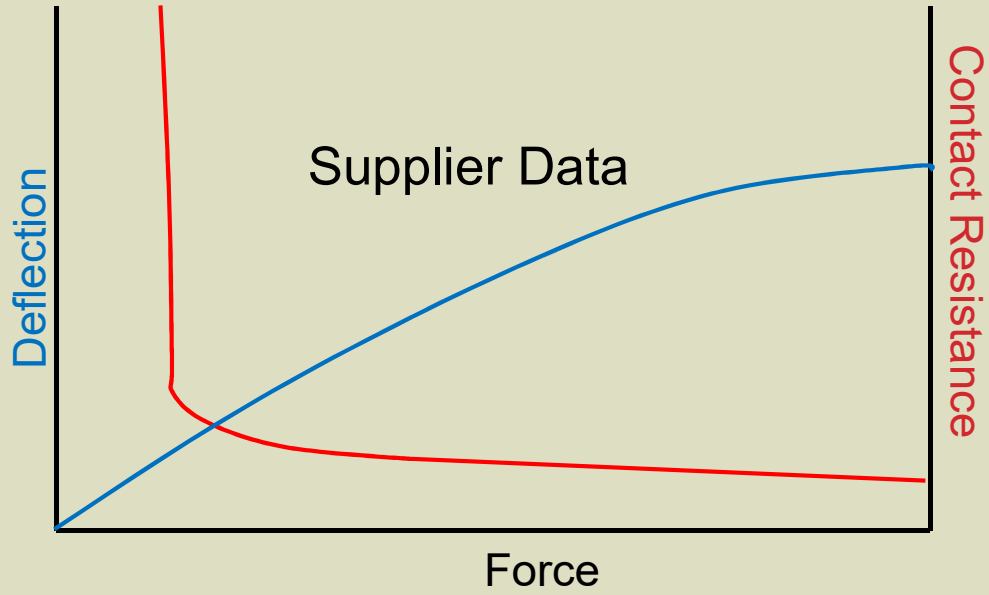
- Pressure Overclosure laws are offered in commercial FEA software packages
  - Customized subroutines typically not required for usage
- The trick to modeling the pin force without material properties is to treat the pin field as a discontinuous “contact surface” model rather than as actual solids
  - If socket pins are modeled as solids, then material properties are needed
- Translates supplier’s socket pin’s Force Deflection curve (see a typical curve) into pressure overclosure law for finite element model’s contact properties
- Circumvents the difficulty of not knowing the elastomer’s material constitutive properties (e.g., stress strain curves) for the pin’s ever changing recipes
- Limitations: cannot model viscoelastic, hyperelastic, or plastic aspects of the pin material

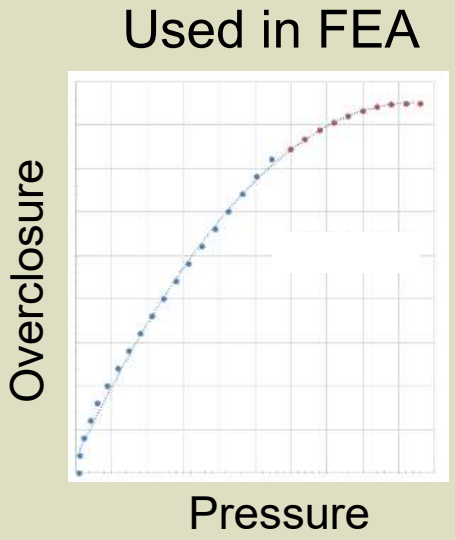
Deflection / Force / Resistance curve of Socket Pin



Note: these characterization curves are typically supplied by socket vendors

Force Deflection Resistance Curve of an Elastomer Socket

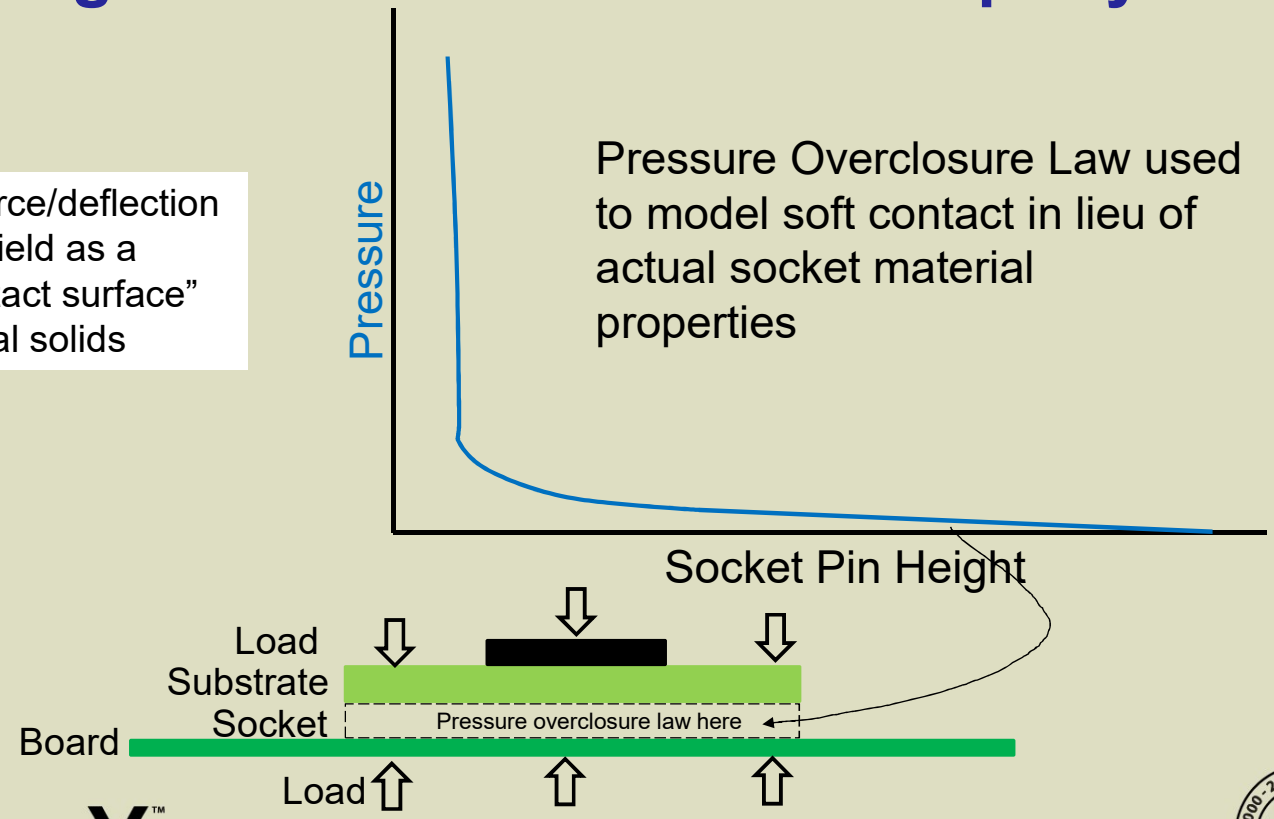




Challenge to FEA: how do we model the socket pin deflection using only this data from the supplier?
Can translate this supplier data into pressure overclosure law in modeling pin contact

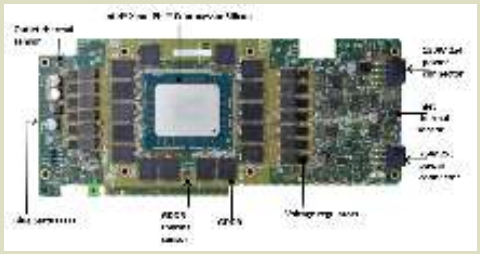
Modeling the Socket as Contact Property

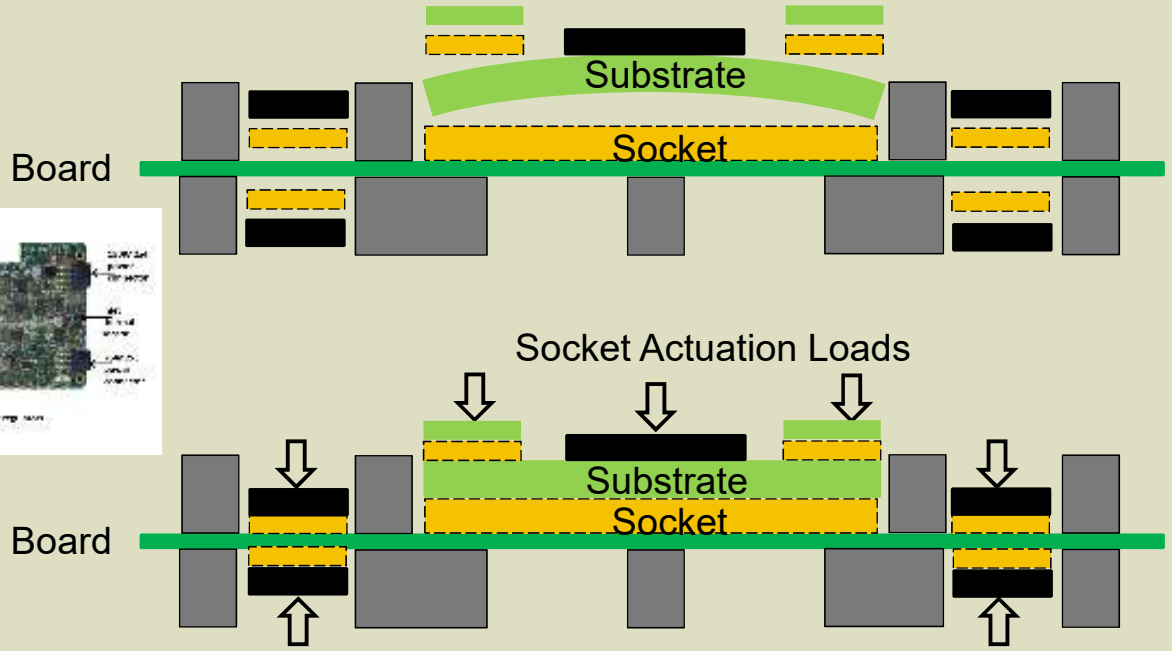
Modeling the pin force/deflection by treating the pin field as a discontinuous "contact surface" rather than as actual solids



Pressure Overclosure Law used to model soft contact in lieu of actual socket material properties

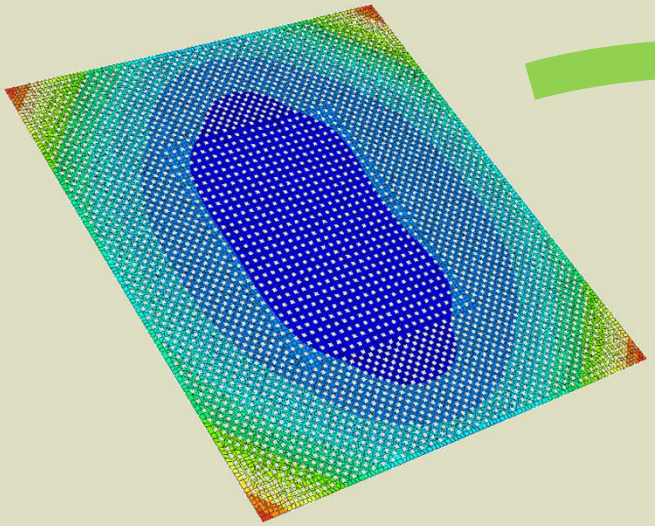
Boundary Condition in Post-Silicon Validation Configuration



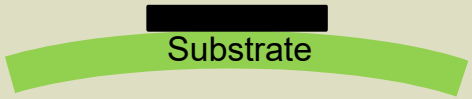


Note: Validation Thermal Mechanical System not shown

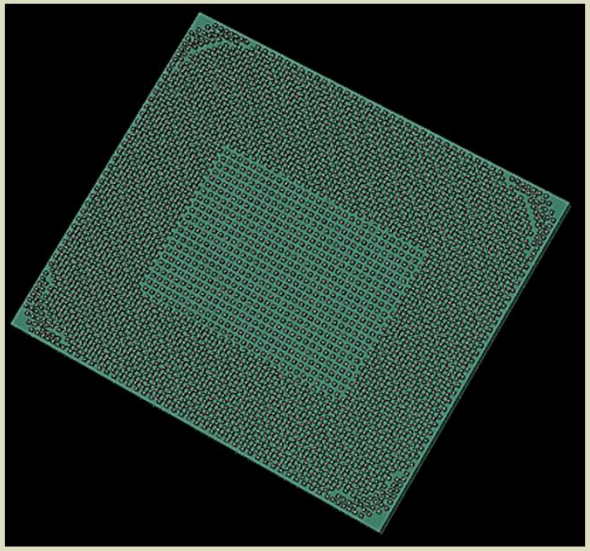
FEA of Incoming Package Warpage Test Vehicle A

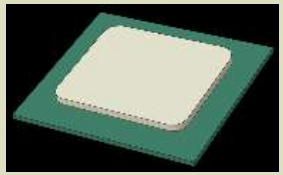


Warpage contour plot at 20C

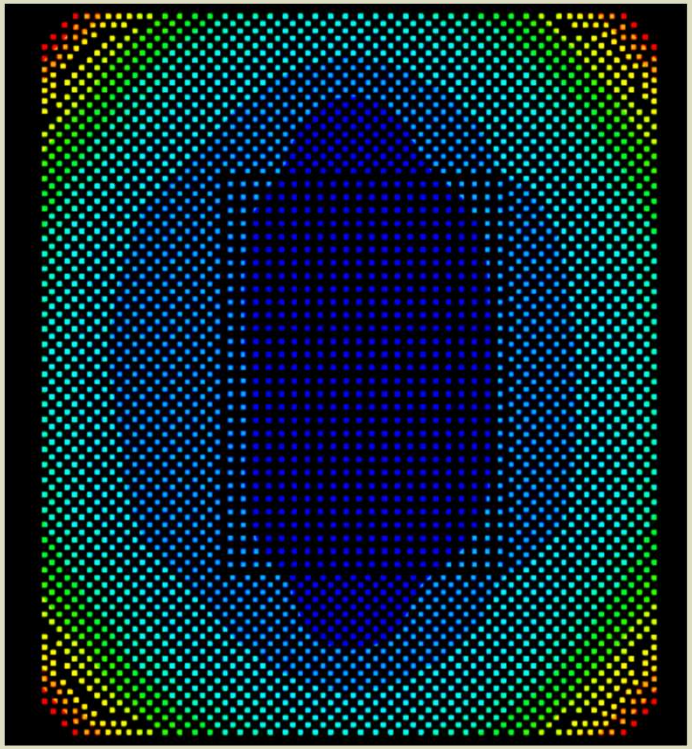


Actual packages can vary significantly in warpage values due to manufacturing process variation





Pin Deflection Contour Plot After Socket Actuation



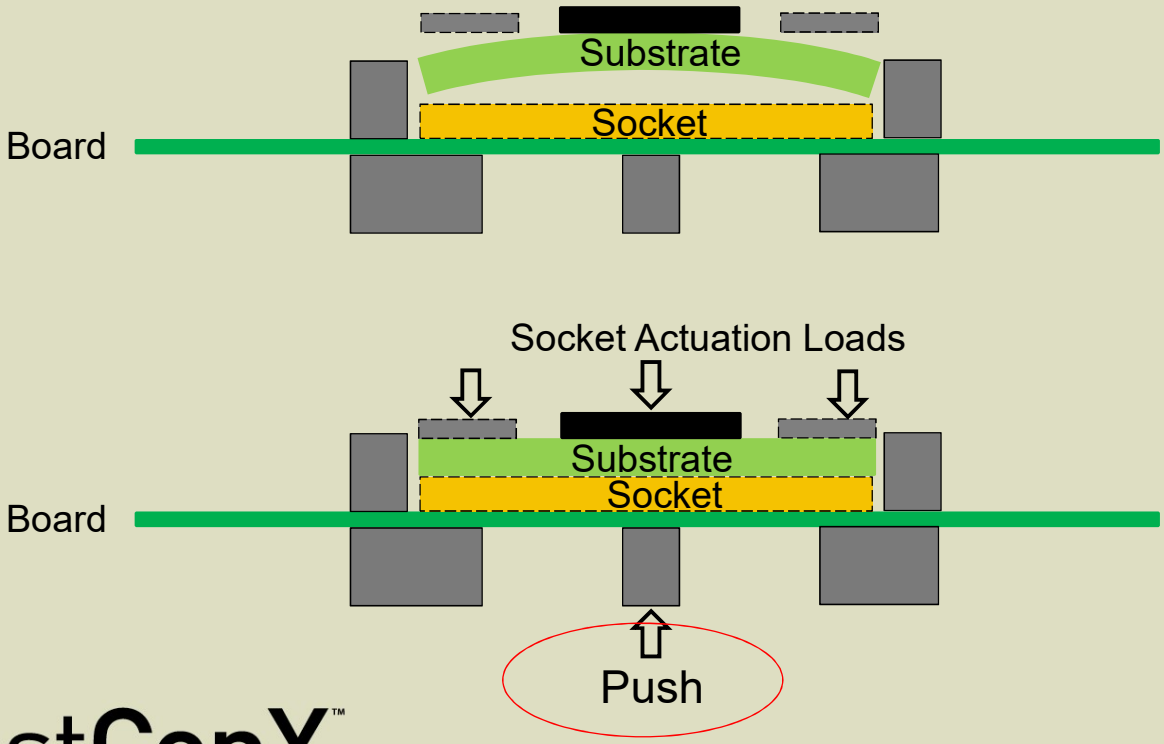
Blue pins have least deflection under socket actuation load with package warpage

In this specific case, center pin has highest LLCR risk

In general case, the highest LLCR pin location may vary

Pin deflection field can be mapped to contact resistance gradient for input as next iteration for electrical simulations

Boundary Condition during Sensitivity Analysis using Test Vehicle B



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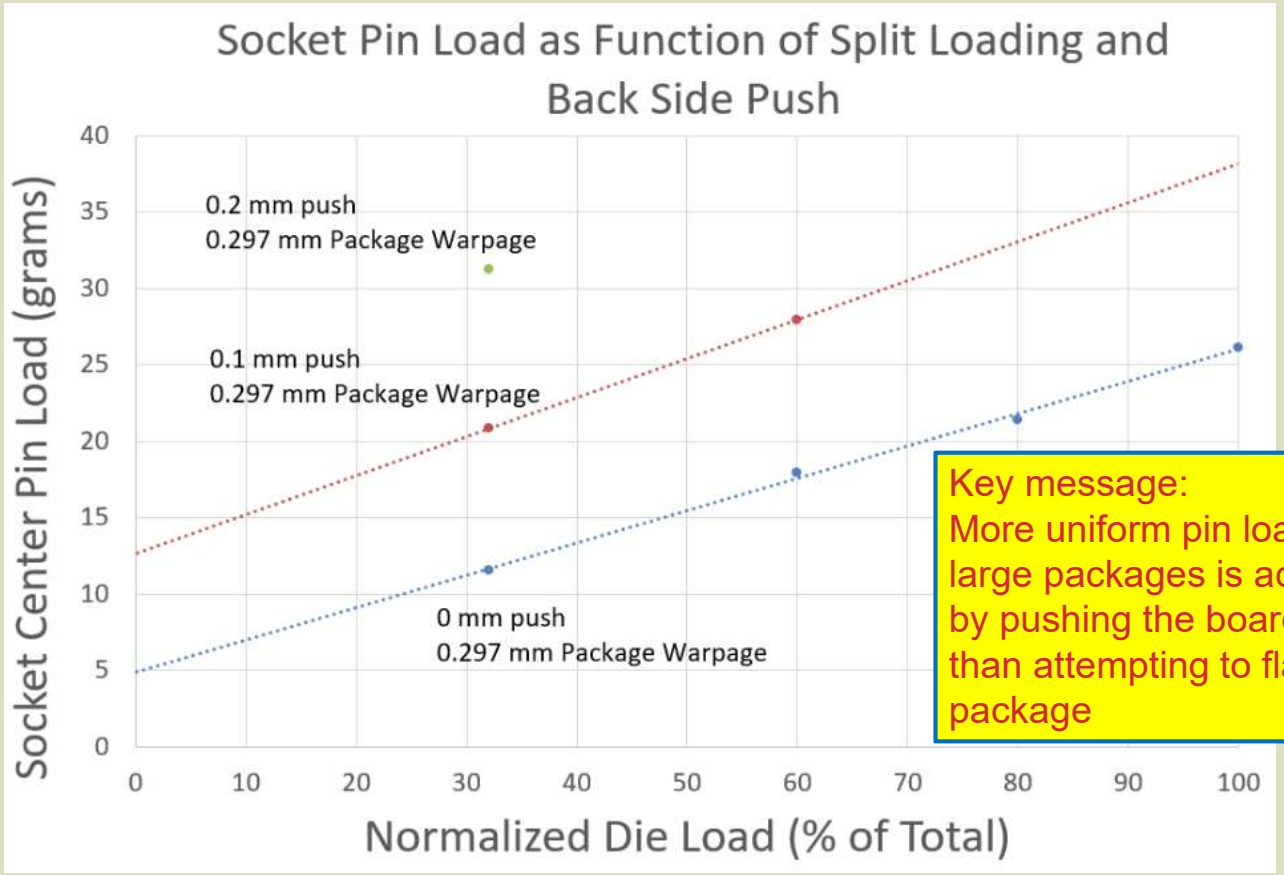
224

224

Sensitivity Analysis (1)

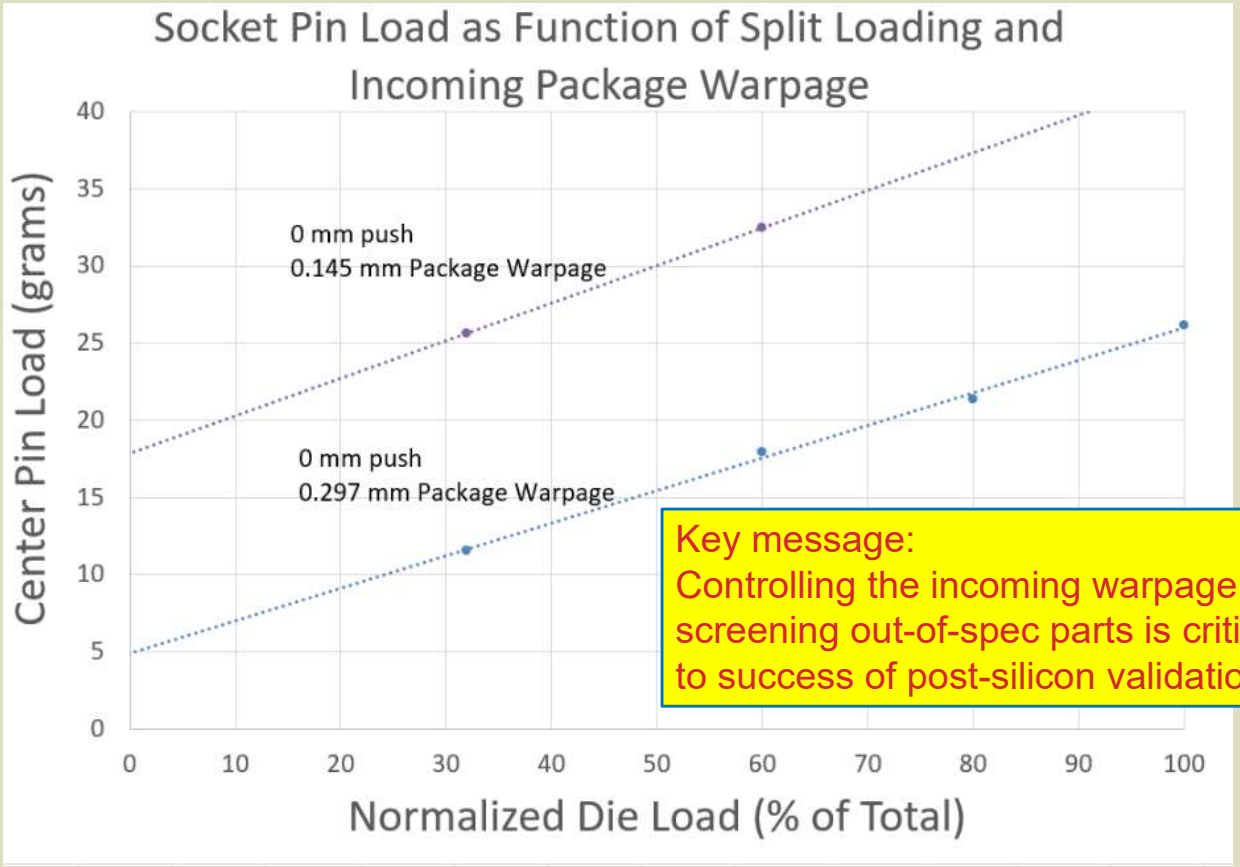
- Parameters varied
  - Force distribution between die and stiffener (total load fixed)
  - Amount of upward displacement on the center of the board on the secondary side
- Output studied
  - Center pin load
- Key Trend
  - Pushing from the secondary side is more effective than changing the force distribution



Key message:
More uniform pin loading of large packages is achieved by pushing the board rather than attempting to flatten the package

Sensitivity Analysis (2)

- Parameters varied
  - Force distribution between die and stiffener (total load fixed)
  - Variation of End of Line (EOL) Package Warpage
- Output studied
  - Center pin load
- Key Trend
  - EOL Package Warpage has a more dominating effect over pushing from the secondary side or changing the force distribution

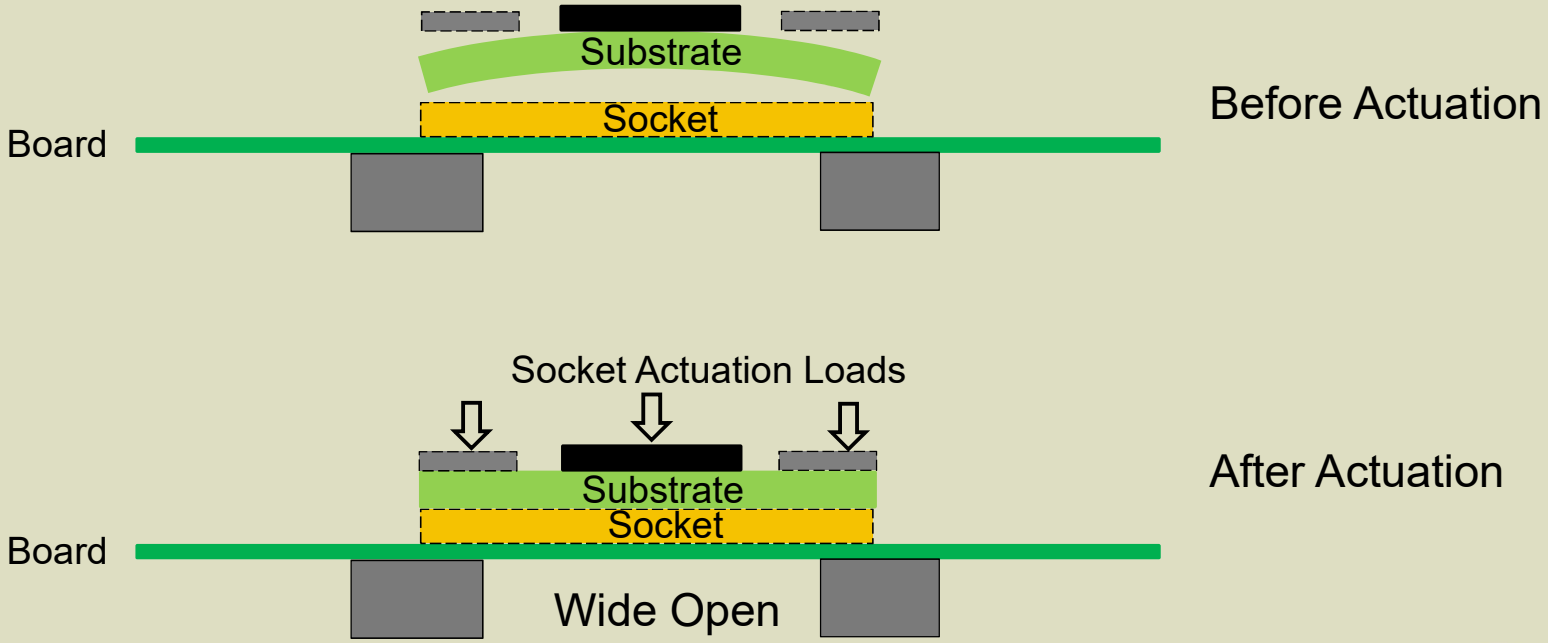


Key message:
Controlling the incoming warpage by screening out-of-spec parts is critical to success of post-silicon validation

Sensitivity Analysis (3)

- Parameters varied
  - Variation of End of Line (EOL) Package Warpage
- Output studied
  - Center pin load
  - Board warpage
- Key Trend
  - Center pin load decreases as board warpage *decreases*
    - This trend is caused by the underlying increasing package warpage
    - Contrary to the conventional wisdom of "as long as the board stays flat, the risk of connectivity is low"
  - Neglecting large package warpage and modeling board warpage alone could yield misleading risk assessments

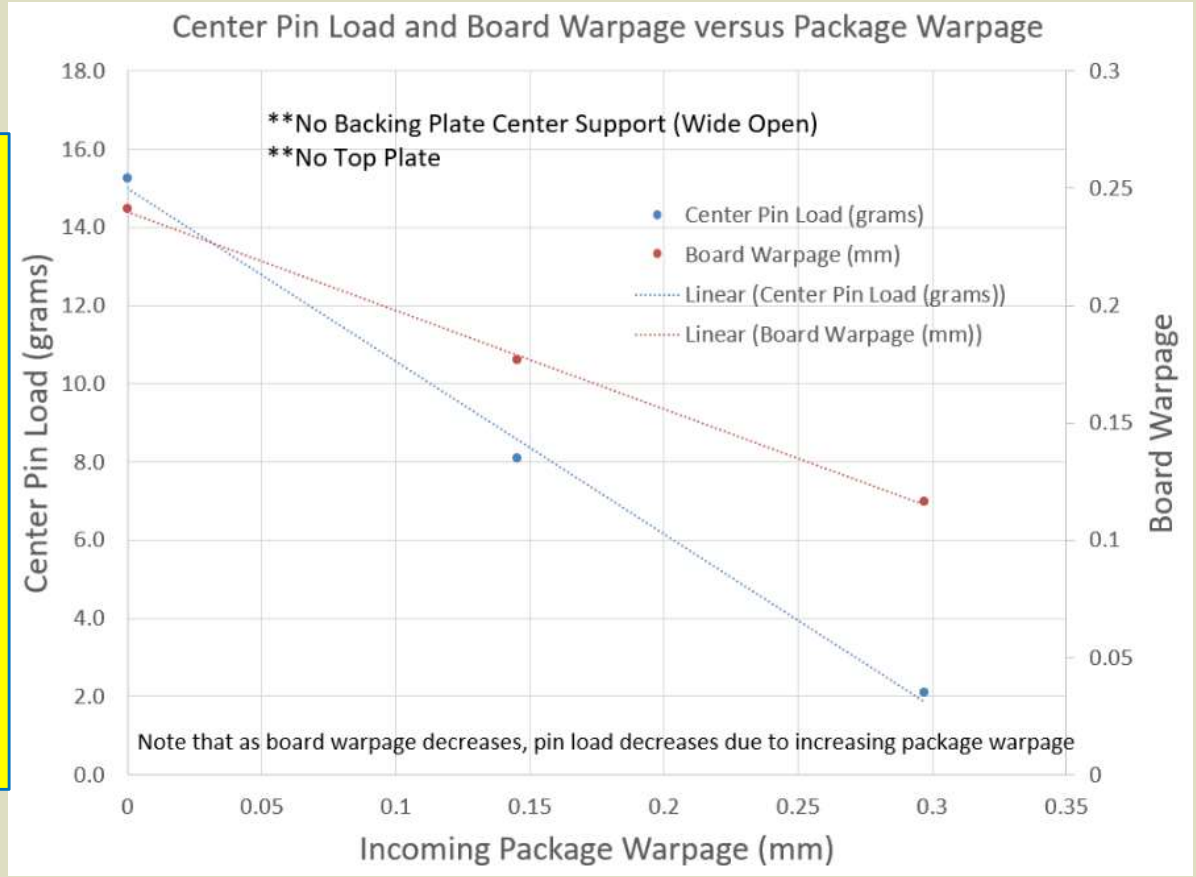
Boundary Condition during Sensitivity Analysis using Test Vehicle B



Key messages:

Controlling the incoming warpage by screening out-of-spec parts is critical to success of post-silicon validation

More uniform pin loading of large packages is achieved by pushing the board rather than attempting to flatten the package



Summary: Socket Case Study

- Sockets typically used in Post-Silicon Validation
- Case Study:
  - Scope: Large BGA package with elastomer sockets, challenges, metrics to mitigate LLCR
  - Case Study: 1st Gen Intel Xeon Phi
  - Physics and control of package warpage
  - Finite Element Analysis to analyze socket pin deflection including large package warpage, what to do with missing information
  - Sensitivity studies showing what the socket retention designer can do to mitigate socket connectivity risk

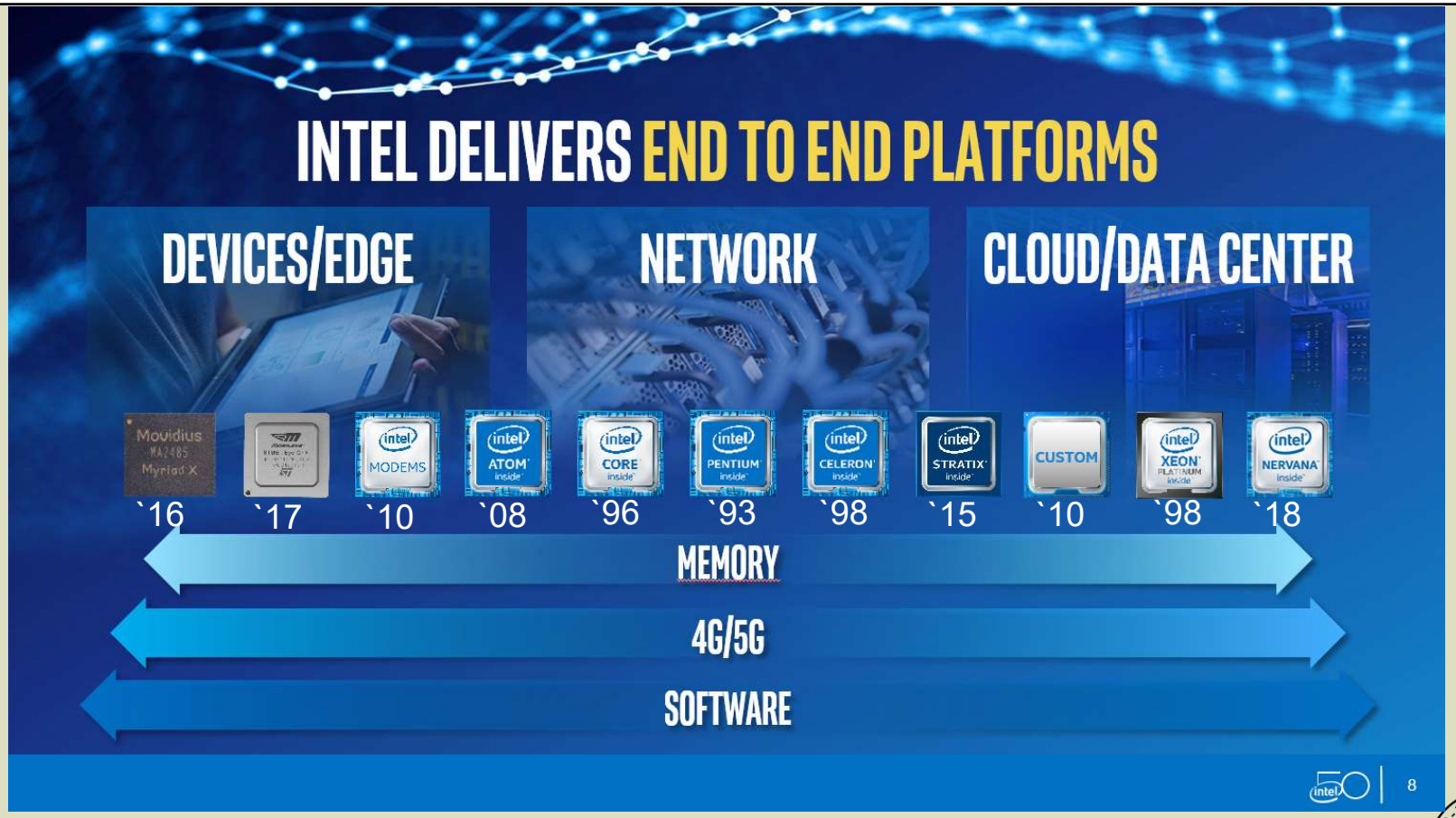
Case Study

SCALING THERMAL TOOLS FOR PRODUCTS WITH > 500 W AND -40 C TEMPERATURE REQUIREMENT

Top Level Agenda

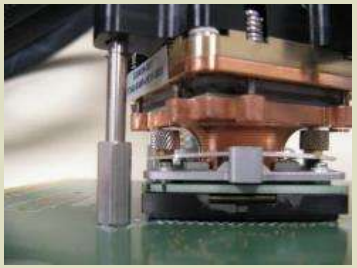
- Trends and Thermal Tool Design Challenges
- Case study: High Power and -40 C Solution
  - Primary temperature forcing methods
  - Types of temperature forcing systems
  - TEC based Thermal Tool
  - Phase Change Thermal Tool
- Summary

Trends and Thermal Tool Design Challenges

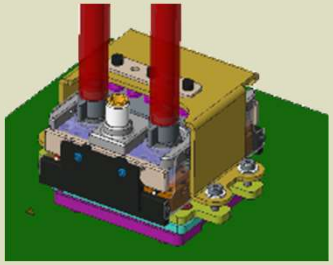

INTEL DELIVERS END TO END PLATFORMS
DEVICES/EDGE
NETWORK
CLOUD/DATA CENTER
Movidius
Myriad X
MODEMS
ATOM
CORE
PENTIUM
CELERON
STRATIX
CUSTOM
XEON
NERVANA
`16
`17
`10
`08
`96
`93
`98
`15
`10
`98
`18
MEMORY
4G/5G
SOFTWARE
8

Challenges to Meet Multiple User Environments

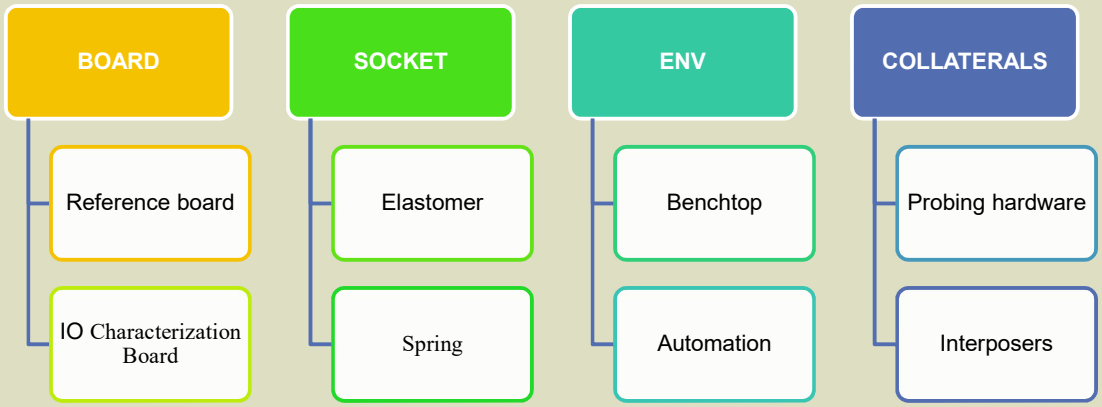
Thermal tools design, development and deployment need to address multiple user requirements, environments and cohabitation with interposer, probing hardware and different sockets.



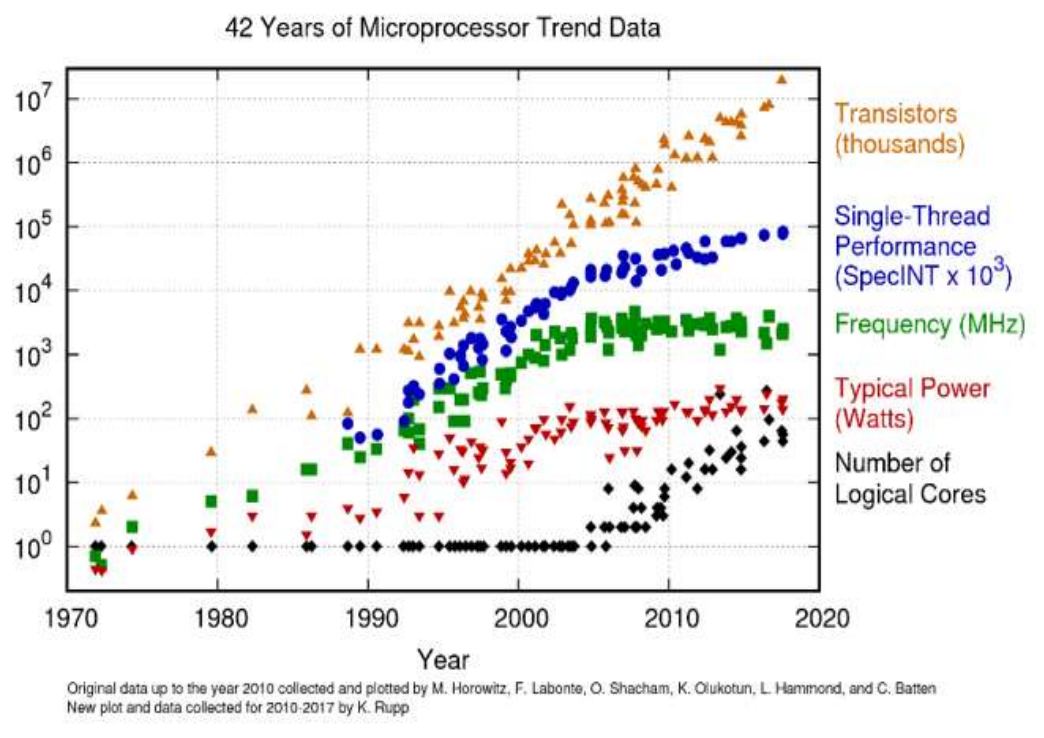
TT cohabitate with Probing HW



TT is compatible with different socket



High Power Product Challenge Cooling Technologies

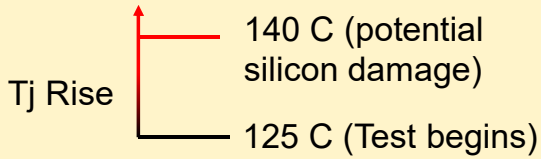


New Markets, Large Thermal Test Range

- ADAS products require broad operating environment (AEC-Q100 grade 2: Tj -40 C ~ 125 C) and long lifetime expectation, typically in the range of 15+ years.

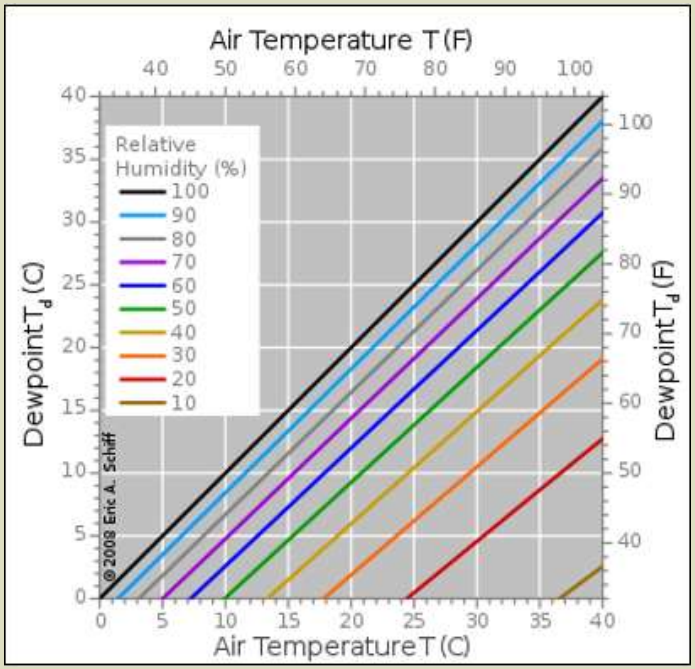
Ambient Operating Temperature Range	Junction Temperature Range
–40° C to 105° C	–40° C to 125° C

- -40 C Tj means Tc should be much lower than -40 C which challenges the TT cooling capability
- 140 C is silicon safety temperature limit

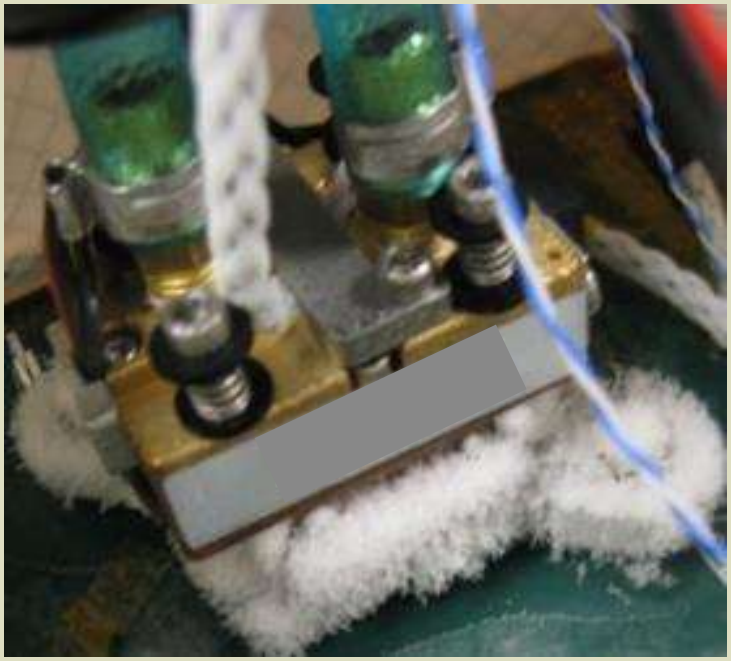


- Condensation management is critical for -40 C test

Condensation Management is Critical for -40 C Test



Graph of the dependence of the dew point upon air temperature for several levels of relative humidity.

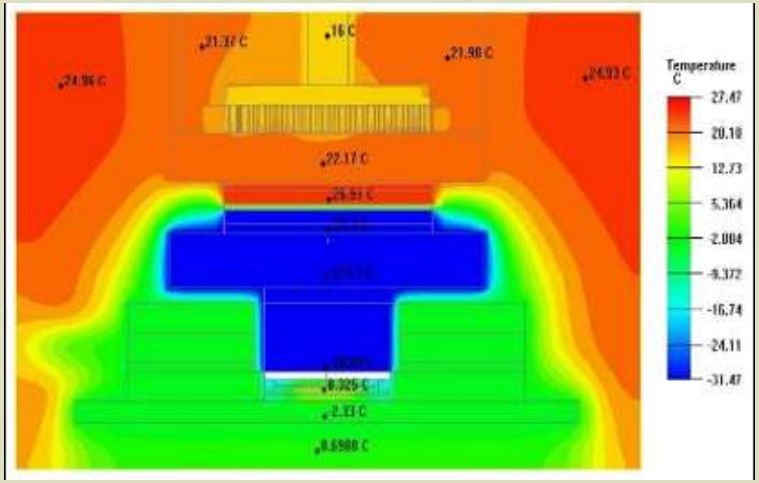


Ice accumulated on cold plate

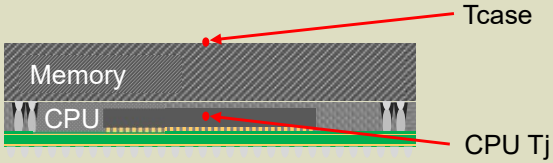
Courtesy: Wikipedia

Pop Package Brings Difficulties for SOC Temperature Control

- High temperature margining requirement for low power package
- Large thermal resistance through package stack-up
- Large temperature gradient from memory Tc to SoC Tj
- Memory operating temperature range is lower than SoC
- PCB operational temperature limit
- Limited thermal solution space between (i) memory and SoC and (ii) SoC and PCB

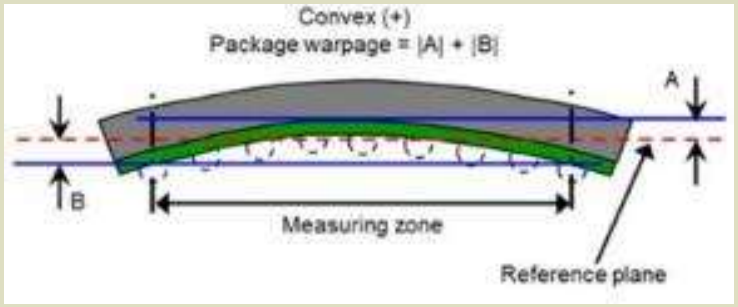


Ice accumulated on cold plate

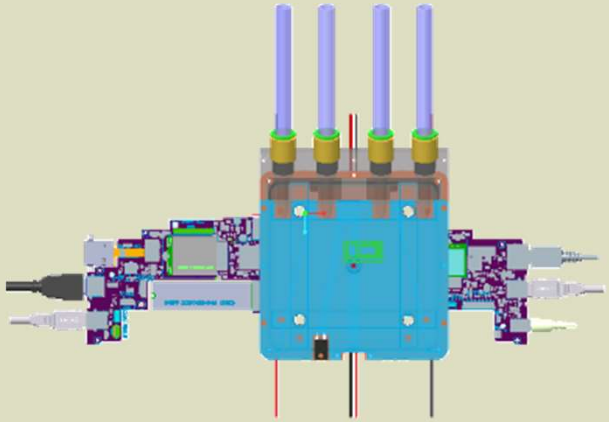


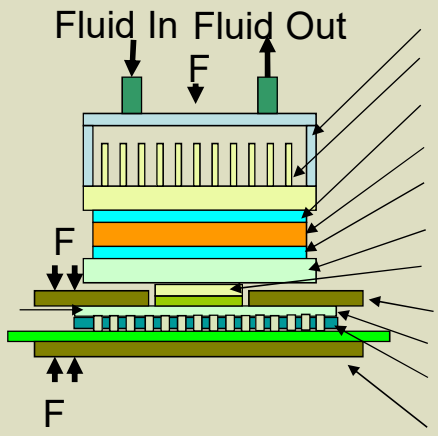
Mechanical Challenges

- Platform mechanical volumetric constraints
- High load required for high pin number socket/package connection
- Large warpage on big package
- Quick release retention
- Limited mounting holes or no mounting holes



Courtesy: Hsiu-PingWei etc





Coolant Chamber Cap
Fins and Base plate
TIM between TEC and base plate
TEC
TIM between TEC and Cold plate
Cold plate
Cold Plate Pedestal
Top Plate
Substrate
Socket
Back Plate

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242

Case Study: Scaling Thermal tools for products with > 500 W and -40 C temperature requirement

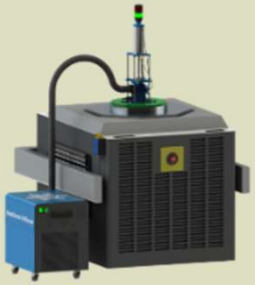
Agenda

- Primary Temperature Forcing Methods
- Types of Temperature Forcing Systems
- TEC Based Thermal Tool
- Phase Change Thermal Tool

Three Primary Temperature Forcing Methods

Mechanical refrigeration i.e. compressor	Expendable coolant such as LN_2 or LCO_2	Thermoelectric cooling Peltier chiller
closed-loop system that recovers and reuses the coolant	open system that expels the spent vapor into the atmosphere.	No need of pressurized of refrigerant lines
high cost if cooling below -40 C is required	Large cooling capability and range, but no heating capability	Relatively low cooling capacity and narrow range of operation
slower transition rates	fast transition rates	slow cooling rate
High initial cost	Storing, supplying and delivering cryogenic fluids can be expensive or otherwise challenging	Easy to be moved, reversible heat pump can also greatly simplify system designs. Performance degrade over time
hazard from pressurized leaks	Releasing N2 or CO2 to environment may have potential hazard issue	no concerns of environmental hazards

Types of Temperature Forcing System

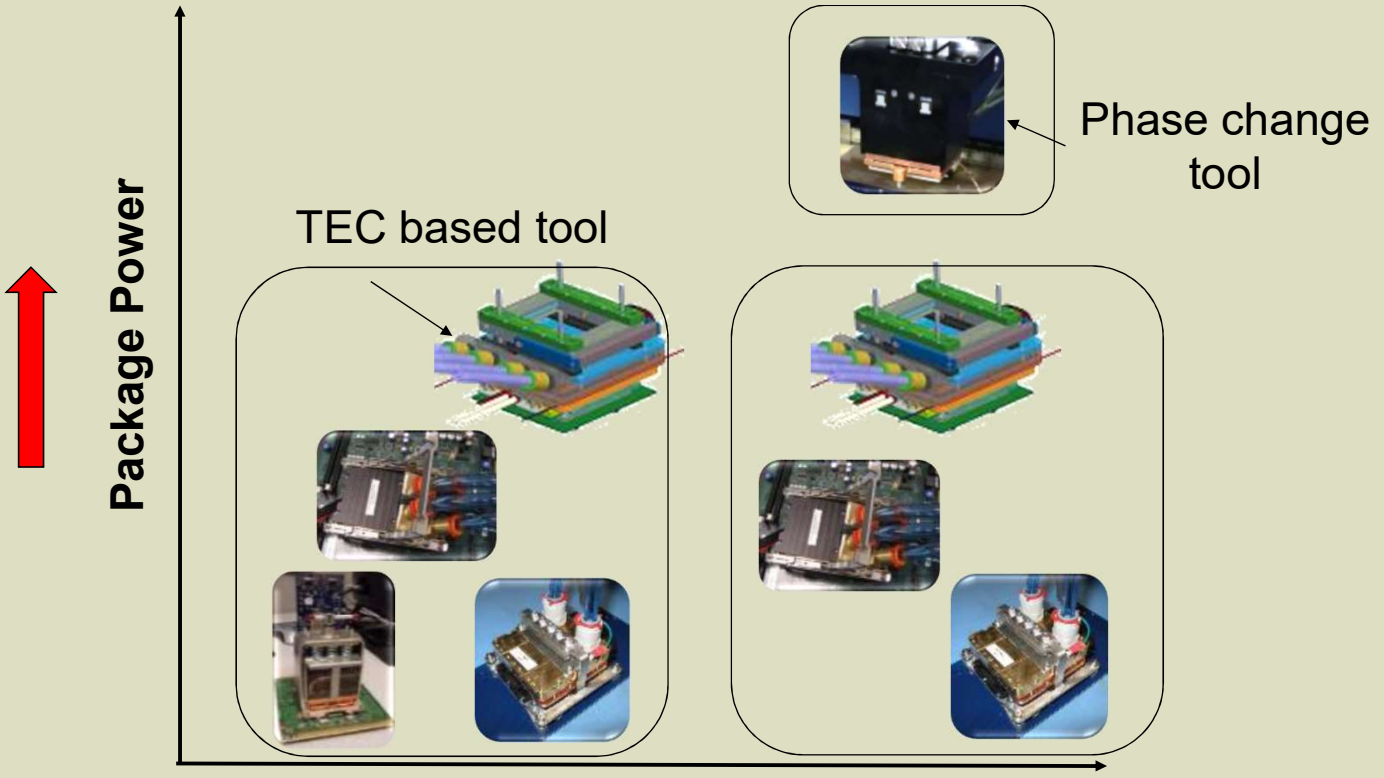
Oven or Test chamber	Thermal stream	Direct Thermal Head
	  Clean Dry Air	 TEC Based Margining Tool   Phase Change System (Refrigeration Compressors)

Courtesy:inTEST, Chroma, ESPEC Corp.

Types of Temperature Forcing System

Test chamber	Thermal Stream	Direct Thermal Head
Control whole chamber temperature	Inject hot and cold thermal air stream directly on the parts	Hot and cold plate directly touch the parts
System heating or cooling	Big KOZ, local heating or cooling	**Small KOZ, local heating or cooling**
Can test more than one devices simultaneously	test a single device per test	test a single device per test
convective temperature transfer	convective temperature transfer	thermal contact conductance
influence on whole testing system	influence on surrounding components	Control local DUT temperature
slower temperature changes	slower temperature changes	**Fast thermal response**

High Power Thermal Tool Solutions



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2000 - 2019 20 YEARS ANNIVERSARY

248

TEC Based Thermal Solutions

TEC Based Temperature Margining System

Liquid-Cooled Thermal Tool

Harness

Thermal Tool Assembly

Controller

Chiller/PCW

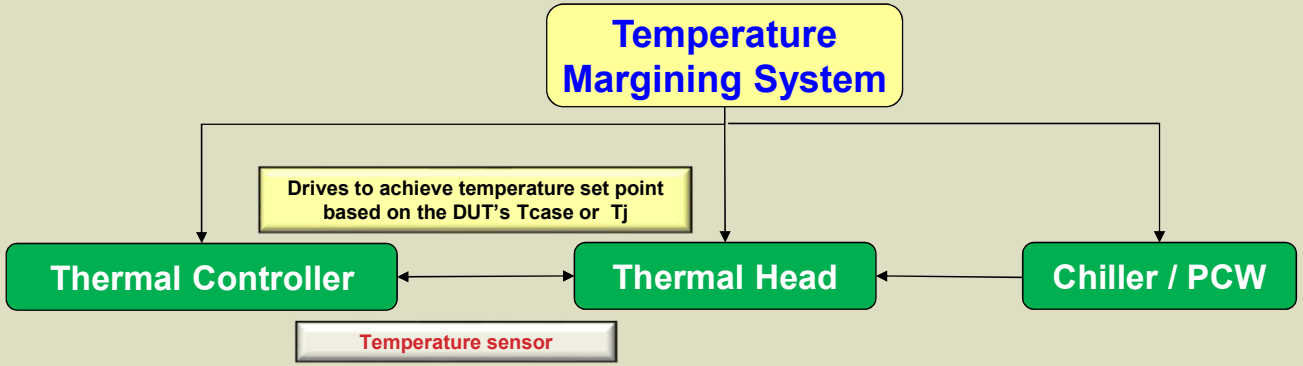
Air-Cooled Thermal Tool

Power Supply

TT

Courtesy:MSC

Thermal Margining System

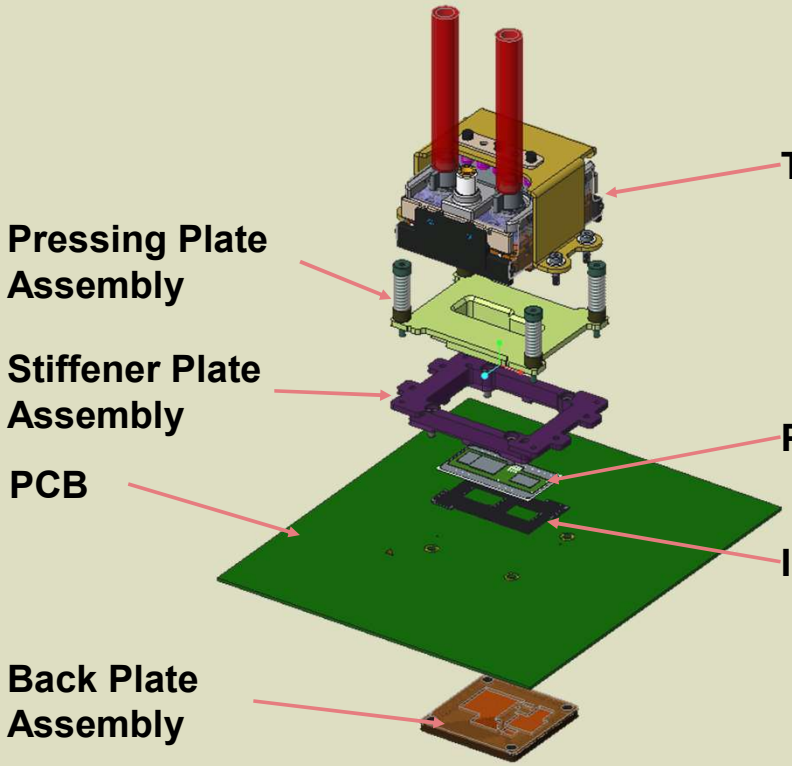


- Provides a T_setpoint based on the DUT's Tcase or Tj
- Controller's manifold system provides coolant to water block
- Adjust current that go into TEC to maintain temp at setpoint

- TEC works as heater or cooler based on T_setpoint
- Heat from heat source and TEC is dissipated by Water block or active heat sink

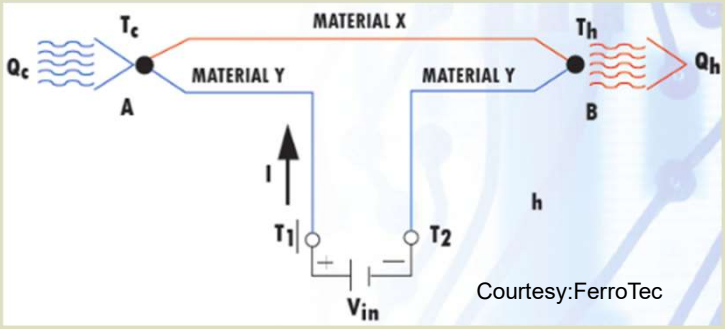
- Provides the Chilled Liquid Coolant

Typical Liquid Cooled Thermal Tool Setup

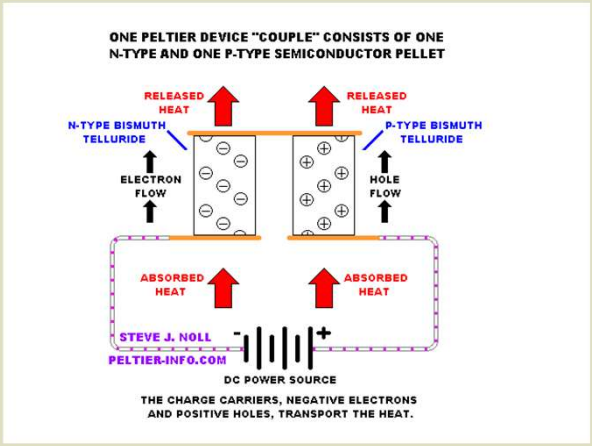


How Thermoelectric Device Work

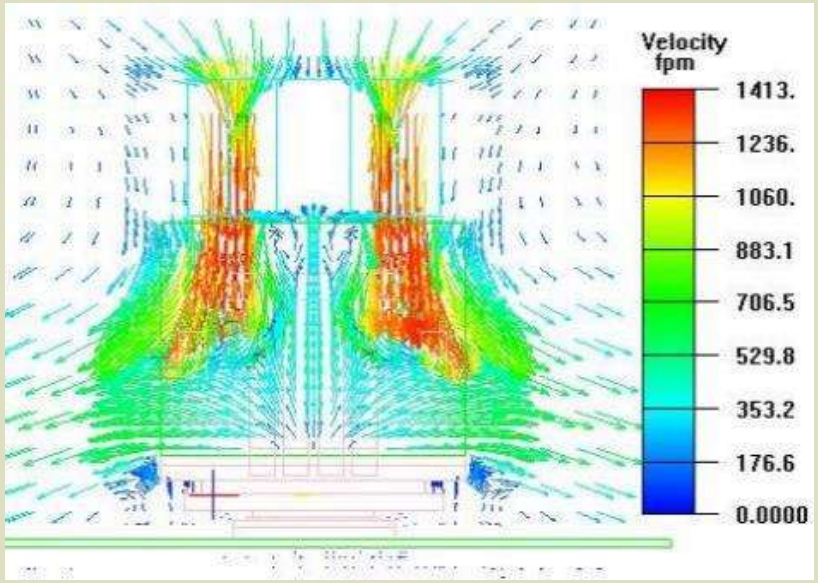
- **The working principle of thermoelectric** modules is based on the Peltier effect — heating or cooling at an electrified junction of two different conductors.
- **Peltier effect:** As per the Peltier effect, when two dissimilar metals are joined together to form two junctions, emf is generated within the circuit due to the different temperatures of the two junctions of the circuit.
- A TEC is a semiconductor-based electronic component that functions as a small **heat pump**. By applying a low voltage DC power source to a TE module, heat will be moved through the module from one side to the other.

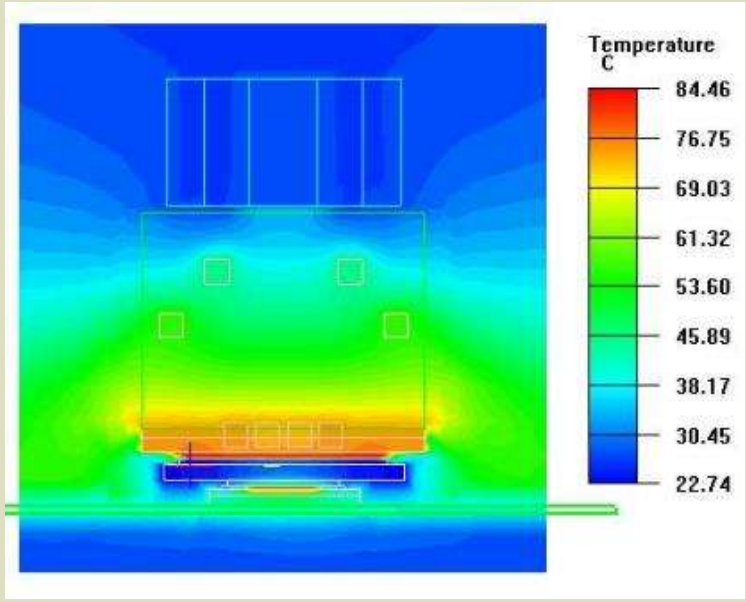


Courtesy:FerroTec



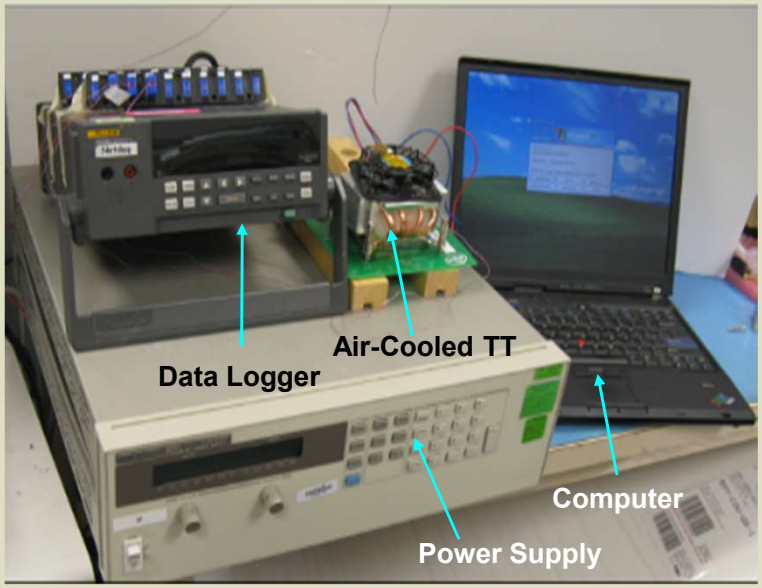
Thermal Modeling: Air-Cooled Thermal Tool

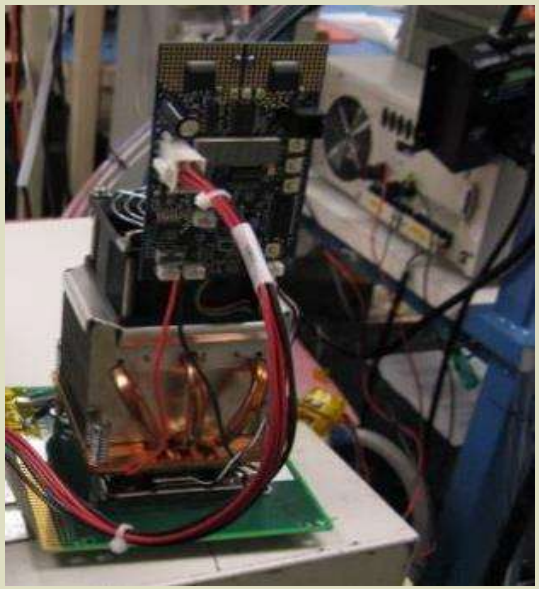




ICEPAK CFD Simulation results: Velocity contours and temperature distribution

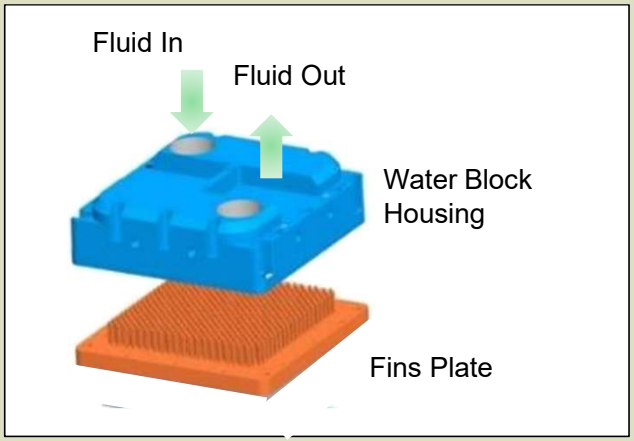
Thermal Performance Characterization & Correlation



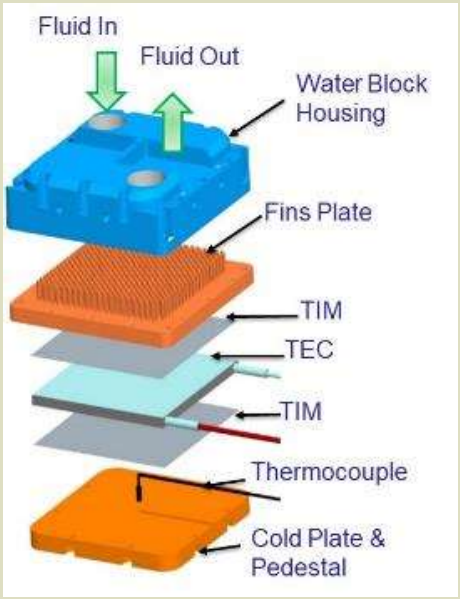


Thermal Characterization Test Setup

Difference Between Cooling Solution and Thermal Tool



Liquid cooling solution



Liquid cooled Thermal Tool

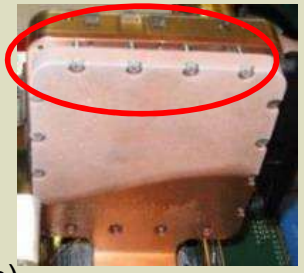
- Thermal tool:
  - Needs cooling solution
  - Can be used as cooler or heater
  - Provides margining capability and control
- Thermal margining system: complete thermal control feedback system
- Cooling solution for thermal tool is more powerful since it needs to cool both heat source and TEC

Facilities Requirements

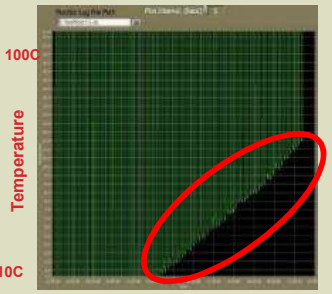
1. **Electrical Requirements**
   - 110 Vac or 220 Vac
2. **Dry Air Requirements**
   - Dry air is needed when TT runs at temperature lower than dew point. Dry air box is required for -40 C test.
3. **Fluid/Process Chilled Water (PCW) Requirements**
   - Fluid/Coolant Temperature range: 10-20 C
   - Special Coolant & Additives is used for corrosion and algae prevention

Common Field Issues & Failure Modes

- Thermal tool can't reach required testing temperature (controller, TEC)
- Performance degradation (bad TEC)
- Socket, package, MB connect issue (quality, retention)
- Abnormal delta T between Tc and Tj (contact)
- Die cracking (uneven load)
- Temperature does not go up or down (bad TEC)
- TT fluctuate and never get to the setting point (TEC, TC or insulation)
- Leak & clog issues in liquid-cooling system (fitting, coolant)
- Algae grow in liquid-cooling system (anti-bacteria)
- TEC cracking (uneven load)
- Galvanic corrosion (bimetal)
- Condensation
- Tube burst (tubing)

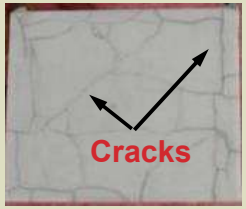


Condensation



Performance Degradation

Clog Issue



TEC Cracking & Degradation

Galvanic Corrosion

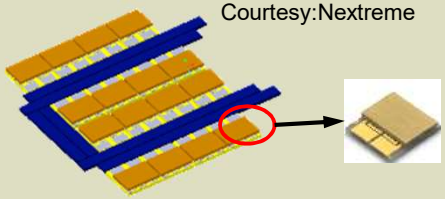
Die Cracking

Innovations to Improve Efficiency

Thermoelectric Cooler (TEC)

Single Stage Bulk TEC

Stacked Bulk TEC



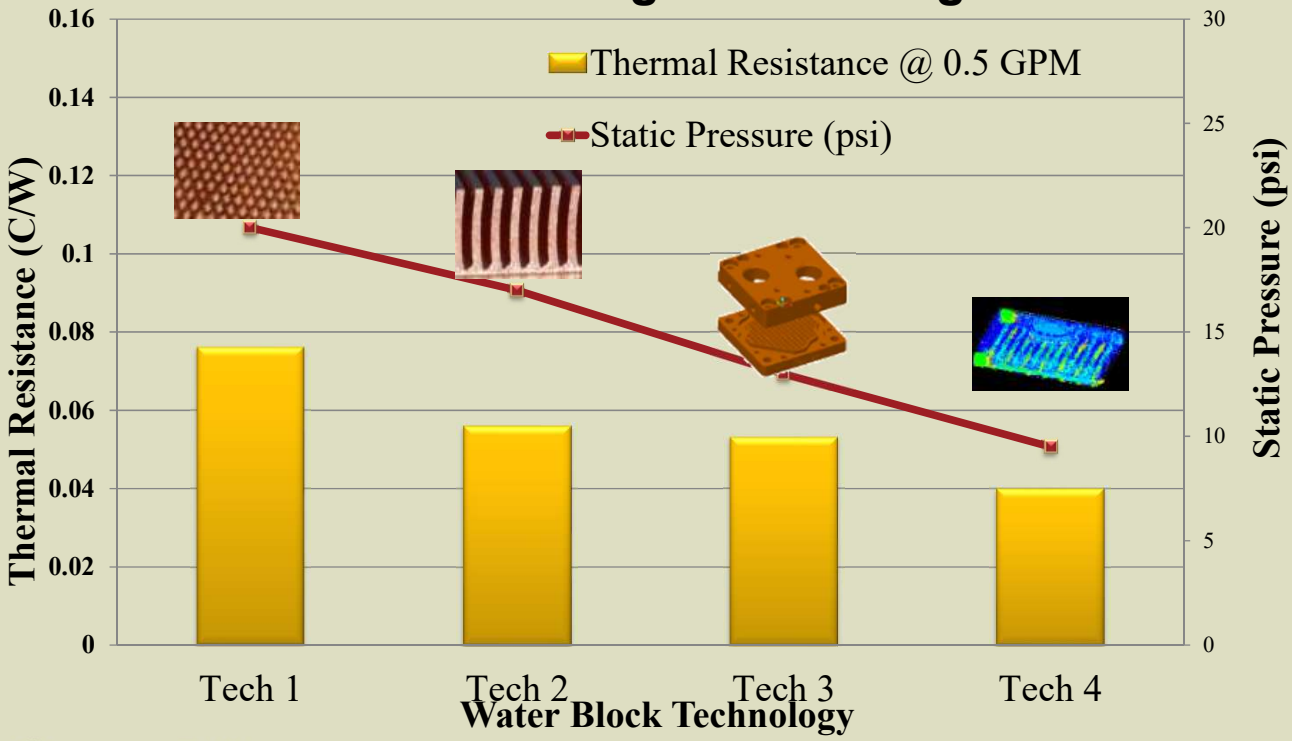
Courtesy:Nextreme

Thin-Film TEC Array

- Improve single stage TEC reliability & thermal performance
- Study dual stage TEC for extreme low temperature test
- Investigate thin-film TEC for small form factor TT design

Innovations to Improve Efficiency

Thermal Technologies – Cooling Block



TestConX™

Beyond Sort, Burn-In, and Class Testing: post-silicon Validation Hardware Strategy

260

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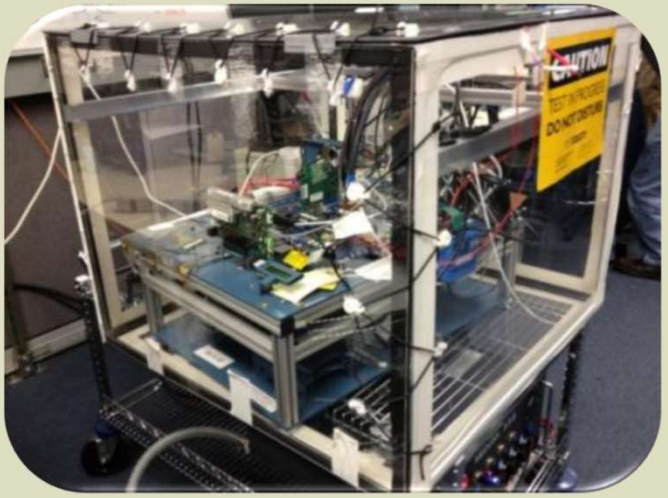
260

Innovations to Improve Efficiency

Condensation Management

Integrated local dry air chamber

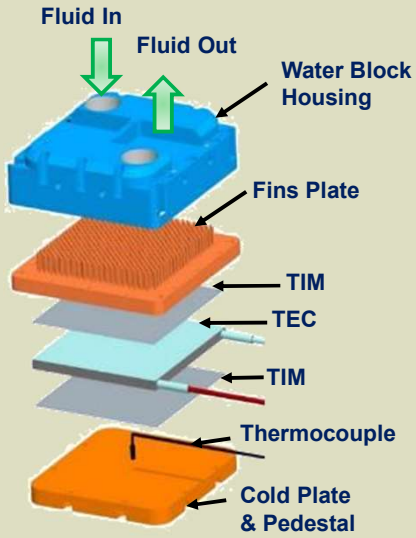


Complete system in a system dry air chamber

1. **TT has integrated dry air chamber which is enough for 0-130 C testing**
2. **System dry air box is required for -40 C testing to cover the whole system including MB**

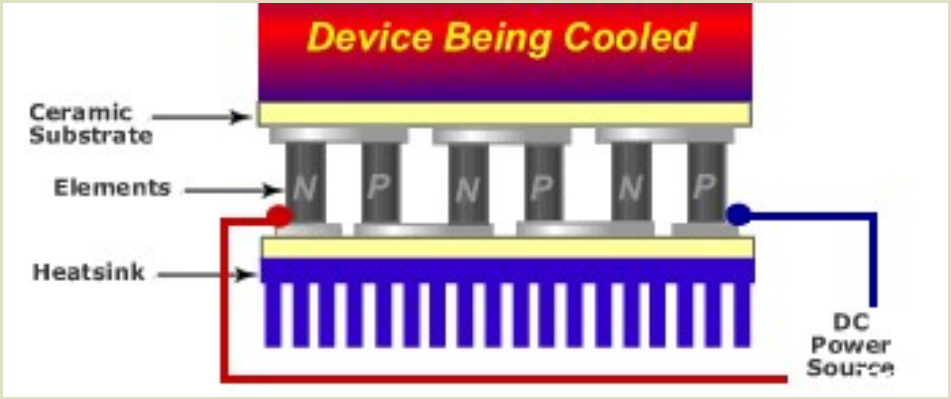
Why Are TEC Used for Cooling?

- No moving parts make them very reliable, long service lifetime
- No maintenance needed
- Ideal when precise temperature control (+/- 0.1° C) is required.
- Ability to lower temperature below ambient.
- Able to operate in any orientation.
- Compact size make them useful for applications where size or weight is a constraint.
- Ability to alternate between heating and cooling.
- Easy to be moved and shipped
- Low cost solution
- No concerns of environmental hazards



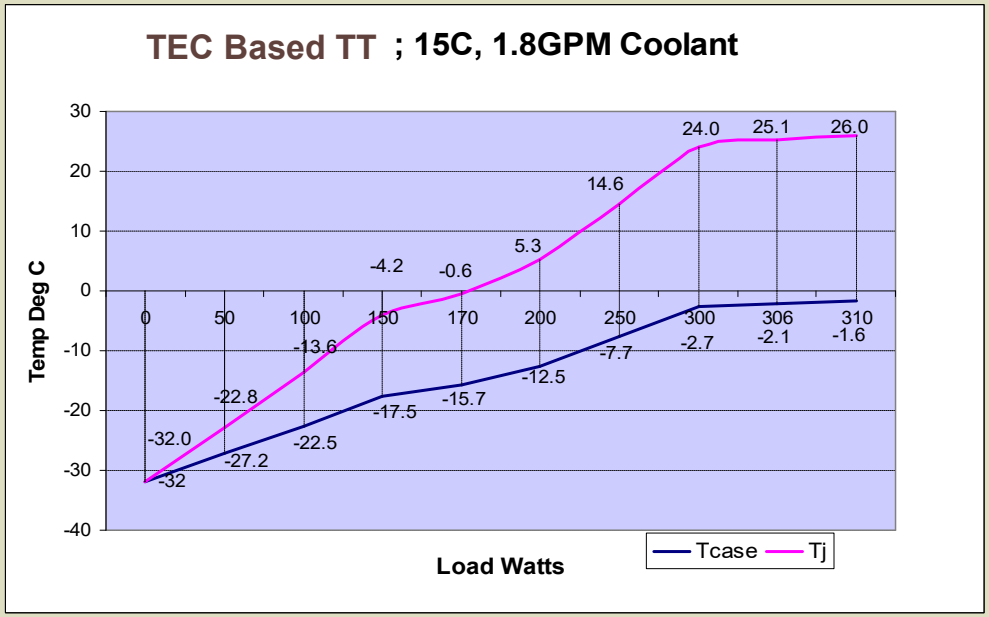
Limitation of TEC Based Solutions

- Dissipate limited amount of heat flux (low to moderate).
- Large electrical power requirements
- Lower coefficient of performance than vapor-compression systems (phase change cooling).
- More total heat to remove than without a TEC $Q_{removed} = Q_{chip} + W_{TEC}$
- Loud pumps, expensive fluids, fragile TECs.
- TEC degradation issue happens in thermal cycling tests



(Simons and Chu, 2000)

Example of TEC based TT Characterized Performance

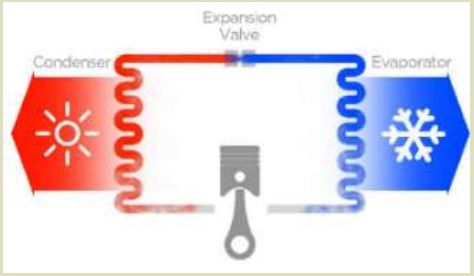


TEC based thermal tool almost reaches its capability limitation and can't meet validation requirement (0C-100 C) for high power product (400 W+) without excessively enlarging the footprint which will interfere with board components.

Phase Change Thermal Solutions

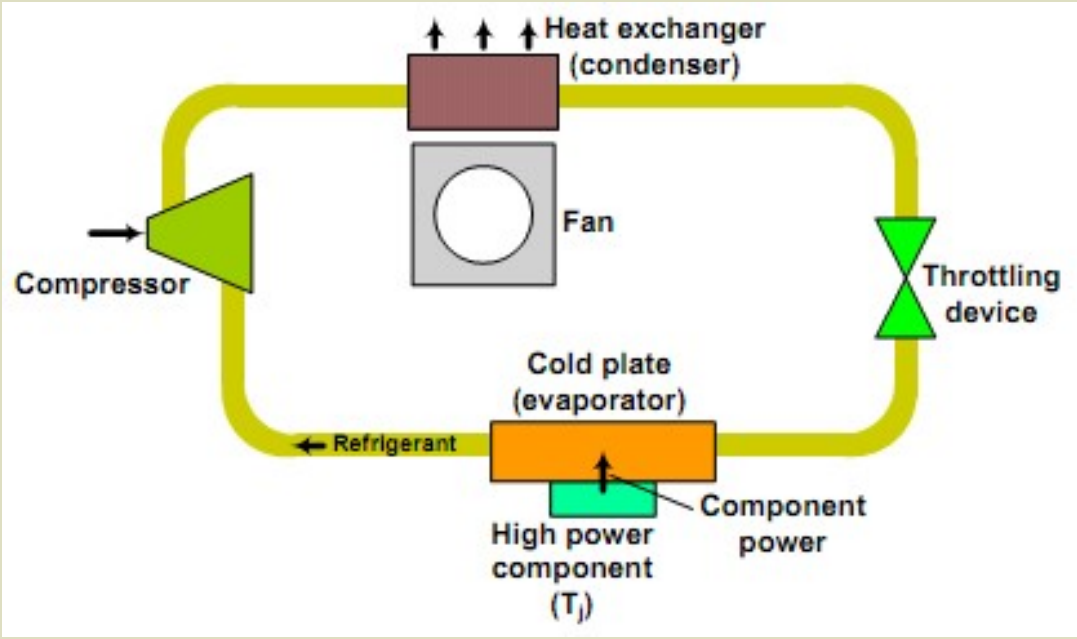
Phase Change Solution for Debug and Validation

- Provide wider thermal performance/margining than TEC based thermal tool
- Will be used for high power CPU, GPU, AI, MIC and graphics products validation test
- Enable automotive electronics to be tested to meet more stringent industrial specs -40° C to 130° C
- A smaller system can be used by cooling the DUT directly with the refrigerant.
- Energy saving by avoiding large electrical power consumed by TEC
- Maintenance is easy comparing to TEC based TT, there is no performance degradation issue



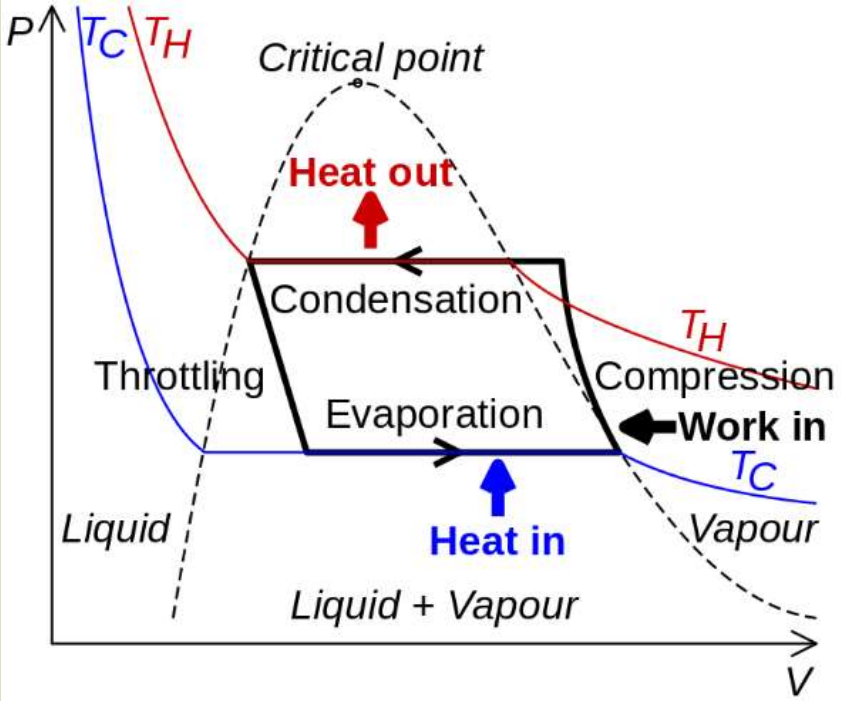
Vapor-Compression Refrigeration System

A basic vapor-compression refrigeration system consists of four major components: an evaporator, a compressor, a condenser and a throttling device.



Courtesy: ATS, Inc.

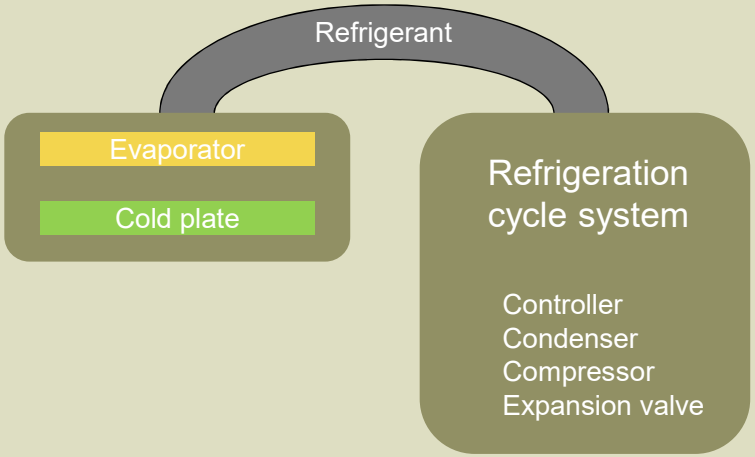
Vapor-Compression Refrigeration System

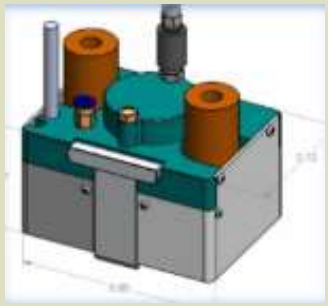


Courtesy: Wikipedia

Typical Phase Change Integrated System

Integrated system





Courtesy: Mechanical devices, Winway, Eldrotec, Sensata

Examples of phase change systems in the market

Typical Server Thermal Tool: TEC vs Phase Change

	TEC Based Thermal Solution	Phase change Solution
Power Support at 0°C [W]	0-300	0-600
Temperature range [°C]	-40 to 125	-60 to 130
Cost [$]	1.5-4 K	15-19 K
Footprint [mm^2]	80x120	70x80
Reliability	performance degrades over time	expected to work for few years
Facility support	Liquid coolant and dry air	dry air for condensation

Compared to the typical server thermal tool, Phase change provides x3 capability with the same foot print or less.

Different Phase Change Solutions Comparison

Lowest temperature at 0 W and 400 W

	Phase Change System 1	Phase Change System 2	Phase Change System 3	Phase Change System 4
400 W	-15 C	**-26 C**	15 C	-10 C
0 W	-48 C	**-60 C**	-20 C	-65 C

Maximum load at 0C and -40C setpoints

Set Point	Phase Change System 1	Phase Change System 2	Phase Change System 3	Phase Change System 4
0 C	600 W	**700 W**	300 W	460 W
-40 C	100 W	**200 W**	Can not reach -40° C	280 W

Summary

- Thermal margining of CPUs, chipsets and ASICs help Intel maintain its leadership in product reliability and Post-Si validation.
- There are more and more challenges ahead for TT development due to high power/power density product and extreme high/low temperature requirements
- Phase change technology is evaluated as an alternative solution for margining tool. It is studied for future generation of Intel processors with high power or requiring extreme low temperature test.

Closing Summary

- The topic of post-silicon validation is broad and deep - this introductory tutorial only begins to scratch the surface
- The complexity of validation and the hardware solutions needed have unique challenges which constantly must be re-evaluated due to continuing process shrinking, higher levels of integration, higher power, and larger packages
- New methods, strategies, and innovation are necessary to successfully validate future products

273

Acknowledgements

- Intel Partners
  - Aurelio Rodriguez Echevarria, Brad Friedman, Sundar Iyengar, Ying-Feng Pang, Wai Kei Pong, Ridvan Sahan, Jack Stone, Prabhakar Subrahmanyam

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1. Shehabi, Arman (2016). *United States Data Center Energy Usage Report*, LBNL-1005775. June 2016. Available at:
https://www.osti.gov/servlets/purl/1372902/

2. Tommy, Bojan (2007). *"Intel's post-silicon Functional Validation Approach"*, IEEE International High Level Design Validation and Test Workshop. December 2007. Available at:
https://ieeexplore.ieee.org/document/4392786

ADDITIONAL INFORMATION

Links to Additional Information

- Intel Roadmap for Public Products
  - https://www.intel.com/content/www/us/en/processors/public-roadmap-article.html
- Intel Platform Memory Validation
  - https://www.intel.co.kr/content/www/kr/ko/platform-memory/platform-memory.html
- Inside Intel: From Silicon to the World
  - https://www.anandtech.com/show/876/11
- Experimental Methodologies for Thermal Design in Silicon Validation Platforms
  - https://www.electronics-cooling.com/2010/07/experimental-methodologies-for-thermal-design-in-silicon-validation-platforms/#

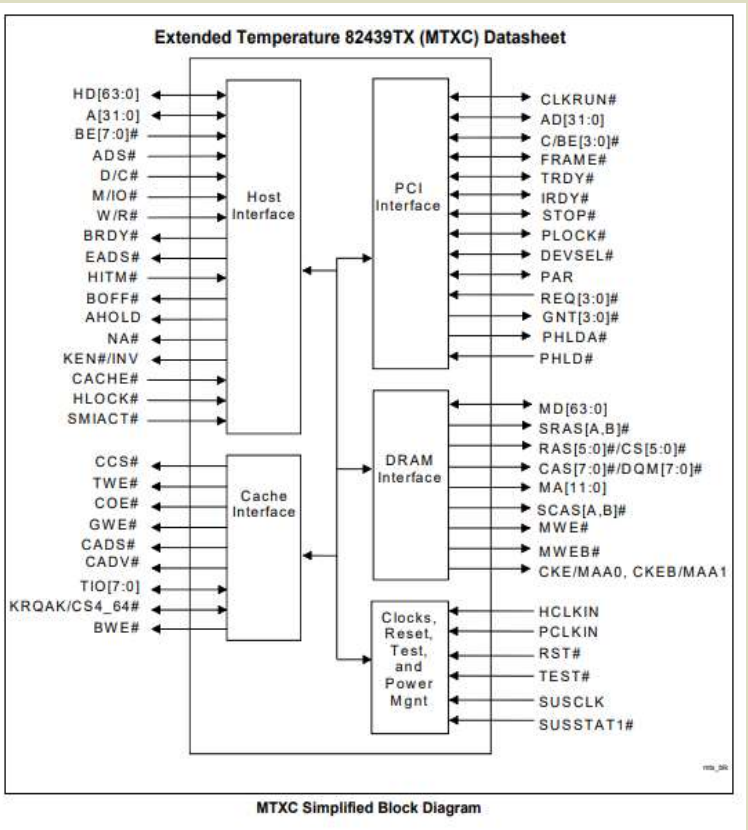
Links to Additional Information (2)

- Intel® 620 Series Chipset Platform Controller Hub
  - https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/c620-series-chipset-datasheet.pdf?asset=14618
- Intel® Xeon® Scalable Processors with Intel® C620 Series Chipsets (Purley)
  - https://www.intel.com/content/www/us/en/design/products-and-solutions/processors-and-chipsets/purley/intel-xeon-scalable-processors.html
- Flip Chip Technology
  - https://www.slideshare.net/DeepakFloria/flip-chip-technology

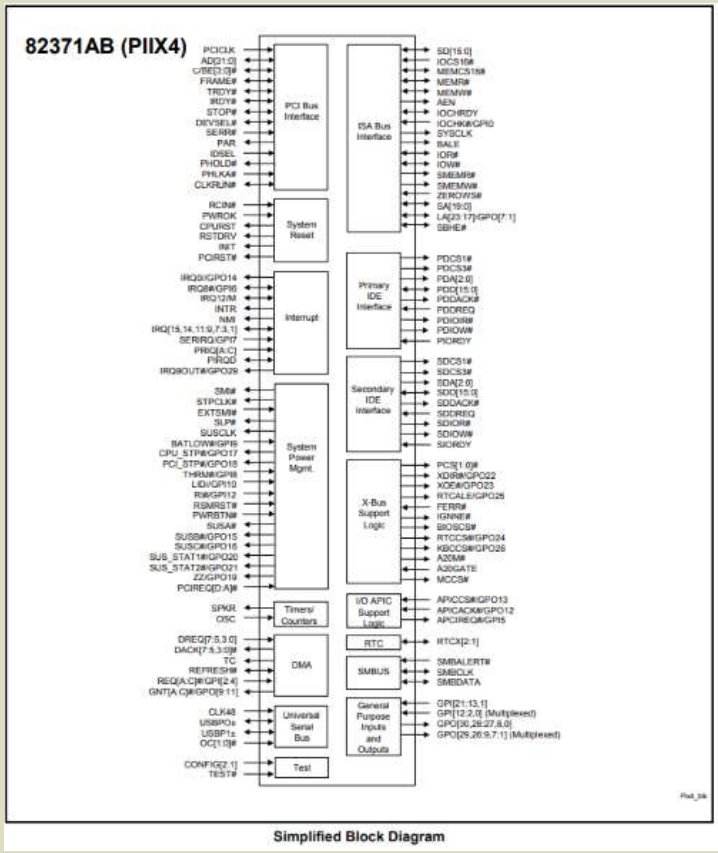
Intel® Acquisitions 2009-2017

https://en.wikipedia.org/wiki/Intel#Intel,_x86_processors,_and_the_IBM_PC

Number	Acquisition announcement date	Company	Business	Country	Price	Used as or integrated with	Ref(s).
1	June 4, 2009	Wind River Systems	Embedded Systems	US	$884M	Software	[67]
2	August 19, 2010	McAfee	Security	US	$7.6B	Software	[68]
3	August 30, 2010	Infineon (partial)	Wireless	Germany	$1.4B	Mobile CPUs	[69]
4	March 17, 2011	Silicon Hive	DSP	Netherlands	N/A	Mobile CPUs	[70]
5	September 29, 2011	Telmap	Software	Israel	N/A	Location Services	[71]
6	April 13, 2013	Mashery	API Management	US	$180M	Software	[72]
7	May 3, 2013	Aepona	SDN	Ireland	N/A	Software	[73]
8	May 6, 2013	Stonesoft Corporation	Security	Finland	$389M	Software	[74]
9	July 16, 2013	Omek Interactive	Gesture	Israel	N/A	Software	[55]
10	September 13, 2013	Indisys	Natural language processing	Spain	N/A	Software	[56]
11	March 25, 2014	BASIS	Wearable	US	N/A	New Devices	[75]
12	August 13, 2014	Avago Technologies (partial)	Semiconductor	US	$650M	Communications Processors	[76]
13	December 1, 2014	PasswordBox	Security	Canada	N/A	Software	[77]
14	January 5, 2015	Vuzix	Wearable	US	$24.8M	New Devices	[78]
15	February 2, 2015	Lantiq	Telecom	Germany	undisclosed	Gateways	[79]
16	June 1, 2015	Altera	Semiconductor	US	$16.7B	FPGA	[60]
17	June 18, 2015	Recon	Wearable	US	$175M	New Devices	[80]
18	October 26, 2015	Saffron Technology	Cognitive computing	US	undisclosed	Software	[62]
19	January 4, 2016	Ascending Technologies	UAVs	Germany	undisclosed	New Technology	[81]
20	March 9, 2016	Replay Technologies	Video technology	Israel	undisclosed	3D video technology	[82]
21	April 5, 2016	Yogitech	IoT security and Advanced Driver Assistance Systems.	Italy	undisclosed	Software	[83]
22	August 9, 2016	Nervana Systems	Machine learning technology	US	$350M	New Technology	[84]
23	Sept 6, 2016	Movidius	Computer vision	Ireland	undisclosed	New Technology	[64]
24	March 16, 2017	MobilEye	Autonomous vehicle technology	Israel	$15B	Self driving technology	



MTXC Simplified Block Diagram



Simplified Block Diagram