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TestConX 2019

Qualcomm

Test, challenges with billions of transistors, terabytes of data, 5G mobile and quality.

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Qualcomm Technologies Inc. (QTI)
March 2019

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Test, challenges with billions of transistors, terabytes of data, 5G mobile and quality.

"The world's most valuable resource is no longer oil, but data"
May 6th, 2017 The Economist.

Semiconductor data sources

Test Time | Burn in | Time to Market

Yield | Actionable data | Quality | I P Management

Data is integral to optimizing semiconductors

Test drives immense amount of data

For QTI and many others, data can be measured in terabytes per month

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- **QTI Semiconductor Landscape**
  - Major Technology Node or foundry changes every 1 – 2yrs
  - 5x more data to analyze on every new technology node (sensors, transistors, conditions, process, etc)
- Requirements:
  - Faster time to yield
  - Shorter time to root cause yield loss
  - Test, Process or Design
- Traditional methodologies do not work well due to complexity and time constraints
  - To many transistors
  - To many interactive variables
  - To much data

A treasure chest of data, but how you optimize that much data ?
Optimized databases and machine learning are some of the keys.

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Source: Qualcomm Technologies data

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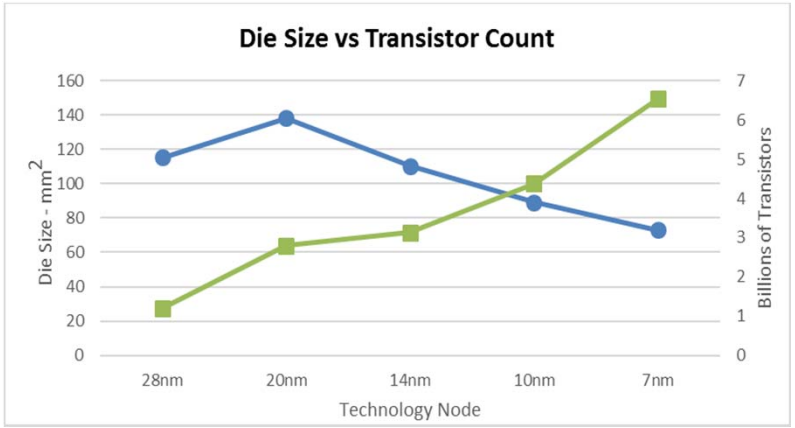
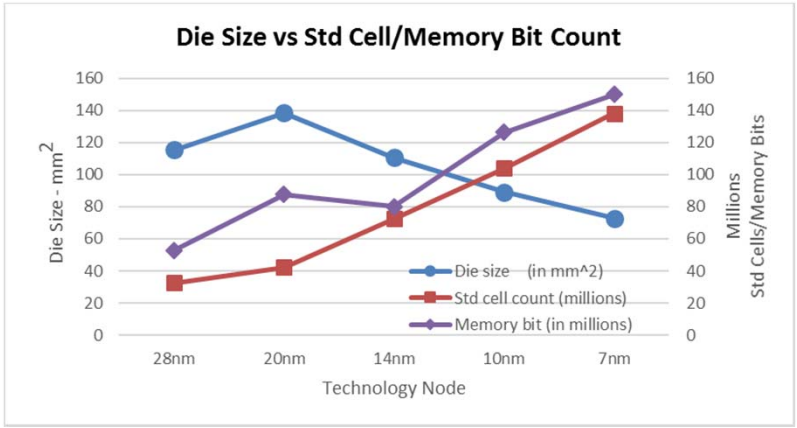
Technology Migration has Enabled Qualcomm® Snapdragon™ Mobile Platform Capabilities …….

but with some challenges.





Source: Qualcomm Technologies data

The amount of transistors has increased over 5x as die size decreased over 50%

In our products, additionally the standard cell and memory bits have increased ~ 3-4x

Source: Qualcomm Technologies data

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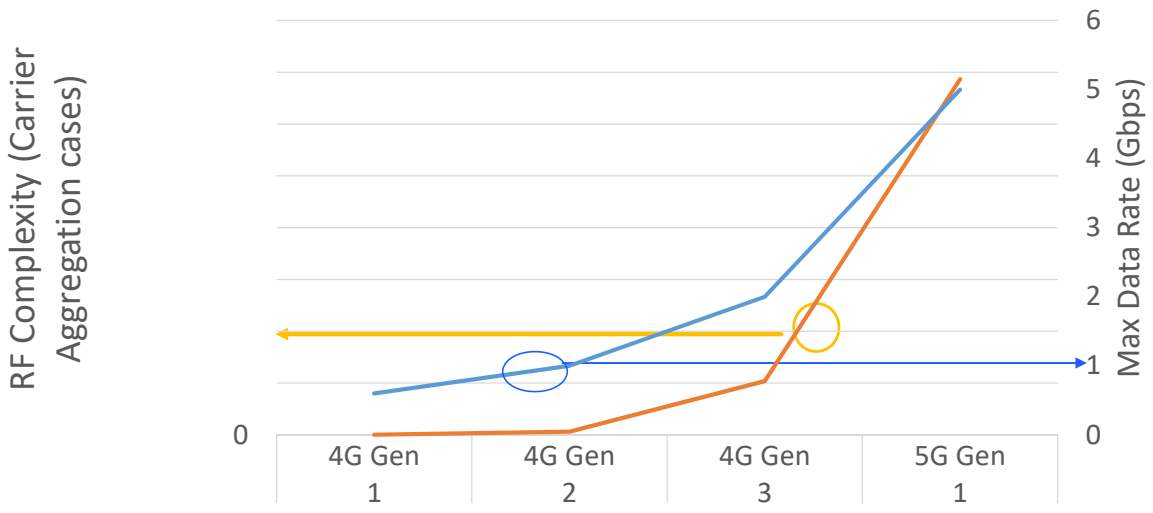
RF transceiver complexity over time



- Data rates are up year over year - more Uplink + Downlink needed to keep up with data rate needs
- Peak Data rates increased ~8x from 2015 thru 2019 while RF complexity increased >1000X.
- Result: 5G RF will more 100-1000 x data taken during characterization and potentially manufacturing

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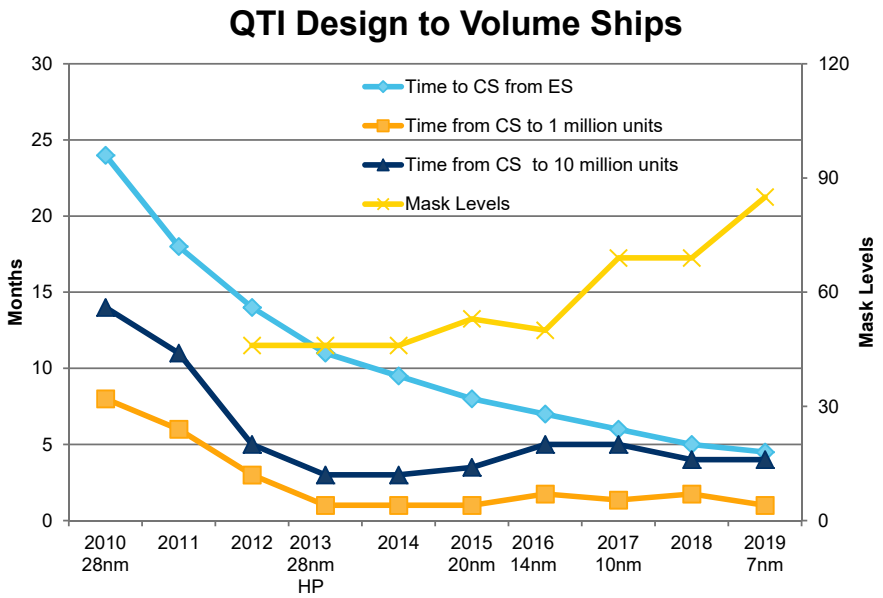
Industry demands are driving more capability and faster time to commercialization.



Source: Qualcomm Technologies data

To meet customer demands requires faster time to yield and qualifty !!

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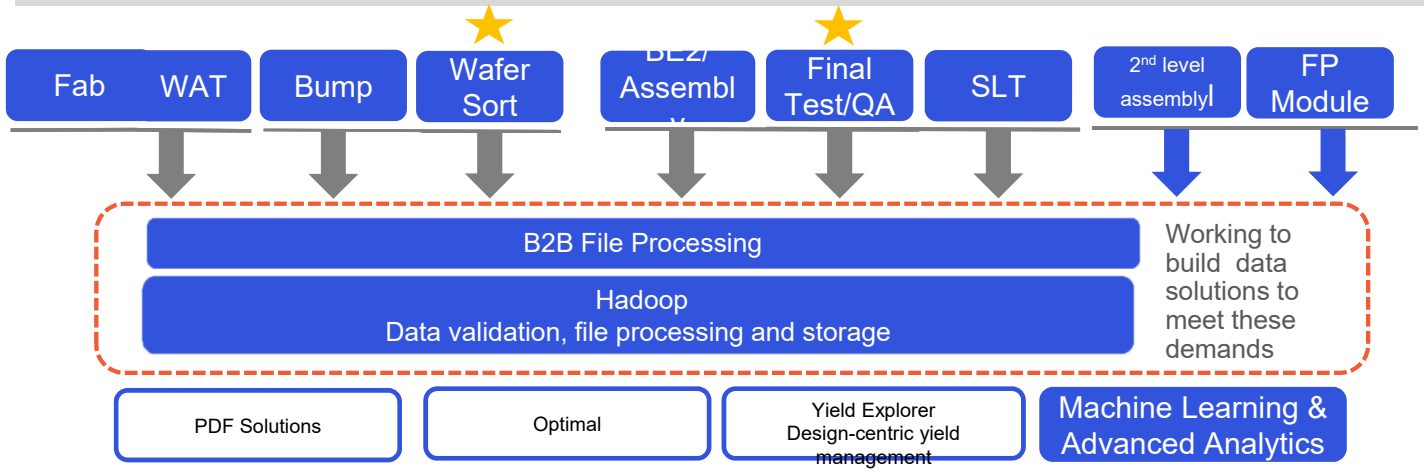
QTI manufacturing process data collection ecosystem

When does data get sent to QTI?



Smartest 8
Enabling more for advanced analytics for digital

Source: Qualcomm Technologies data

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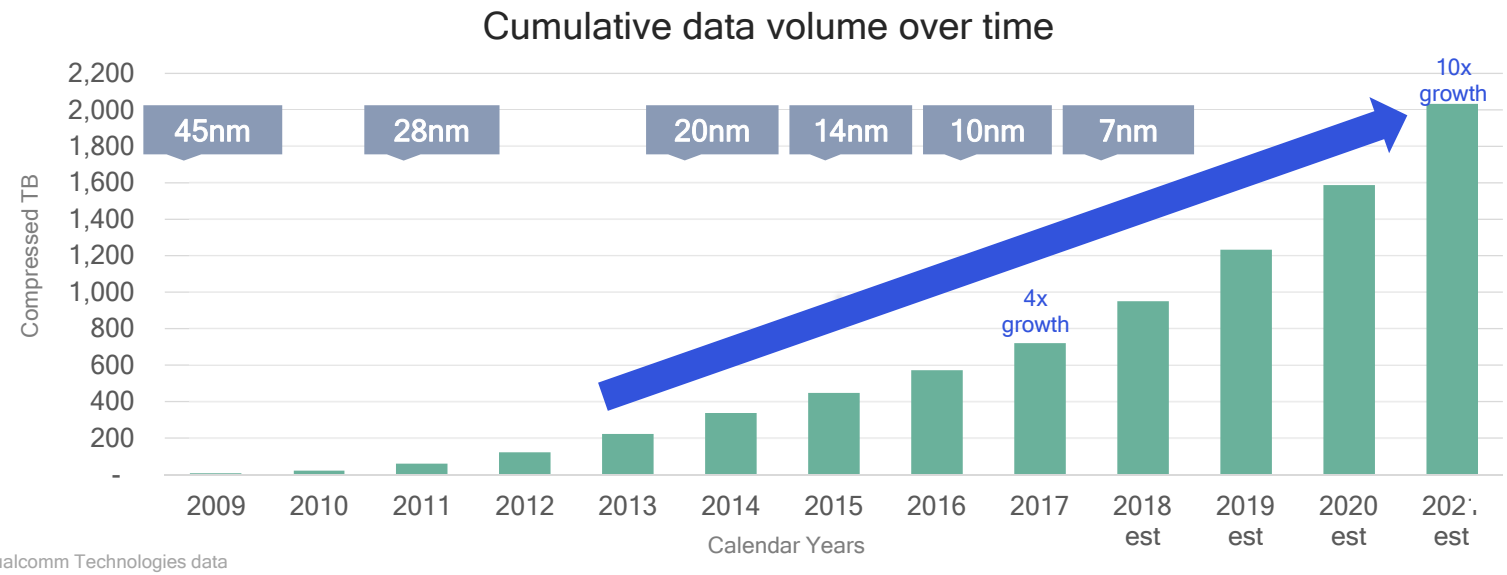
Manufacturing data continues to increase



Source: Qualcomm Technologies data

Increased design/process/test/In Line data is driving data volume.

Machine learning increasingly required to detect data shifts.

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Source: Qualcomm Technologies data

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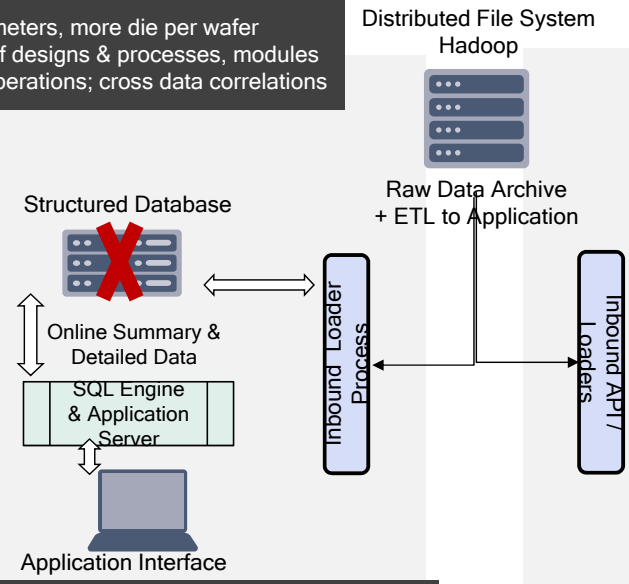
Data volume is forcing “Big Data” architectures on analytic applications

Legacy architectures can’t keep up

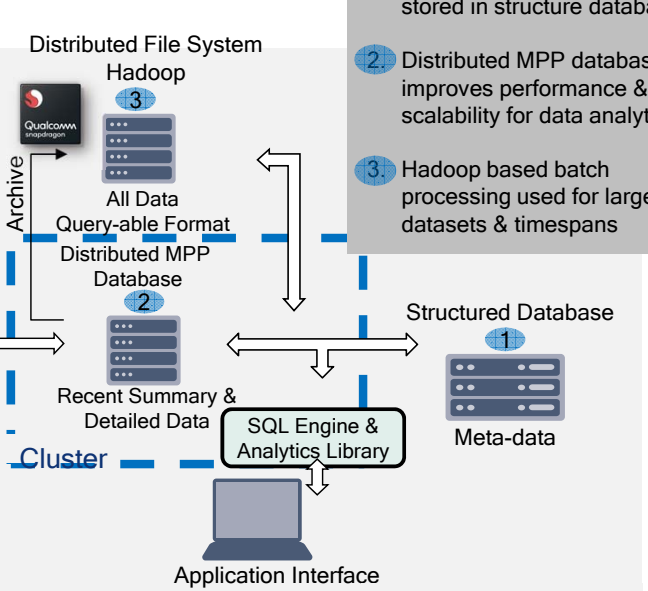
Increasing
Files sizes.. more tests, more parameters, more die per wafer
Data types.. increased complexity of designs & processes, modules
Analysis.. larger retrievals across operations; cross data correlations

Impacts
- Data volumes are too large for a traditional relational database to manage
- Data loading, database & client performance degrade
- Database becomes unmanageable
- Scaling is complex & costly



Results
- Migration to big data becomes required to maintain usability

Changes
1. Only key meta-data is stored in structure database
2. Distributed MPP database improves performance & scalability for data analytics
3. Hadoop based batch processing used for larger datasets & timespans



4months of active data ~ 80-100 terabytes of data optimized ~10% meta data; Vertica (distributed db) has ~90% of the data

The new solution - shows 2x faster load , with query performance ~6x - 10x improvement especially on the unit/device level data

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Machine Learning

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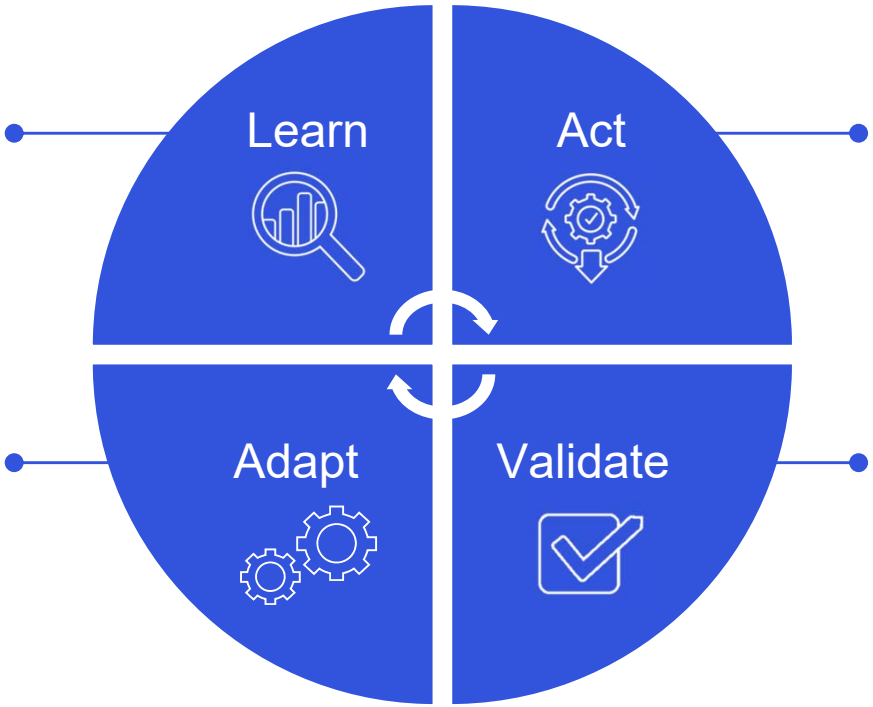
The Machine Learning Process

Use historical data to build and test a model



Deploy the model and use it to do/decide/alert on something

If model performance degrades => Refresh the model

Measure model performance as things change (all the time)

Reference from Optimal Plus.(O+)

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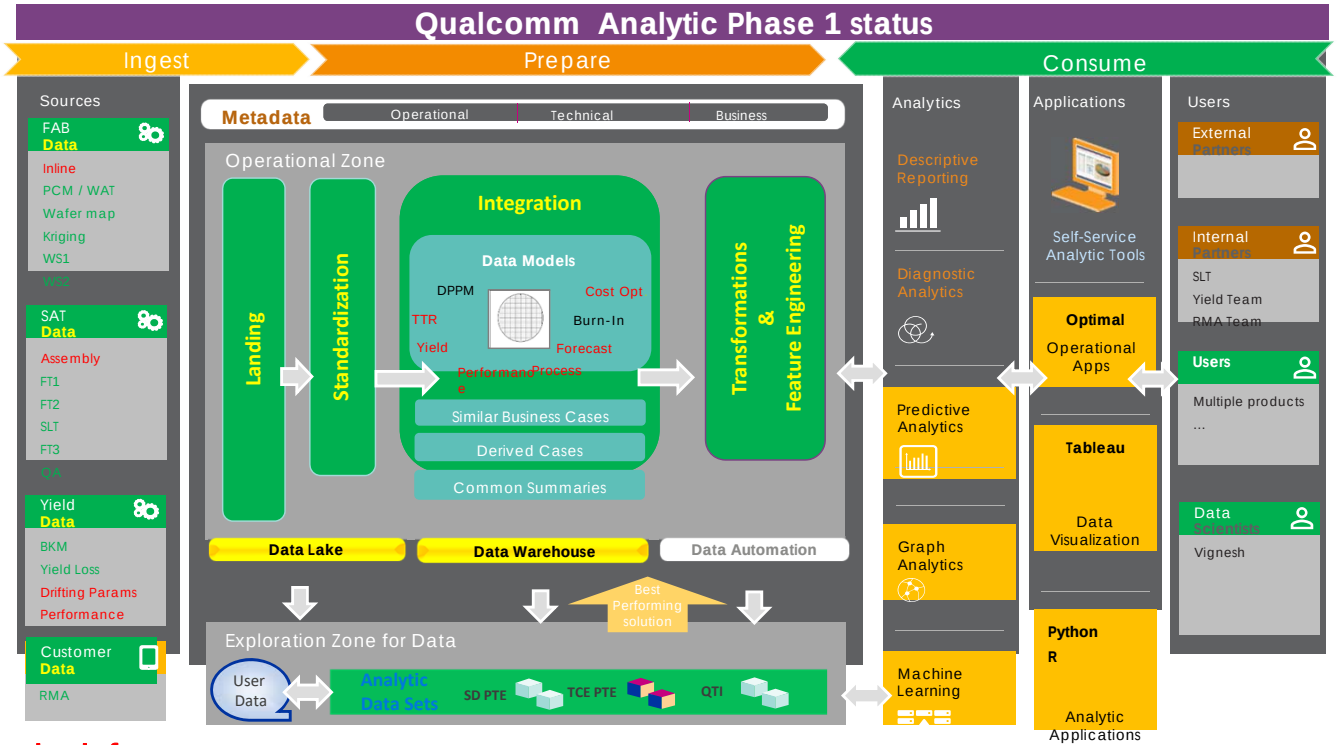
QTI Product and Test : Machine Learning System Overview



It's all about the infrastructure:

Need to have the relevant building blocks to create, validate, deploy and monitor ML models in production.

The ML code itself is only a small part of the picture.

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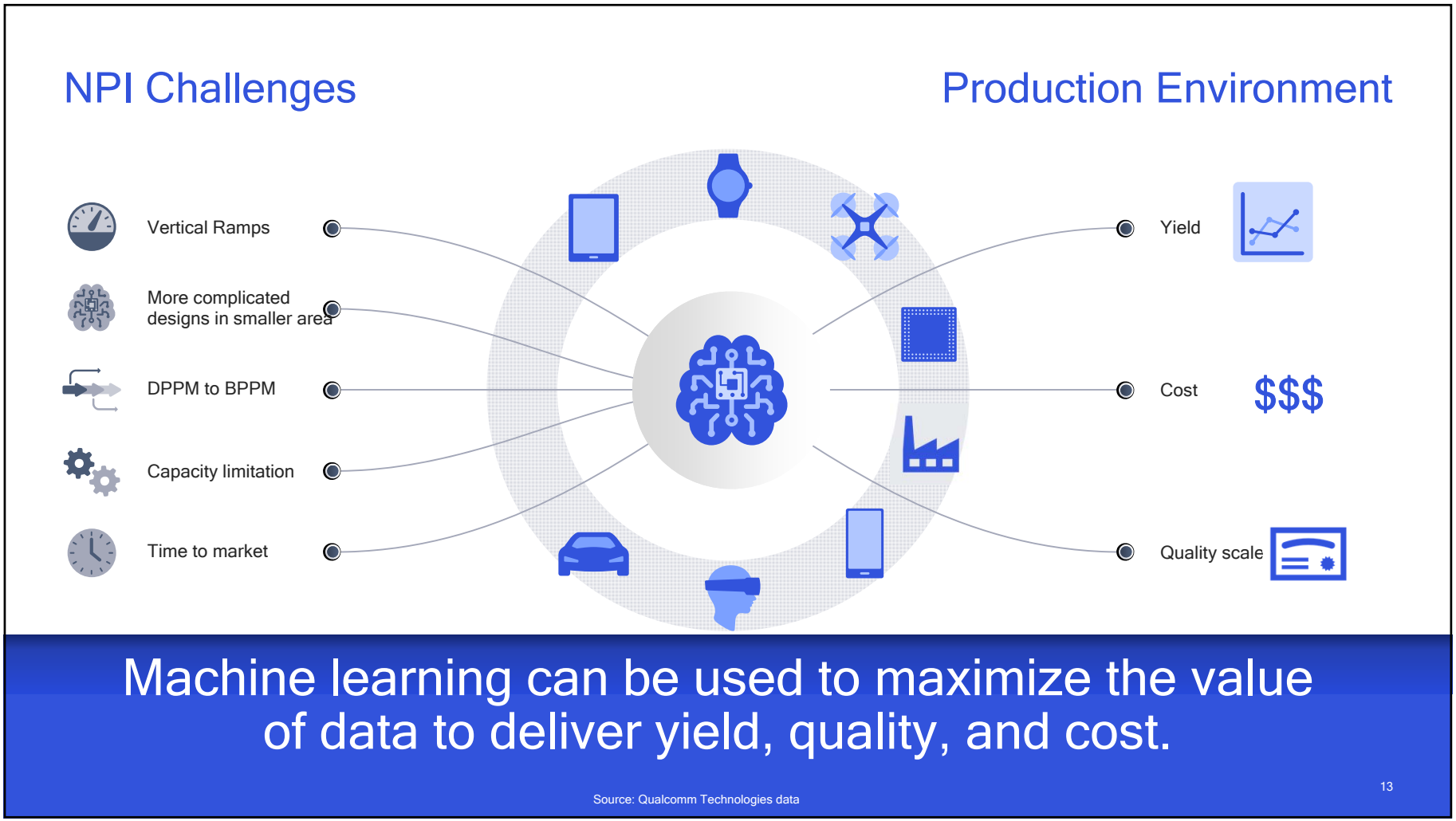

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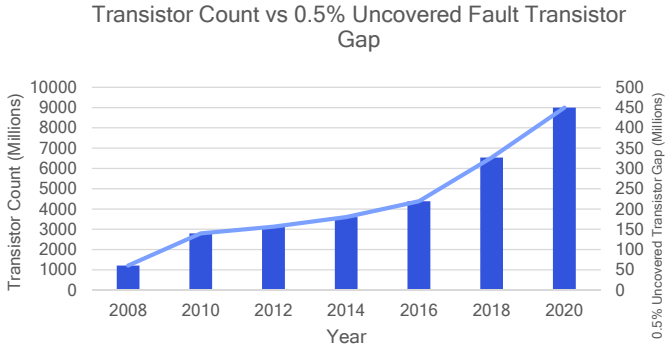
Continuous challenges…

Mobile industry is now driving toward “almost-automotive” quality levels (<< 100 DPPM)
With nearly vertical ramps in new technologies.

New technology nodes require higher number of tests:

- The 0.5% baseline fault coverage gap became TOO BIG to skip.
- EDA tools can’t cover ALL faults in production.
- New fault models are needed
- ATE Vector Memory is limited
- Higher test times constrain volume

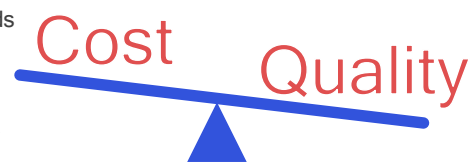


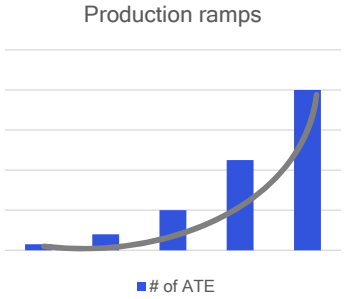
More functional tests @ NPI :

- Covering inter-block defects
- Provides gap feedback to DFT
- Helps close gap with DPPM
- Required with performance tests

Balancing Quality and Cost of Test:

- Adapt fast to higher production demands w/o quality risk increases.
- Continuous optimization of throughput capacity across family tiers.
- Live KPI monitor to guarantee all levels are met.
- Continue DFT and Test innovation solutions to address new challenges proactively.





Production Ramps are going “Vertical”

- From 9 months to 3 months in latest projects.
- No room for errors
- TTR and monitor techniques in place from day 1.
- Identify effective tests ASAP

Smarter and more adaptive test programs are needed!!

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Source: Qualcomm Technologies data

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  - Major Technology Node or foundry changes every 1 - 2yrs
  - 5x more data to analyze on every new technology node (sensors, transistors, conditions, process, etc)
- Requirements:
  - Faster time to yield
  - Shorter time to root cause yield loss
  - Test, Process or Design
- Benefits:
  - Transforms high dimensionality problems into a simplified version for human analysis
  - Self-train / adapts according to the fabrication & test conditions
  - Detects systematic patterns related to areas of interest (yield loss, marginalities, HW, etc)

A treasure chest of data, using R and python(linked to O+) can create value add data.

People drive decision based on data, ML (Machine Learning) brings value add data!

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Source: Qualcomm Technologies data

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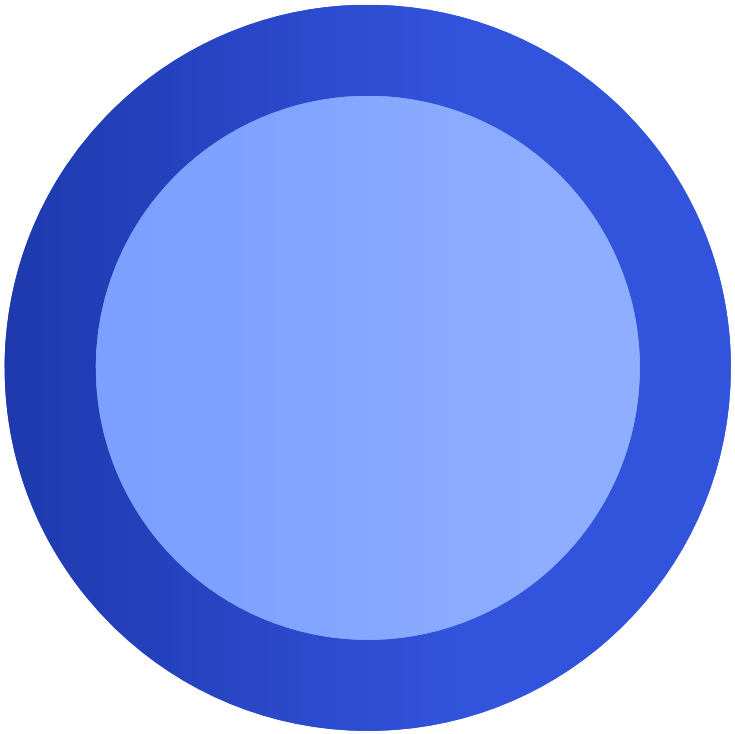
Machine learning examples

Test time and Quality



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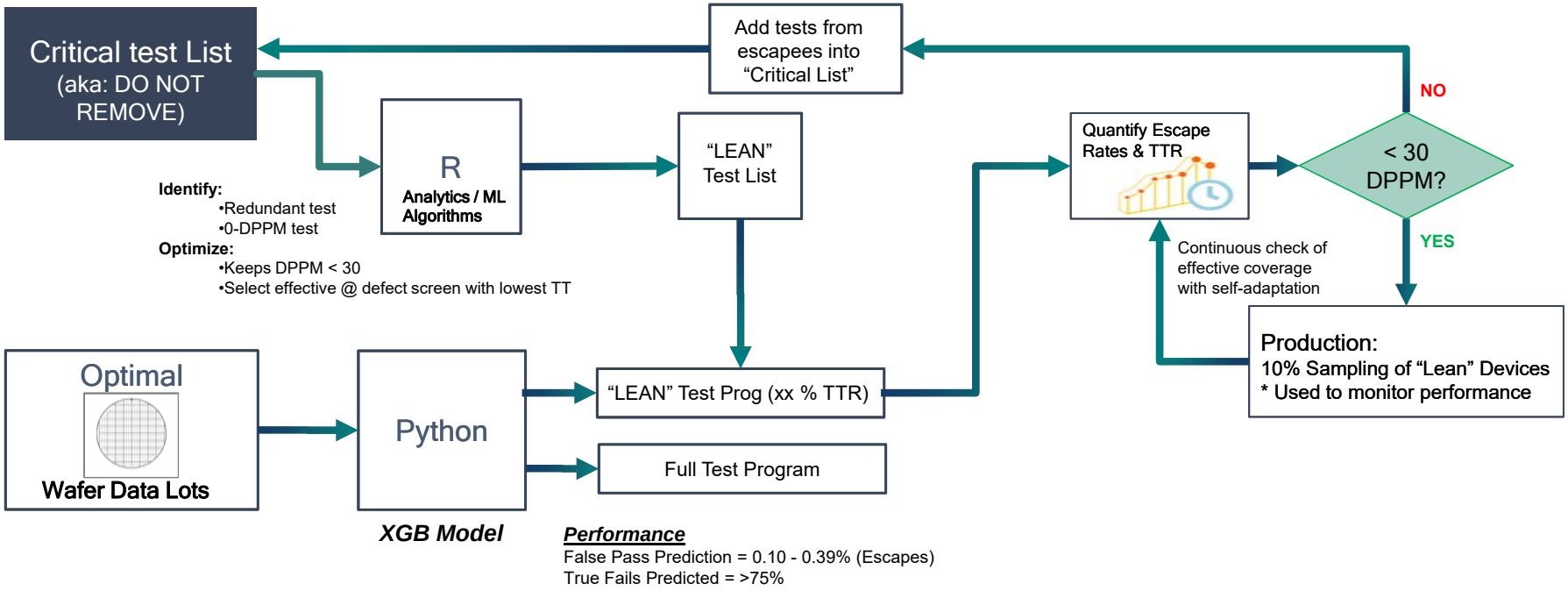
Lean coverage with machine learning- Test Optimization and predicting Quality



TTR Savings up to 20% @ < 12 Escapes / mu

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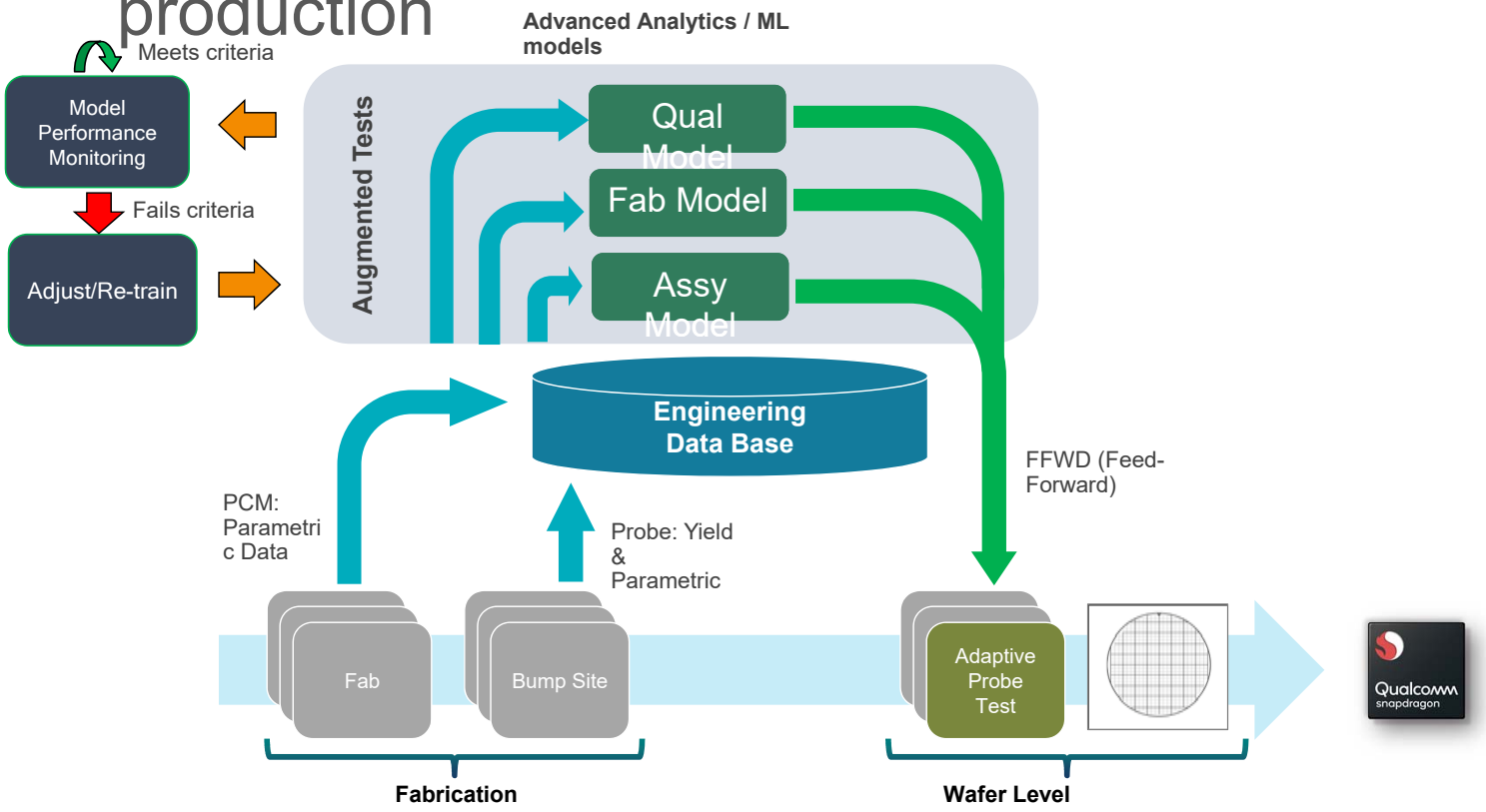
Forward Looking implementation in production



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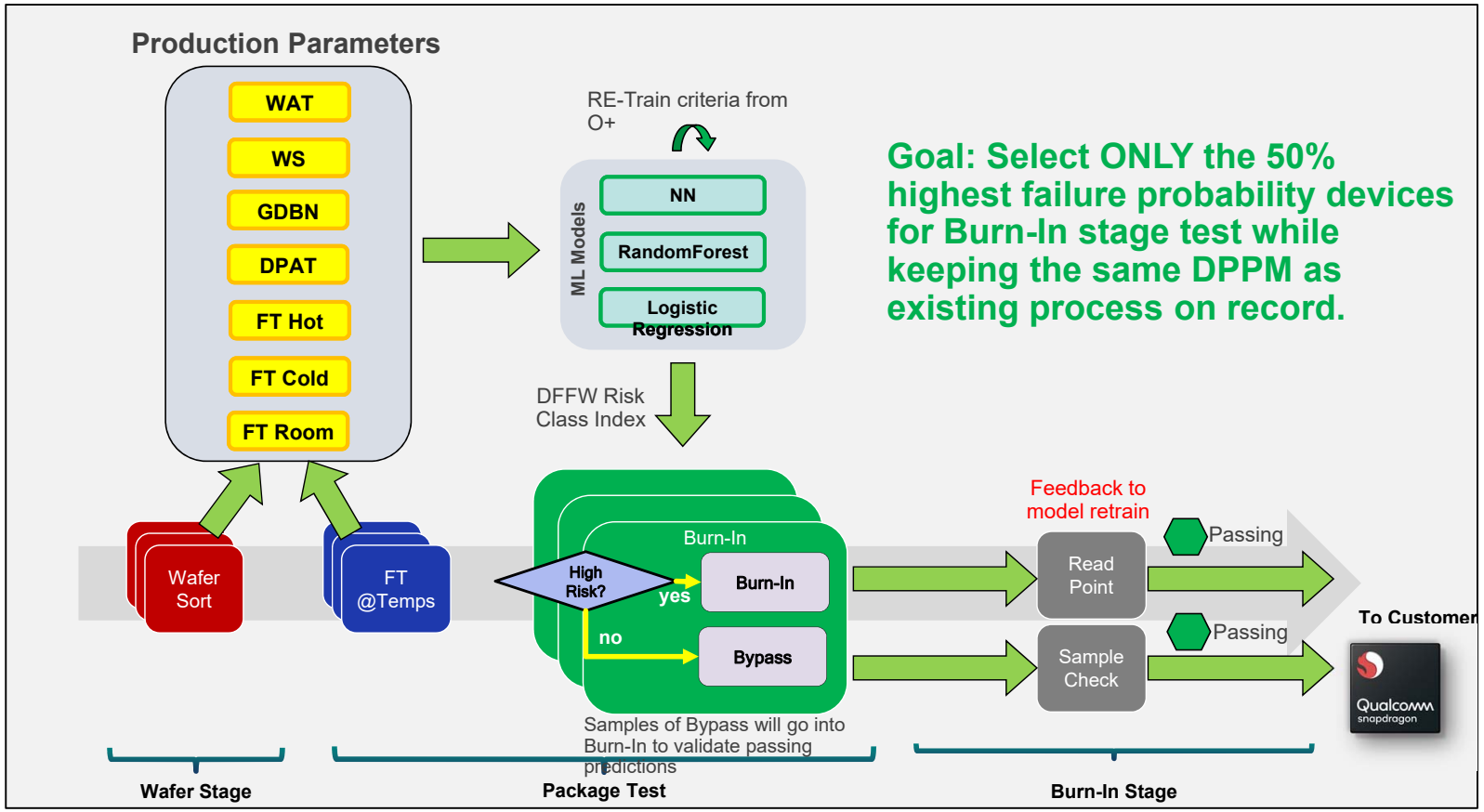
Quality - Selective devices for Burn-In



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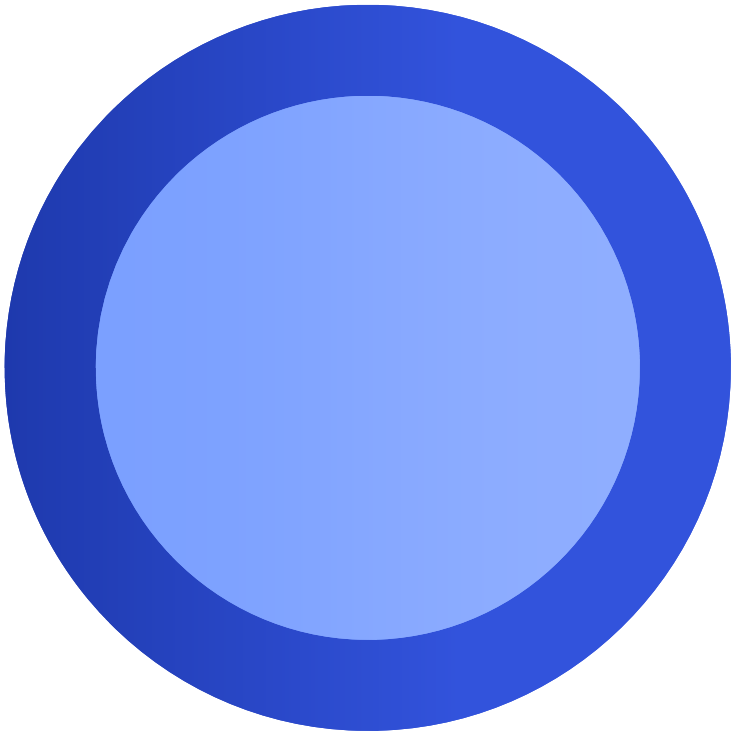
Source: Qualcomm Technologies data

DFT and fault models



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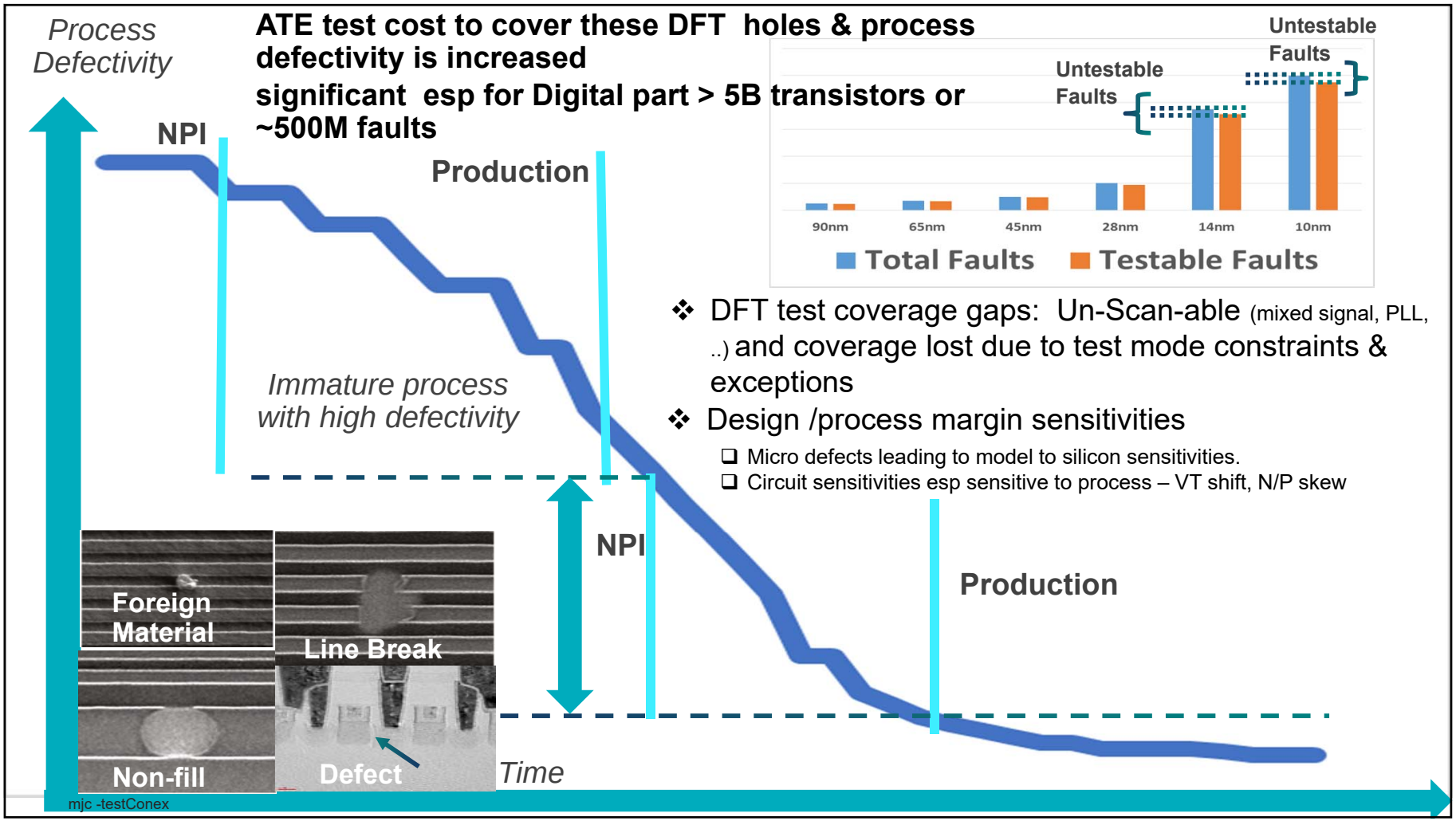

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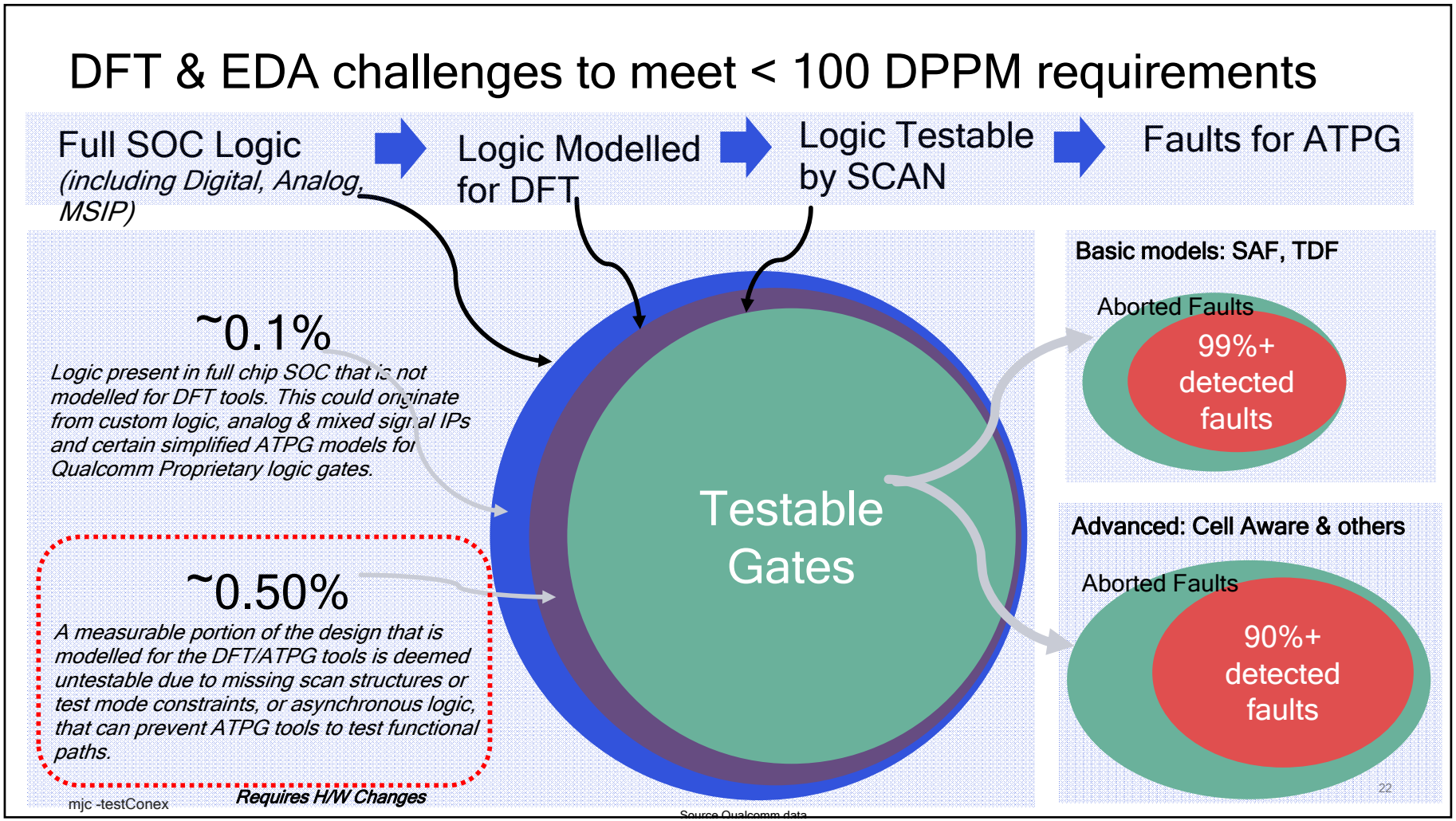

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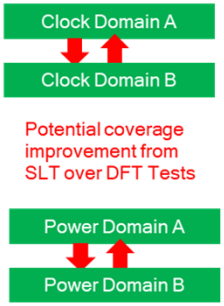
DFT & EDA challenges to meet < 100 DPPM requirements

Gaps in Test Mode Vs Mission Mode

EDA tools create tests only on the test modes as enabled by the Design & DFT architecture.

These test modes are expected to cover all functional paths, including cross clock domain & power domain paths - however, there may exist some gaps.

Limited EDA capabilities today to comprehensively analyze faults across all functional paths and highlight test mode gaps.

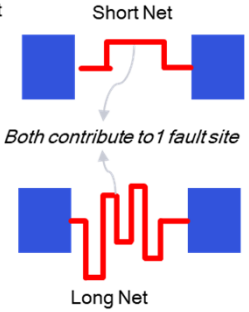


Equal Weight for all fault sites

EDA Tools assume equal defect probability and thus tend to weigh all fault sites equally.

Example: a short net and long net could have significantly difference probability of defect, however, for fault accounting, they both are considered a single fault site.

Such equal weighing of faults could skew coverage metrics and impact outgoing DPPM.

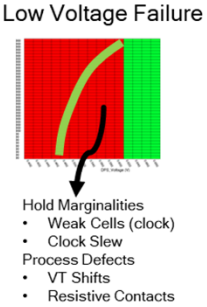


Modelling Design & Process Interactions

EDA/DFT methodologies assume ideal design margins and operate on fault models that are manufacturing defect oriented.

In advanced process nodes, Design and Process interactions are starting to cause functional path failures.

Many such functional path failures do get screened with standard DFT fault models, however, those detections are largely accidental, thus driving the need for Advanced Fault Models.

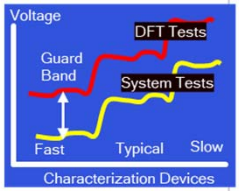


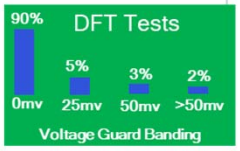
Higher Voltage Needs for DFT Vectors

EDA tools assume perfect correlation and alignment of DFT VDDmins Vs System VDDmins.

This is not always the case, especially for high performance cores at higher power corners where a voltage boost of 20mv-50mv may be required to enable tests in production.

Such Test-Only voltage boosts could escape small delay defects from the classical Fault Model oriented defect screening.



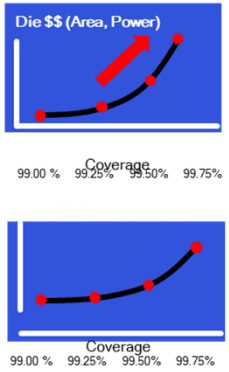


Prohibitive Cost for last 1% coverage

Significant advancements in DFT Test Compression h/w, Test Point Algorithms and best in class DFT practices have occurred in the past decade.

However, DFT (Design) cost continues to be high and increases exponentially to pick the last 1% of the fault coverage.

In addition, Test Cost (both test time and vector memory), increases significantly as coverage numbers are pushed beyond the 99% mark.

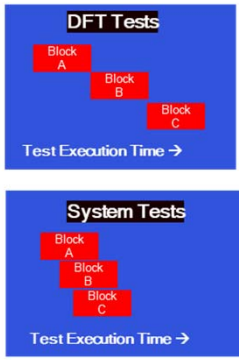


Differences in concurrency: DFT Vs SLT

EDA tools have adopted hierarchical DFT techniques to test one core at a time, unlike system tests where concurrent cores are enabled and tested simultaneously.

Such differences in concurrency between DFT and System tests put different levels of stresses and could allow for escaping subtle Power, PDN related defectivity from DFT tests.

Forward looking DFT flows are exploring testing multiple cores simultaneously, however, test power continues to be a challenge.



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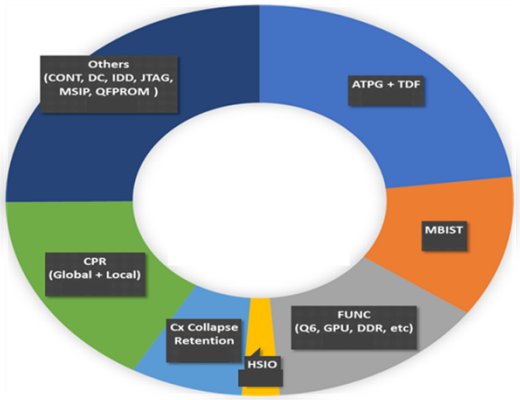
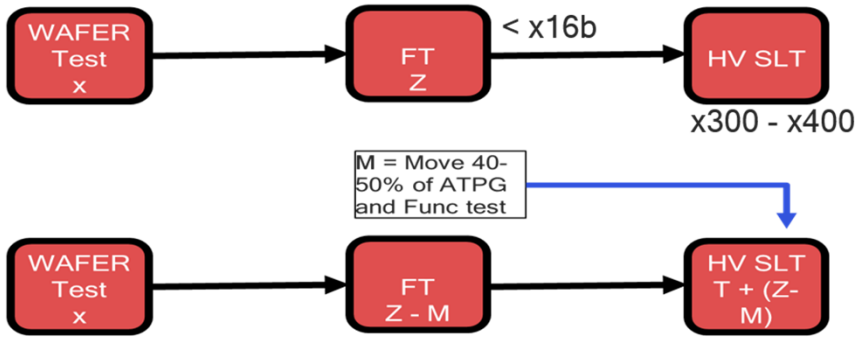
Source Qualcomm data

USB on ATE – on chip system test – cost and quality

- ATE testing for functional and Scan tests have parallelism constraints due to pins and power for complex SOC's. Incorporating a HV SLT could improve throughput and cost due to massive parallelism if enough ATE content can be moved. Test cost could reduce ATE costs while eliminating perceived DFT limitations on ATE due cost reasons. ATPG on SLT could optimize test-cost.

Hypothetical test time breakdown





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Summary

- Excel is still a powerful tool, however,
- Machine learning leverages excel, while maximizing the data reviewed and minimizes the time to value add data by > 100X.
- Machine learning DOEs have provided value add in TT, yield, and quality analysis.
- Test over USB is a way to potentially lower COT and overall cost.
- High volume SLT's may be in the cards for the future
- Automating the mundane machine learning could unleash more engineering creativity
- Lets look at one view of the future. From ITC 2018, author DR Li-C. Wang, and IEA project https://www.youtube.com/watch?v=HpajqoRdz-Q

Change – it's a good thing.

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Thank you

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