TWENTIETH ANNUAL

TestConX™

March 3 - 6, 2019

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

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Mechanical Reliability Enhancement of Ceramics for a High Parallelism Probe Card

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Introduction

BACKGROUND

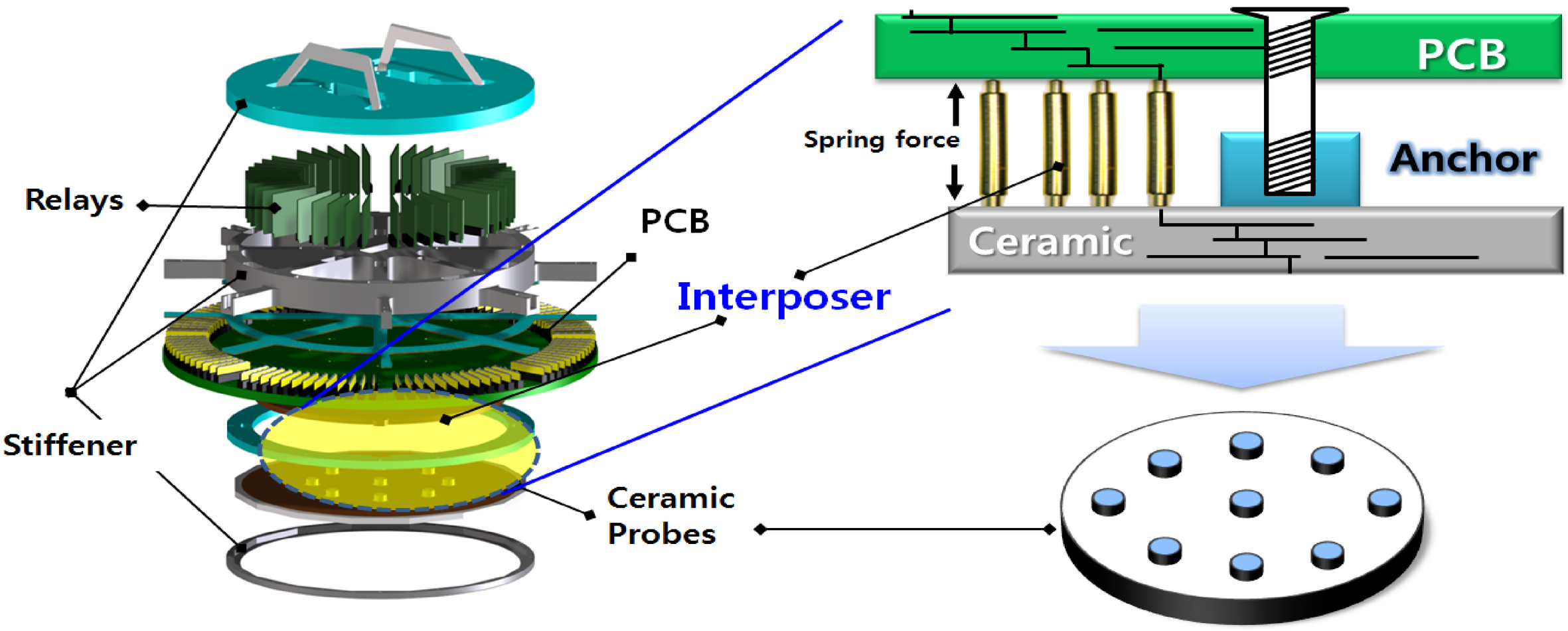
• The parallelism capacity of probe cards has greatly increased from 96-parallelism to 3,000-parallelism (96 parallelism multiplied by 32 branches).

• For this tremendous parallelism extension, about 100,000 probes and 60,000 interposer pins are used in a high parallelism probe card, which is composed of PCB and Ceramic, Stiffener, probes and interposers.

• As the number of interposer pins increases, it is more difficult to maintain the mechanical stability of a high parallelism probe card. Especially, the mechanical stress on the probe card causes damage on the anchor which is made on the surface of ceramic as shown in Fig. 1.

• In this paper, we suggest how to effectively disperse the stress on a ceramic through an optimized mechanical design and reduced number of interposer pins.

Structure of Probe Card & Anchor



[Fig.1. Structure and Binding of Probe Card]

Experiment and Solution

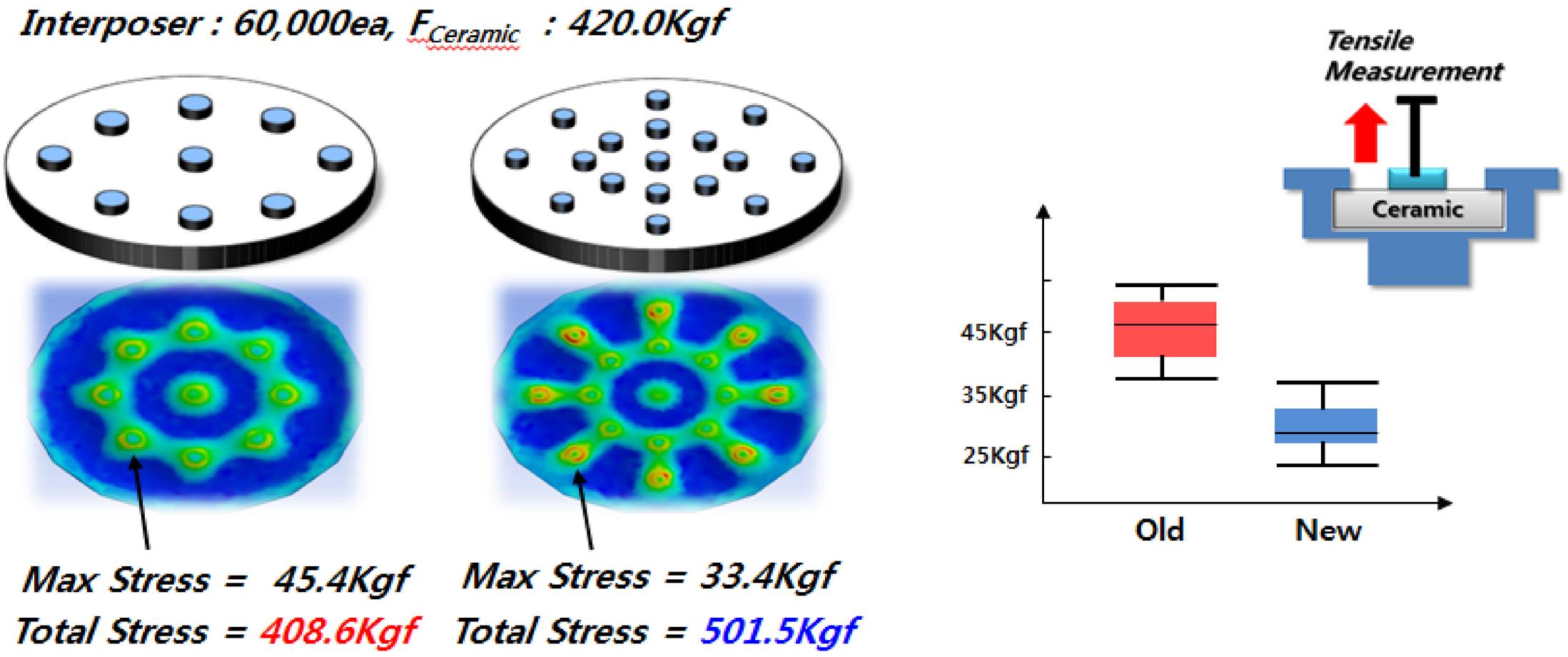
Design Optimization for Reducing Mech. Stress on Ceramic

• To secure the mechanical stability of a high parallelism probe card, the assembly structure should be elaborately designed.

• The size, number, location of anchors were decided through a mechanical simulation with an estimated force of interposers, PCB, and ceramic. In our new design, the stress of each anchor is decreased by about 25%. And it was proven through stress measurements as shown in Fig. 2.

$$\textbf{Must be } F_{\sum anchor} \geq F_{cermaic}$$

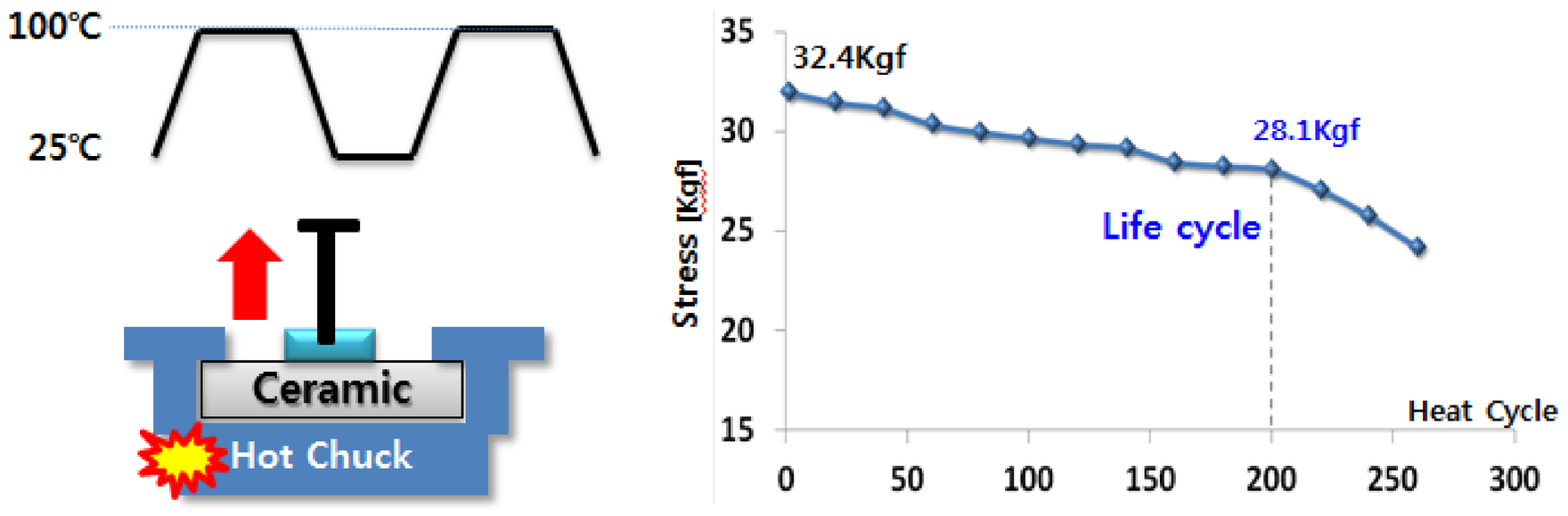
$$F_{Ceramic} = F_{interposer1} + F_{interposer2} + F_{interposer3} \cdots$$



[Fig.2 Improvement of binding between PCB and Ceramic]

• The degradation of mechanical reliability by temperature should be confirmed because the temperature of the wafer during the test processes can be as high as +95℃ and as low as -25℃.

• The heat cycle was based on the lifetime of the Probe Card, and anchor's stress resistance decreased by about 13% in repeated high temperature experiments as shown in Fig.3.



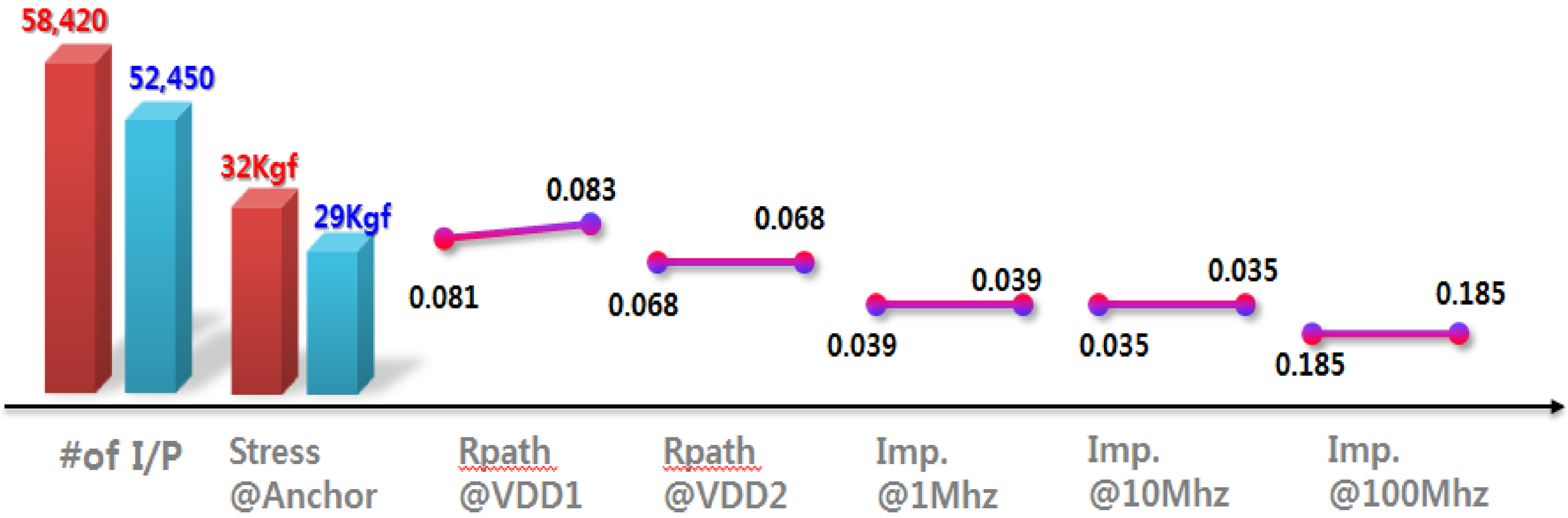
[Fig.3 Heat Cycle Evaluation in High Temperature]

Decreasing Stress through optimizing interposer pins

• In addition to mechanical design optimization, the force reduction by interposer pins has also been considered. The fewer interposer pins used, the lower the mechanical stress from the interposer.

• The risk of reducing the number of interposers pins is not high due to the electrical characteristics of the interposer. Bandwidth is about 10 GHz due to the interposer pin length of 6 mm.

• Fig. 4 shows the impact on power and ground channels when the number of interposers pins are decreased to 6,000 pins (10%). The stress is also decreased by 11% and the effect of the impedance of the power planes is negligible. Wafer test results shows no problems.



[Fig.4 The Effect of Reducing Interposer Pins]

Conclusion

• As the parallelism capacity of a high parallelism probe card increases, the mechanical stress also increases causing mechanical problems.

• Therefore, the mechanical design requires elaborate mechanical simulation under the expected stress environment to insure performance.

• In addition, as the temperature increases the reliability of mechanical design needs to be proven at these higher temperatures.

• Also, minimizing the force by optimizing the number of interposers pins should be considered. To get the proper result, electrical characteristics need to be carefully verified.