TWENTIETH ANNUAL

TestConX™

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Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

The Future of Advanced Packaging: Challenges Ahead

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

E. Jan Vardaman, President and Founder

RELEVANT, ACCURATE, TIMELY

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Industry Trends

- **Smartphones still represent large volumes, even with slower growth**
  - Drives WLP and FO-WLP volumes
  - Drives system-in-package (SiP)
- **Connectivity trends and 5G drive changes in packaging**
  - IoT drives demand for sensors
  - 5G drives new RF module designs
- **Big data analytics drives high-performance packaging**
  - Driving Si interposer and FO on substrate
  - Strong demand for HBM
  - Heterogeneous integration

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WLPs Increase Count in iPhone….

- **First iPhone contained 2 WLPs, and it was a big deal**
- **The iPhone 8 Plus contained ~60 WLPs, and it is a bigger deal**
  - One is FO-WLP (TSMC's InFO)
  - Additional 59 on main board plus WLPs in lightning cable, earbud, etc.

Source: TPSS.

2 WLPs **~60 WLPs**

iPhone 2007 **iPhone 8 Plus 2017**

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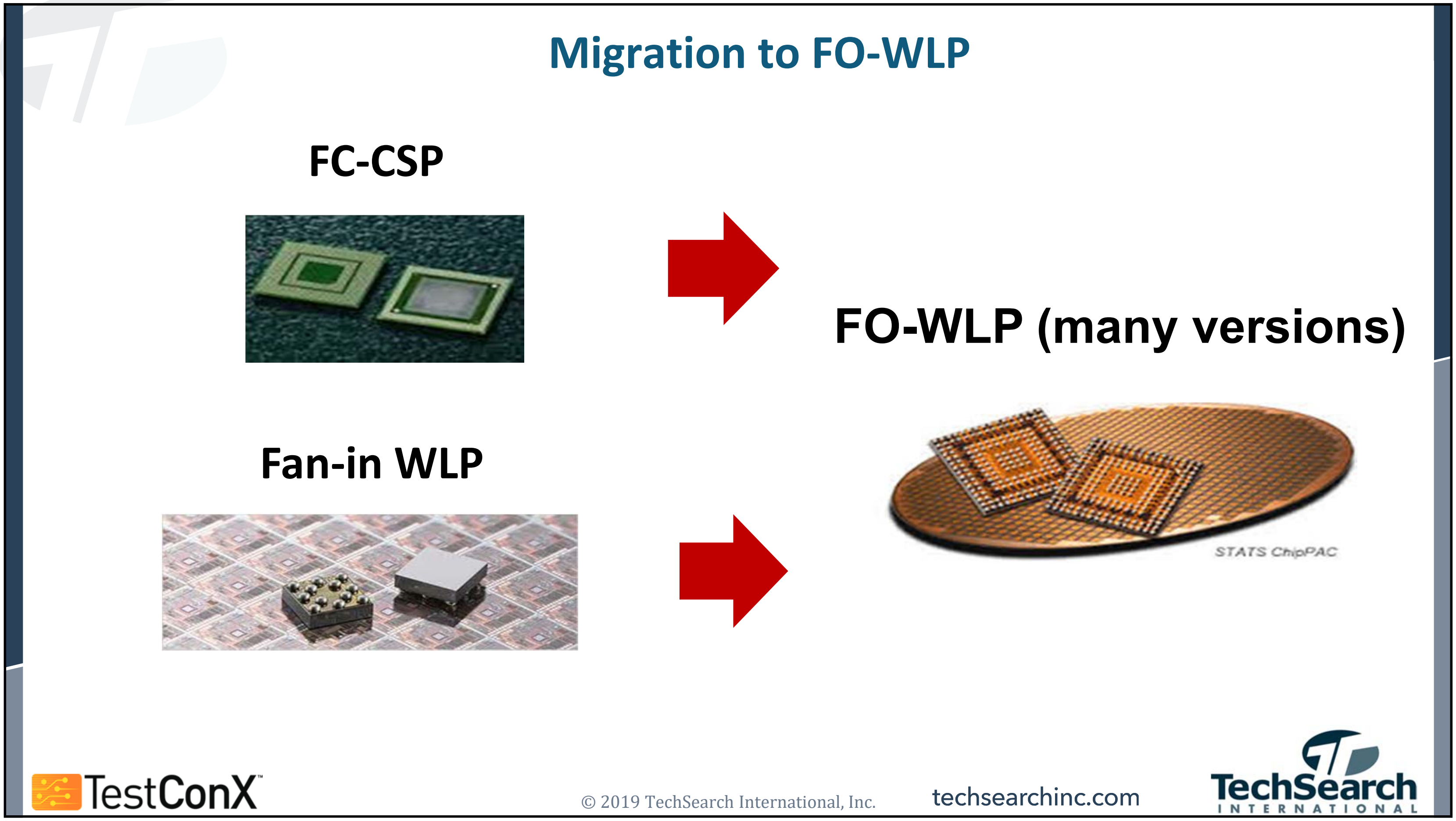

Migration to FO-WLP
FC-CSP
Fan-in WLP
FO-WLP (many versions)
STATS ChipPAC
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Why FO-WLP?

- **Smaller form factor, lower profile package: similar to conventional WLP in profile**
- **Thinner than flip chip package (no substrate)**
- **Support increased I/O density**
  - Fine L/S (10/10µm)
  - Roadmaps for <5/5µm L/S, future 2/2µm L/S
- **Split die package or multi-die package/SiP**
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- **Excellent electrical and thermal performance**
  - Future silicon technology nodes ≤ 5nm will require interconnect with greater density for high density, tight pitch Cu pillar
  - Pad pitch of < 55 µm will be required and laminate can not achieve

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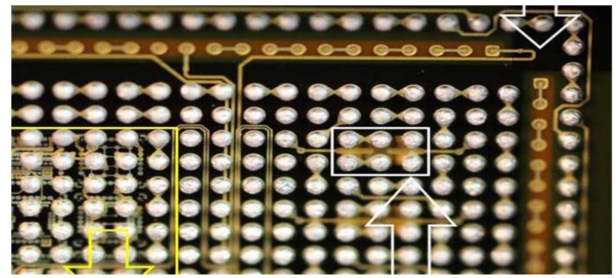
Growing Number of FO-WLP Applications

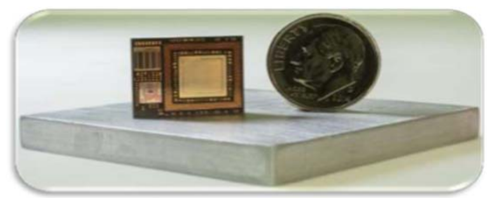
- **Baseband processors**
- **Application processors**
- **RF transceivers, switches, etc.**
- **Power management integrated circuits (PMIC)**
- **Connectivity modules (IoT)**
- **Radar modules (77GHz) for automotive**
- **Audio CODECs**
- **Microcontrollers**
- **Logic + memory**
  - Data center servers, networking, AI etc. (Fan-out on substrate)
  - Future AP + DRAM for mobile possible
- **Sensors (fingerprint, image, etc.)**
- **Many multi-die configurations**

Multidie FO-WLP



Source: Amkor Technology (Nanium).

IoT Module



Source: Nepes.

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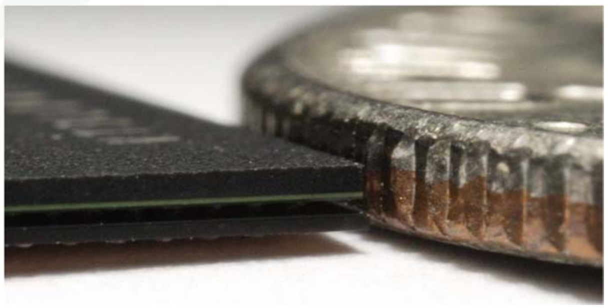
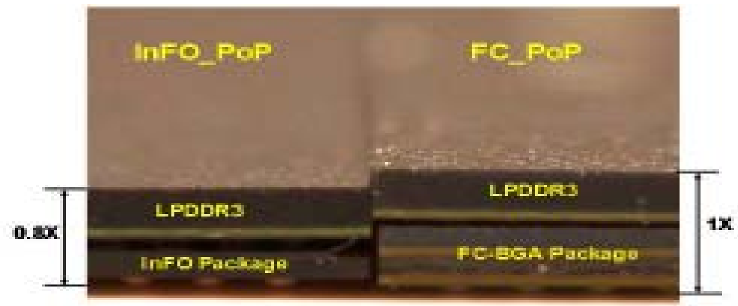
TSMC's InFO for Apple's Application Processors





Source: TSMC.

Source: TSMC.

Source: TechInsights.

- **Die-first, face-up process, RDL formed on top of Cu pillars on die**
- **Improved electrical and thermal performance of InFO vs. FC-CSP**
- **Thinner than flip chip package (no substrate)**
  - InFO-PoP is 20% thinner than FC-PoP, but thin is not only driver
  - Future silicon technology nodes 7nm and 5nm will require interconnect with greater density for high density, tight pitch Cu pillar

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Large Area Panel Processing

- **Higher throughput and lower manufacturing cost are main drivers for large area panel processing**
  - Some estimate as much as 25 to 30% cost reduction
  - Unit density increase on panel vs. that achieved on wafer lead to higher throughput (more parts)
- **Major challenges**
  - Panel warpage and handling
  - Die shift
  - How do we test and inspect in panel?
- **Material requirements**
  - Low stress materials to control warpage (less shrinkage)
  - Low-CTE materials and low process temperatures
  - Low-k polymers and low loss polymers for RF
- **Need high volume of a package that is not too small**

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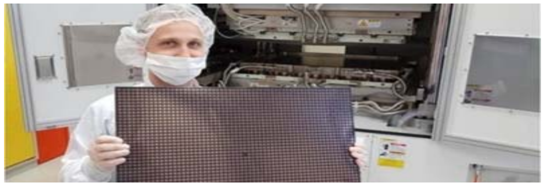
Consortia and Companies Working on Panel FO-WLP

- **Companies**
  - SEMCO in Korea
  - Nepes in Korea
  - Powertech Technology (PTI) in Taiwan
  - Unimicron in Taiwan
  - ASE/Deca in Taiwan
- **Consortia**
  - Fraunhofer IZM
  - FOPLP Consortium (ASMPT promoting) in Hong Kong
  - IME A*STAR in Singapore
  - ITRI in Taiwan
  - NCAP in China
  - Jisso Open Innovation of Tops in Japan (New)



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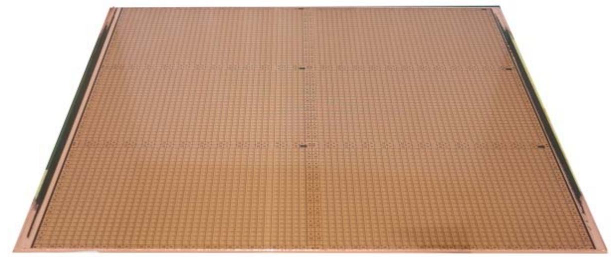
Panel-Level FO-WLP Activity

- **PTI is qualified with its panel FO-WLP line**
  - Uses chip first process
  - PMIC from MediaTek (1 RDL, 15µm L/S)
- **SEMCO in production with panel FO-WLP for Samsung Gear watch**
  - Application processor and PMIC with backside RDL
  - Backside RDL for memory stacking to form PoP
  - Thin solution
- **NEPES demonstrated panel FO-WLP for fingerprint sensors**
- **Unimicron continues R&D activity for panel**



Source: PTI.

Image courtesy of Samsung.

Source: Nepes Corp.

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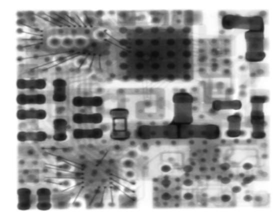
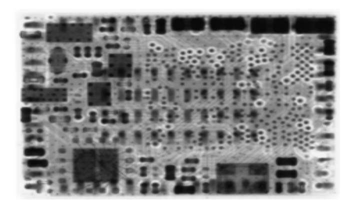
SiPs Commonly Found in Mobile Devices: Highest Volume

- **Power amplifier module (PA)**
- **Front end module (FEM)**
- **Transceiver + RF frontend**
- **Some SSDs (with controller, NAND memory, and power source)**
- **Connectivity modules**
- **Power management module**
- **MEMS integration with ASIC (this could be stacked in a QFN)**
- **3G/4G modem**

Avago PA module includes FBAR



4.4 x 4.25 x 0.88mm FLGA with 18 pads



Murata WiFi 802.11/ Bluetooth / FM Radio module

9.8 x 7.5mm LGA with 58 pads

RF module typically contains filters, antennas, and switches (CMOS and/or GaAs)

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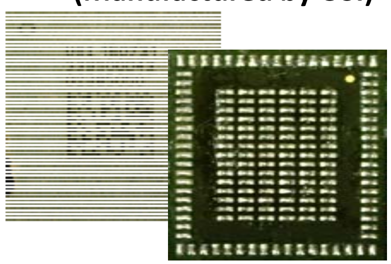
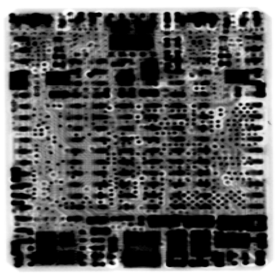
WiFi/Bluetooth/FM Connectivity Modules

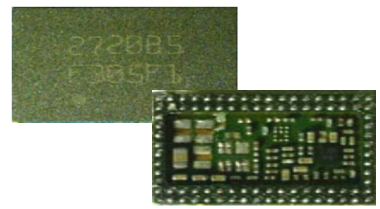
WiFi/BT/FM Module (Manufactured by USI)

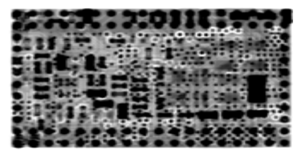




9.0 mm x 11.7 mm x 0.8 mm FLGA with 72 lands

WiFi/BT/FM Module (Manufactured by Murata)





9.3 mm x 6.3 mm x 1.1 mm FBGA with 84 balls

Source: TPSS.

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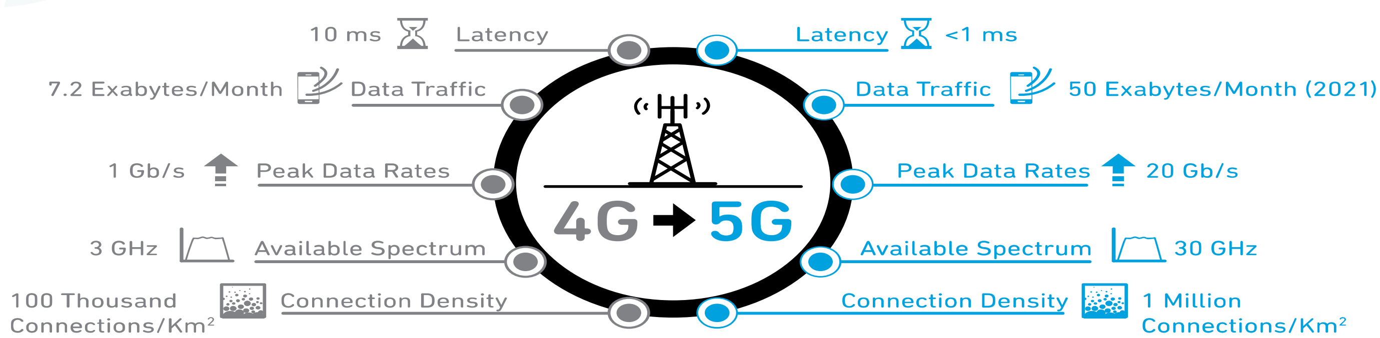
Comparison of 4G and 5G Performance and Specifications



Source: Qorvo.

- **5G promises higher data rates, lower latency, greater reliability, and larger capacity**
- **5G infrastructure is moving into place**
  - Long development cycle, 6 GHz smartphone ramp in 2019
  - U.S. focus on mmWave 28-39 GHz bands because FCC has not released sub-6 GHz spectrum for 5G at 3.5 GHz to match with ROW
  - China focused on 2.6, 3.5, and 4.9 GHz bands in 2019
- **IDC projects 200 million 5G-enabled smartphones will ship in 2022**

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Future Trends for RF Modules: 5G

- **5G New Radio offers high bandwidth, low latency, and massive scalability of 5G**
  - High-performance baseband processors
  - Broadband, steerable, and high gain mmWave antennas
  - Efficient and broadband mmWave front-end ICs
  - RF components for co-design of mmWave antennas and front-end ICs with high-Q inductors, filters, power dividers, phase shifters, and attenuators
- **5G potentially means new radios, new modems, new PA, and new FEM**
  - Greater modularization expected
  - System-in-package designs with fully integrated antenna (so antenna design capabilities are important)
  - Thermal and electrical modeling become more critical
  - Electromagnetic compatibility and EMI shielding become more important
- **Test is critical**

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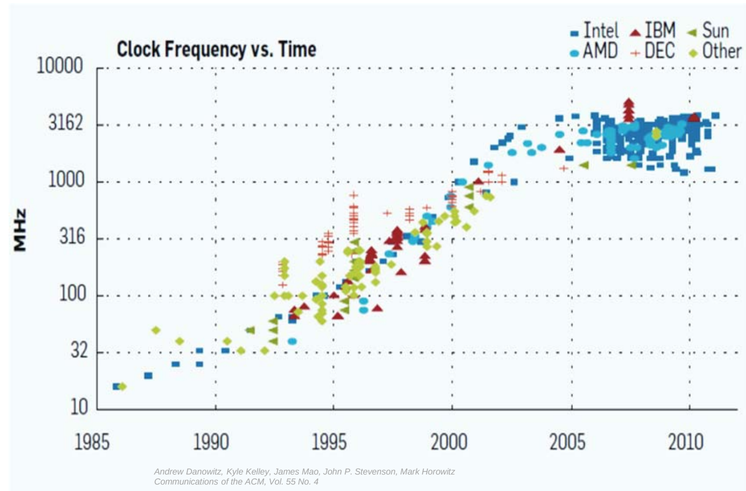
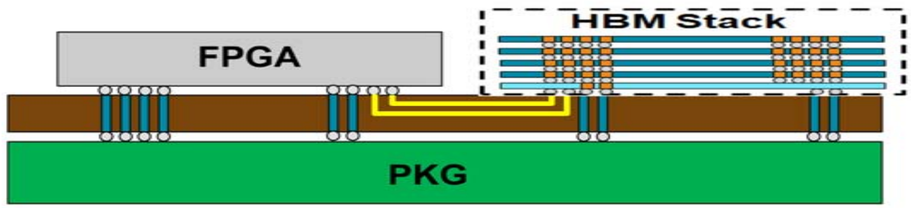
Trends Driving Heterogeneous Integration

- **With the move to each new silicon node, Moore's law (observation) has fulfilled the economic and technology promises of**
  - Density scaling
  - Speed scaling
  - Power scaling
  - Cost scaling
- **CPU architectures are not scaling**
  - Processor frequency scaling ended in 2007
  - Multicore architecture scaling has flattened
- **As the industry moves to the next silicon nodes (7nm, etc.) new packaging solutions are need to achieve the economic advantages that were previously met with silicon scaling**
- **Heterogeneous integration provides a solution**
  - Silicon interposers
  - Alternatives such as Intel's EMIB or Fan-out on Substrate



Source: Xilinx.

Xilinx Heterogeneous Integration



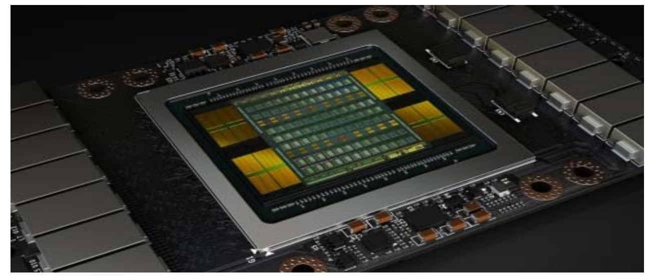
"Logic & Memory"

Source: Xilinx.

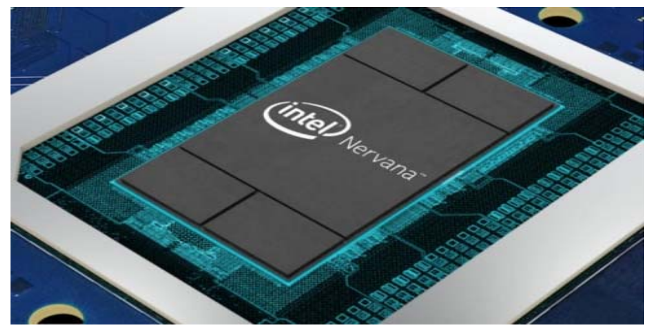
- **Silicon interposer with TSVs to handle communication between HBM stack and FPGA**

What's Driving Demand for Si Interposers?

- **AI accelerators in datacenters to increase to 50% by 2020**
- **Network systems**
- **Graphics market**



Source: NVIDIA.



Source: Intel.

AI Accelerators Using Heterogeneous Integration

- **Logic and high capacity memory as close as possible to provide low latency and lower power**
  - Use of large die (up to 28 mm x 28 mm) with high I/O counts and micro bumps
  - Use of HBM with wide bus (1,024 I/Os, ~4,000 bumps, 55µm micro bump pitch)
  - Mount on silicon interposer with TSVs (or high-density alternative) with as small a gap as possible, TCE matched to provide good reliability for logic die with ELK
  - Silicon interposer mounted on laminate substrate with C4 bumps (~130µm bump pitch)
- **Si interposers provide a high-density routing connection between logic and memory**
  - Silicon interposers are the only solution ≤1µm for routing today

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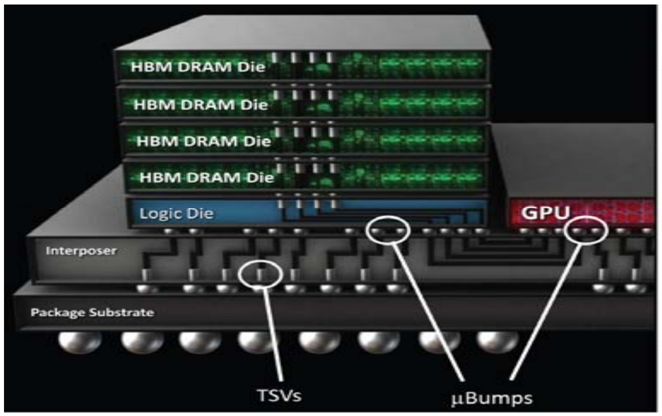
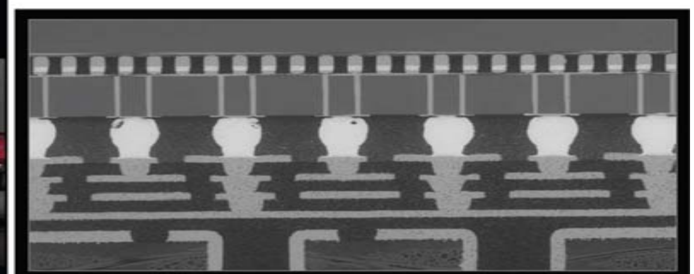
AMD's "Fiji" with Silicon Interposer and HBM





Source: AMD.

- **AMD "Fiji" solution for the graphics market**
- **Four HBM stacks, each containing stacked DRAMs and a logic die with TSVs mounted on a 1,011mm^2 Si interposer**
  - Approximately 200,000 interconnects in the module including Cu pillar microbumps and C4 bumps
  - Si interposer has 65,000 TSVs with 10µm-diameter vias

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Test Strategy: Key To AMD Success

Source: ASE and AMD.

- **Wafer sort (important to consider probe tip, pad size, and control of probe mark)**
- **Partial assembly test (unique to this application, LGA pad surface finish, contact force control, yield repeatability, and contamination control)**
- **Final test (thermal management important)**

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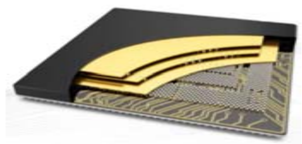
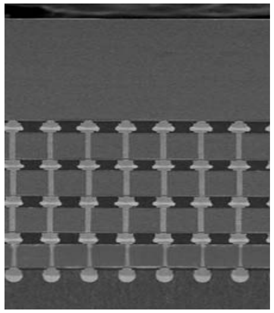
3D IC: Memory Stacks with TSV

- **Tezzaron high-speed memory**
  - High-performance applications shipped
- **Samsung RDIMM with stacked memory for servers**
  - Modules delivered in Sept. 2014, in production in 2015
  - DRAM stacks with TSVs
- **SK Hynix (HBM)**
  - Stacked die mounted on interposer
  - GPU, etc. applications
- **Micron HBM…coming soon**



Source: Samsung.



Source: SK Hynix.

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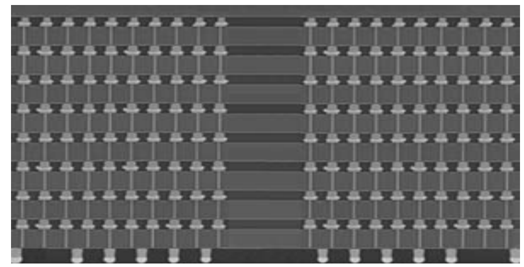
HBM Test and Test Vehicle Development

- **Stacked die with TSVs requirements**
  - Well joined TSV/micro bumps
  - Well aligned micro bumps
  - No underfill delamination or voids
- **Test vehicles TSV stacked memory**
  - Robustness of TSVs and micro bumps important
  - All test patterns electrically tested in test vehicles
- **Bump pitch**
  - Bottom die bump diameter 25µm
  - Bottom die bump pitch 55µm staggered for HBM versus 100µm for HMC
  - Bump pitch between die 40 µm (Cu pillar)



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Nokia's FP_4 with Si Interposer and Memory

- **First 2.4Tb/s network processor**
  - Uses Si interposer and HBM
  - Occupies one-fifth the board space of the previous generation of FP silicon
  - 22 dies – 1 packet processor ASIC, 16 memory, 4 MAC chips + interposer
  - Uses TSMC 16FF+ for ASIC
  - Cuts power consumption in half (per Tb), up to 250% greater port fan-in/fan-out.
  - Assembled with TSMC's CoWoS process

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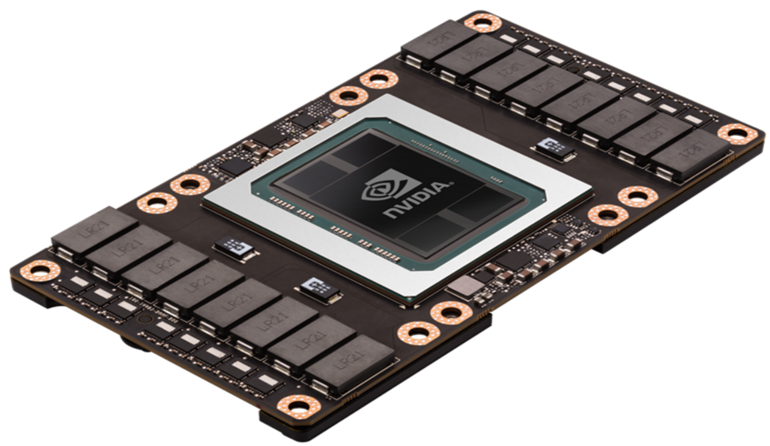
NVIDIA’s GPU + HBM

- **NVIDIA’s GPU with Cu pillar mounted on a 100µm-thick silicon interposer with TSVs using TSMC’s CoWoS process**
- **Four HBMs with 8 DRAMs per stack plus logic layer are also mounted on the silicon interposer (HBM with 55µm pitch)**
- **Silicon interposer is mounted on a 55mm x 55mm laminate substrate with 130µm pitch C4 bumps**



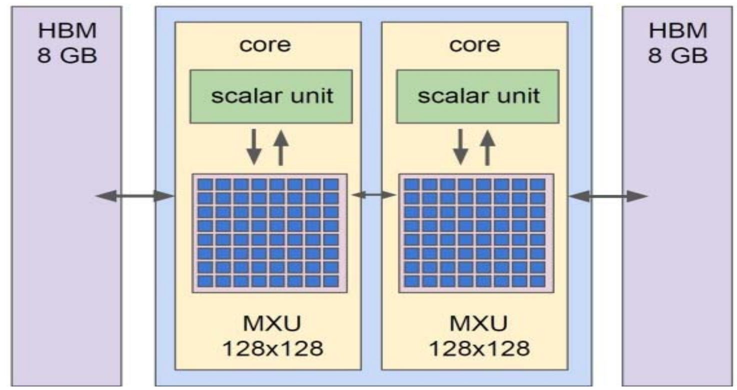
Xilinx VIRTEX UltraScale+™

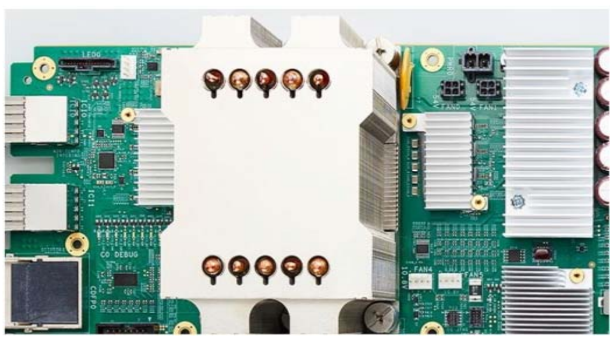
- **VIRTEX UltraScale+™ silicon interposer with TSVs**
  - Interposer as large as 30 mm x 36 mm
  - Metal line stitching used for larger than reticle interposer products at <1µm pitch
  - 3 Cu metal layers plus 1 Al layer
  - Dual damascene process used to form vias and diameters
  - ~0.4µm lines and spaces
- **Approximately 660,000 interconnects in the module**

Source: Xilinx.

Google Tensor Processing Unit v2 with Interposer and HBM

- **Google-designed device for neural net training and inference**
  - 16 GB of HBM
  - 600 GB/s memory bandwidth
- **ASIC + HBM on Si interposer using TSMC's CoWoS**





- **Version 3, introduced in May 2018, doubles the HBM**

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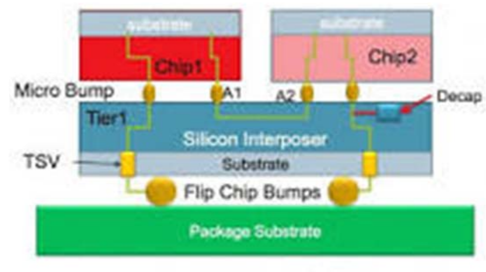
Drivers for Silicon Interposers

- **Demand for higher performance, lower latency in computing solutions**
  - Fast random-cycles and low latency/power memory access are required
- **Si interposers provide a high-density routing connection between logic and memory**
  - Applications such as networking systems, big data processing, cloud computing, and machine learning (also called artificial intelligence) require high-density routing
  - Silicon interposers provide fine features for communication between chips (< 1µm L/S)



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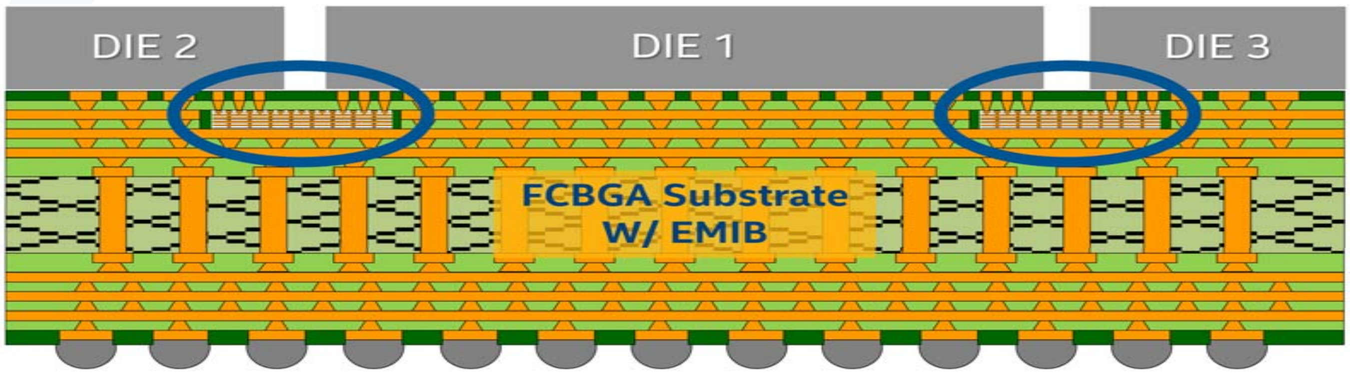
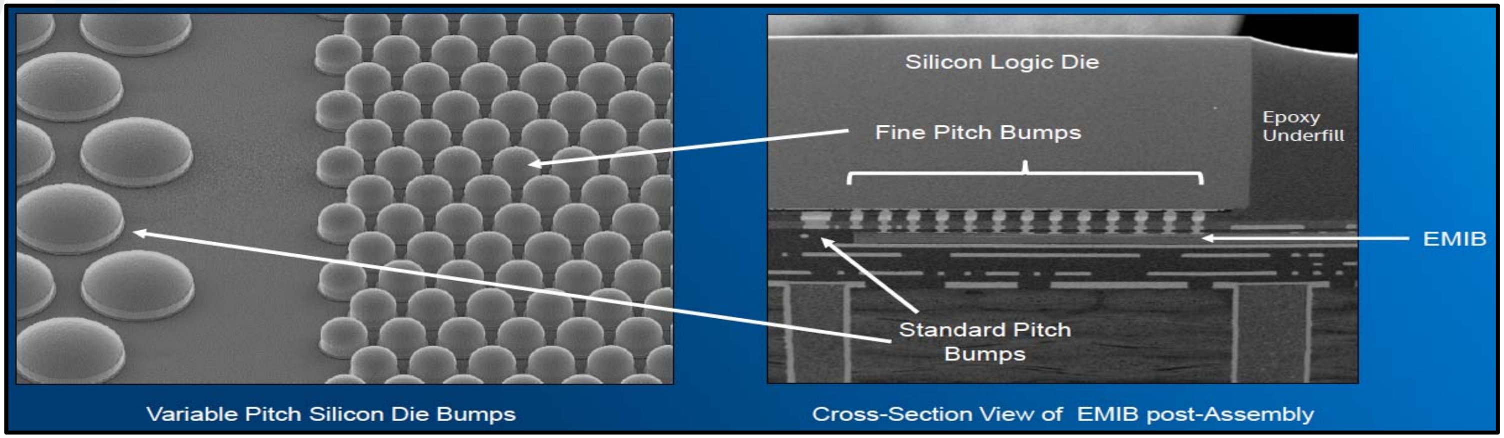
Intel's Silicon Bridge



Source: Intel.

- **Embedded Multi-die Interconnect Bridge (EMIB) A small silicon bridge chip is embedded into the package (no TSVs)**
  - Package substrate provided by substrate supplier (does Si bridge embedding)
- **Considered less expensive because only small area for high-density silicon and no TSVs**
- **EMIB allows the die I/O or bumps to be placed as close as possible to the edge of the die because fewer I/O or bumps are required**
  - Micro bumps on chips, communication between chips through interposer
- **Good electrical performance is reported due to the short interconnects**

EMIB Uses Micro Bumps and Standard Flip Chip Bumps



Source: Intel.

- **Custom I/O circuits fabricated on die and connect to neighbor die through substrate and silicon bridge**
  - Silicon die with 55µm pitch bumps to connect to silicon bridge
  - Bump pitch of 130µm on chip area outside the silicon bridge
- **Assembly done by Intel (Known Good Substrate and Known Good Die)**
- **Challenge of how to maintain planarity during assembly**
- **Requires thermo-compression bonder and epoxy underfill**

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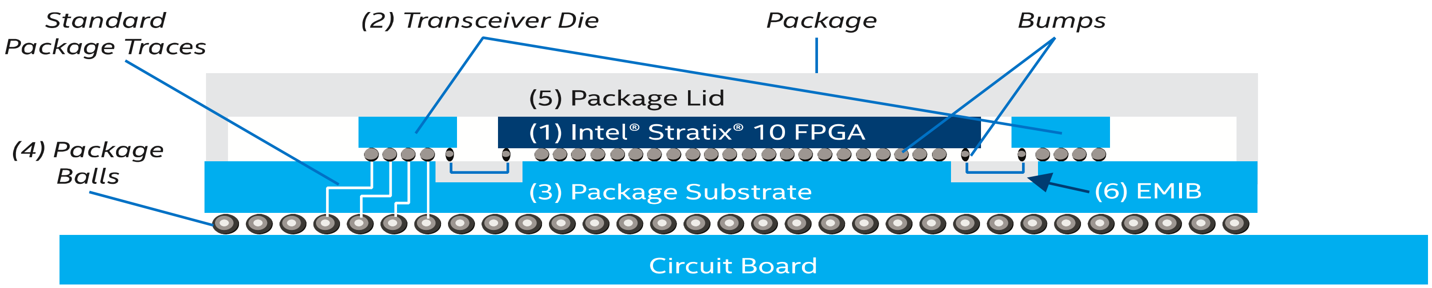
Heterogeneous Integration Using EMIB Technology



Source: Intel.

- **Stratix 10MX FPGA product with integration of HBM2 uses EMIB**
- **Stratix FPGA on 14nm FinFET silicon node**
- **Intel purchased Altera in 2015**

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Growth in FO-WLP on Substrate

- **ASE's Fan-Out Chip on Substrate (FOCoS)**
  - RDL with 2µm/2.5 L/S
  - Up to 3 RDLs plus UBM
  - High I/O (>1,000)
  - Production for Hi-Silicon since 2016, new customers expected
- **TSMC Integrated Fan-Out WLP on Substrate (InFO_oS)**
  - RDL with 2µm L/S
  - Up to 3 RDLs plus UBM
  - In production or MediaTek Switch
- **Amkor's Silicon Wafer Integrated Fan-out Technology (SWIFT®)**
  - RDL with 2/2µm L/S
  - Up to 3 RDLs plus UBM
  - Potential customers in 2019

FOCoS – Fan Out Chip on Substrate (FO FCBGA)

Source: ASE.

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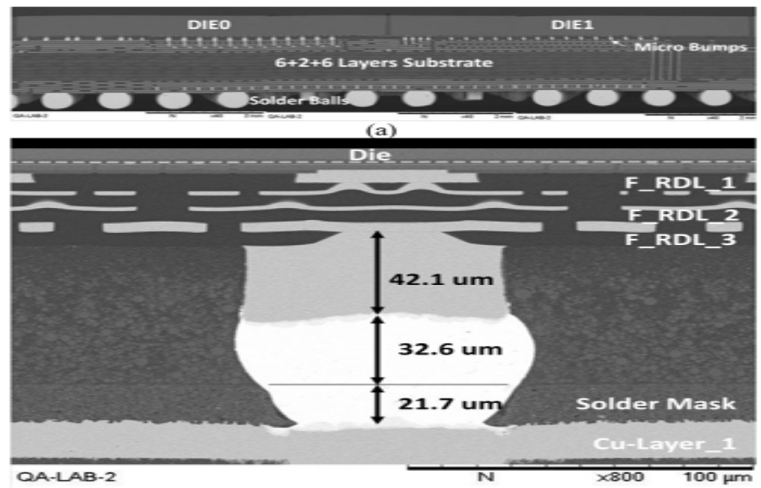
TSMC's InFO_oS for Switch

- **MediaTek network switch fabricated using TSMC's InFOoS process for a switch**
- **Attached to a 55 mm x 55mm organic interposer**
  - Organic substrate
  - 44µm pitch Cu pillar bumps
- **Two homogeneous die integrated onto a wafer level carrier with fine feature 3-layer RDL**
- **Excellent performance**
  - Verified use of high-speed SERDES with 25Gbit/second data rate
  - Excellent signal and power integrity were reported



Source: MediaTek.

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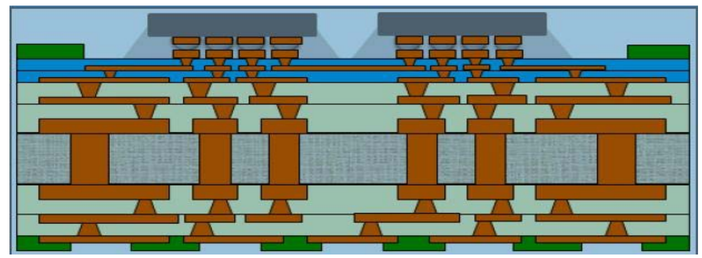
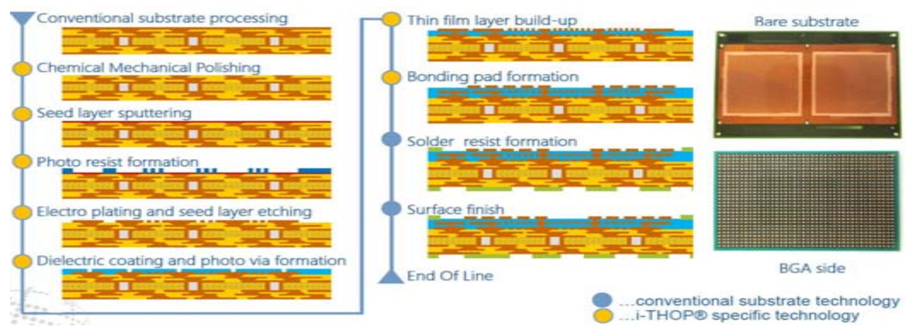
Shinko Electric's i-THOP®

- **Shinko Electric's integrated Thin film High density Organic Package (i-THOP®)**
  - Collaboration between Shinko Electric, GLOBALFOUNDRIES, and Amkor
- **Potential applications**
  - Server/Networking with large die
  - Logic/logic or logic/memory integration
  - Where substrates ≥ 55mm x 55mm required
- **Interposers developed**
  - Fine line routing layers, minimum 2µm (L/S)
  - Suitable for HBM integration
  - Higher routing capability compared to conventional substrates
  - Cost advantages expected compared to silicon interposer





Source: GlobalFoundries and Shinko Electric.

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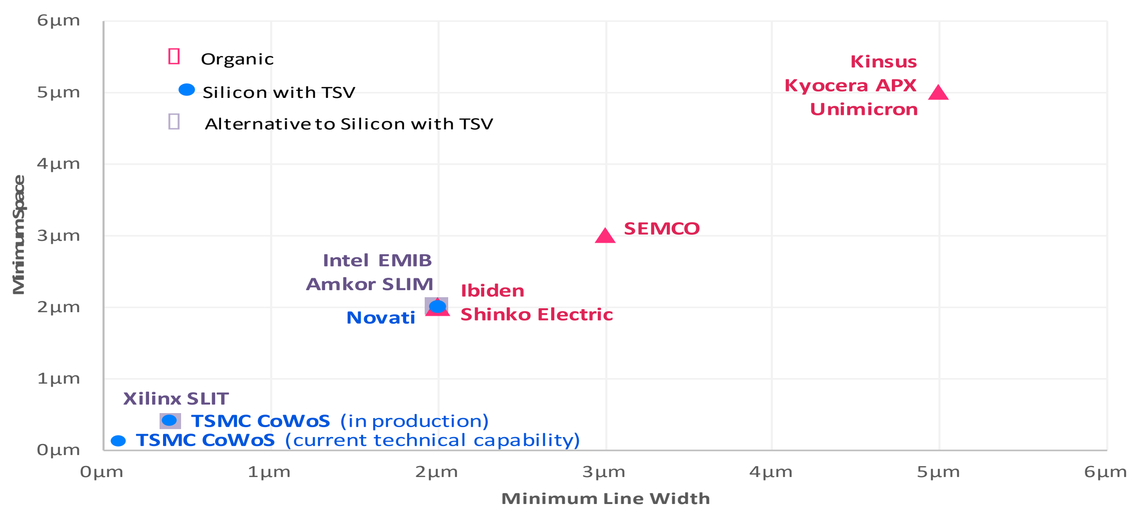
Selected Interposer Suppliers and Features



- **Silicon interposers with TSVs remain the highest density solution**
- **Companies continue to make progress in organic interposers and other alternatives to silicon interposers with TSVs**

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Test Challenges for Heterogeneous Integration

- Known Good Die (KGD) required
- Known Good Substrate needed
- Know Good Interconnect (assumed)
- Need more comprehensive test content that can be run at wafer-level
- Need new methods to probe fine pitch bumps or test coverage without touching µbumps

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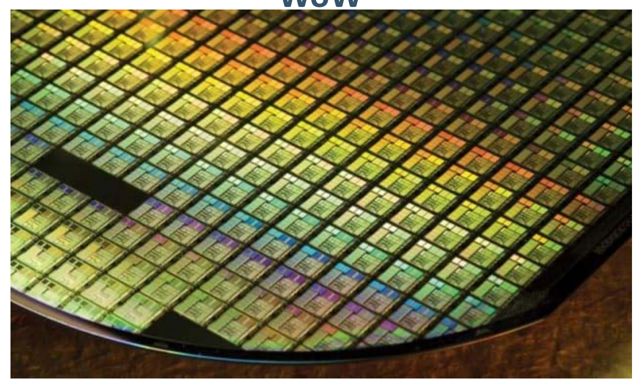
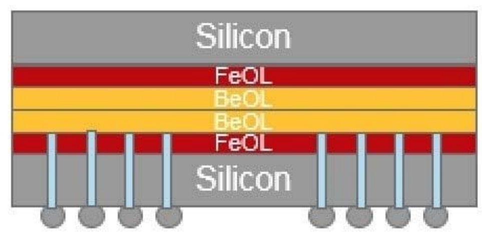
What's Next? 3D Integration

- **3D integration of image sensors, memory and logic**
  - In production today
- **3D memory stacking**
  - In production today
- **Intel's Foveros**
- **TSMC's CoW, WoW, and SoIC**
  - System on Integrated Chip (SoIC) 3D stack using CoW process to handle <10µm bond pitch between chips
  - Two-die stack face-to-face (F2F) and a three die stack
  - Use of hybrid bonding
- **New forms of 3D stacking (die-to-die interconnects) are coming**

WoW



Source: TSMC.



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Test Issues for 3D IC with TSV

- **Want to minimize total cost of test and test-escape**
  - **Today: "Stack and Pray" = accumulated yield loss**

1 chip	2 chips	3 chips	4 chips
90%	81%	73%	64%

  - **Today 3D IC memory stacks tested in packages**
  - **100% Test before assembly and after each assembly event = high test cost**

- **Do we test through the TSV/micro bump interface or around it?**
  - Testing a 10,000 micro bump array is difficult and potentially very expensive
  - Need to test connections
  - Need BIST, redundancy, self-repair

Source: Adapted from P. Franzon

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Conclusions

- **Despite lower growth rates, mobile phones still drive volume**
  - WLP and FO-WLP
  - System-in-Package
- **5G is coming**
  - Infrastructure roll out started
  - RF modules require good test solution
- **Increased use of social media and IoT driving datacenter demand**
  - Growth for AI accelerators
  - AI accelerators demand drives use of silicon interposer and HBM
  - Si interposer proven technology, but alternatives emerging
  - Heterogeneous integration key to "economic limits of scaling"
  - Good test strategy critical
- **Challenges**
  - Need more attention to design for test and test methods
  - Yield is key, metrology important

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Thank you!

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