

TWENTIETH ANNUAL



TestConX™

March 3 - 6, 2019

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

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Time to Market Acceleration with Virtual Validation Farm in Post-Silicon

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Time to Market Acceleration with Virtual Validation Farm in Post-Silicon

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Design Validation in Post-Silicon

System on Chip (SoC) design consists of multiple predesigned Intellectual Property (IP) blocks, which leads to complexity in design validation/debug

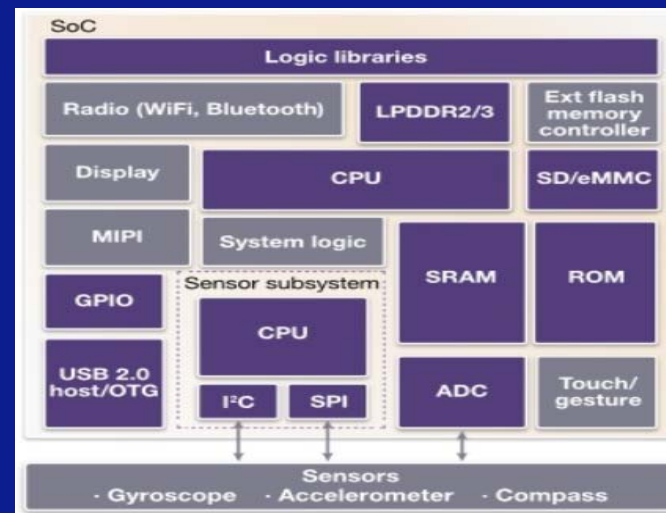


Diagram 1: Sample of SoC IP Blocks

Design Validation in Post-Silicon

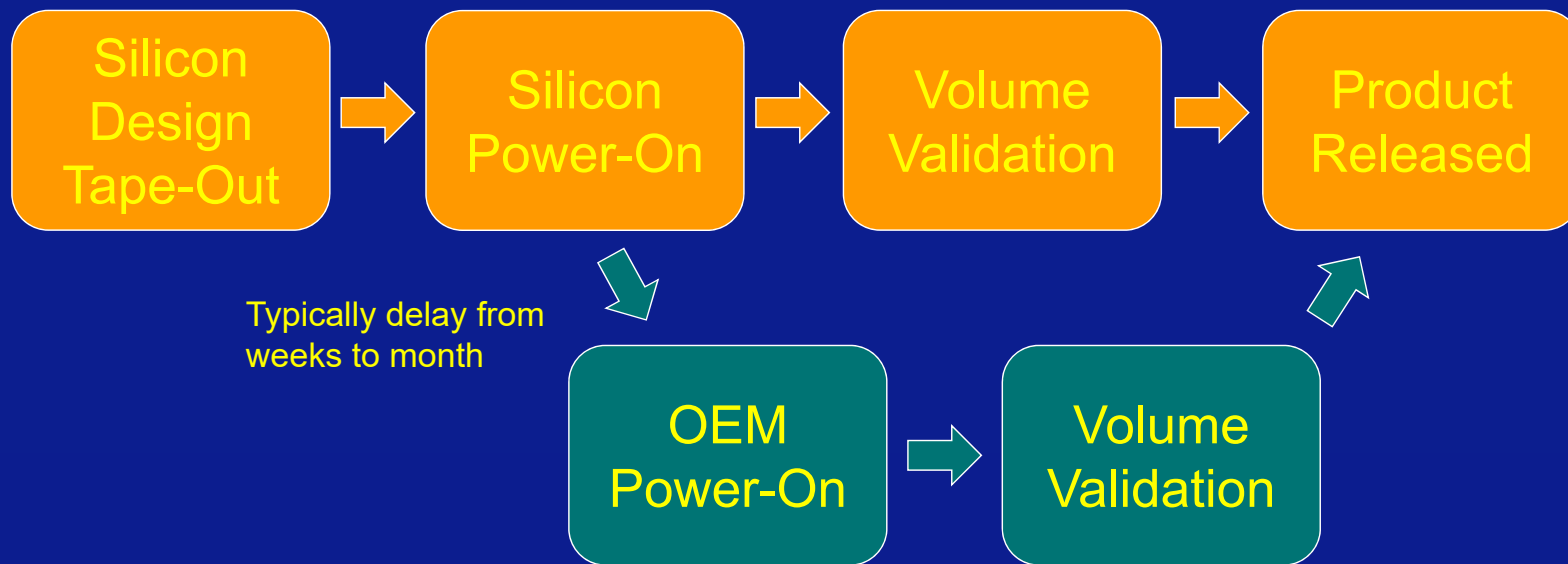


Diagram 2: Typical Design Flow

Validation Challenges in Post-Silicon

- Collaboration from cross functional team in bug sighting
- External IP supplier to support bug sighting
- Limited first article silicon
- Slow in silicon design iteration

High Development Cost!



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TTM Acceleration with Virtual Validation Farm

Ideal development environment:

1. Secure debug environment
2. Self-operate
3. 24x7 validation operation
4. Remote accessible
5. Fast access, anytime, anywhere

Improved Time-to-Market!



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TTM Acceleration with Virtual Validation Farm

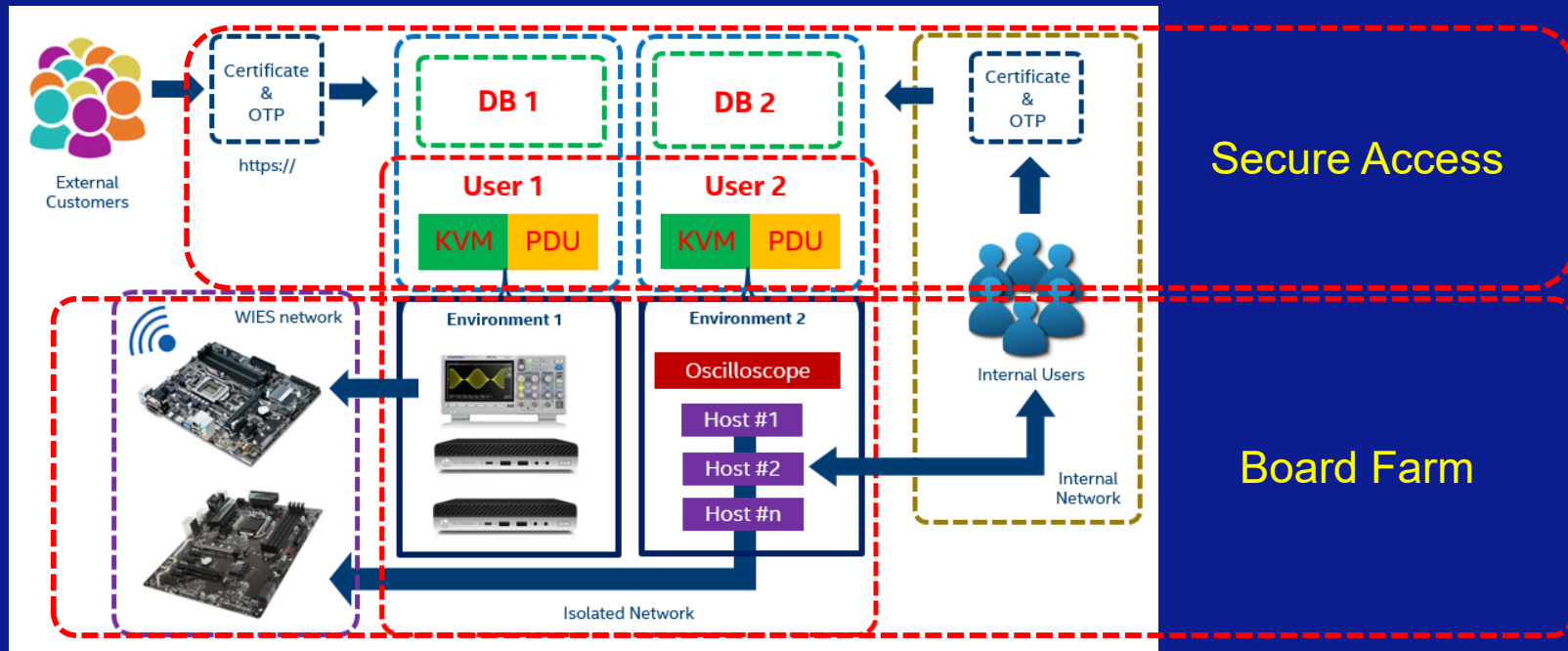


Diagram 3: Virtual Validation Farm

TTM Acceleration with Virtual Validation Farm

- Secure Access:
 - Online certificate
 - Individual login credential
 - Secure Virtual Private Network (VPN)
 - One-Time-Passcode (OTP)



TTM Acceleration with Virtual Validation Farm

- Board Farm:
 - Asset access & control management system
 - Platform scheduling system
 - Auto OS provisioning solution
 - Extensive remote debug features



Summary

- Virtual Validation Farm has helped to transform validation operation in Intel by:
 - Reduced 20% cost in reference board purchase
 - Improved 3 weeks early customer engagement
 - Improved 90% design infra setup time in lab
 - Enabled 24x7 validation operation
- Received overwhelming response from users



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Acknowledgements

- Eric Chan - VP in Intel IoTG
- Board of Directors in Intel Malaysia Design Center (MDC)
- Ng, Hooi Ching – IT Malaysia Hub Manager
- Goh, Kean Hean – Engineering Lab Manager
- Lim, Hock Lam – MDC Lab Manager
- Chang, Siew Cuong – Engineering Lab Manager
- Mamat, Siti Zurmarini - Post-Silicon Technologist



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