# TWENTIETHANNUAI

estConX

## March 3 - 6, 2019

Hilton Phoenix / Mesa Hotel Mesa, Arizona

Archive

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Session 6B Presentation 1

Material Differences - PCB Materials

# Coaxial Via-Based Microstrip Line for High Performance HDI Platform Design

Xiao-Ming Gao Intel Incorporation





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## Agenda

- Applications of ground return via in high speed design
- Pros and cons of using ground return vias
- Coaxial via construction
- Design of coaxial via based microstrip line
- Application of coaxial via microstrip line
- Manufacturing process
- Summary





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GND vias (Green) near SFP connector



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## **Pros and Cons of Using Ground Return Vias**

#### Pros:

- Minimize impedance discontinuities
- Reduce noise and crosstalk to nearby signals
- Improve EMI
- Cons:
  - Cost extra space
  - Sometime prohibitive such as in some HDI designs
  - Crosstalk isolation is limited





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## **Design of Coaxial Via Based Microstrip Line**

8 Layer PCB Stackup Parameters

Name	Туре	Material	Thickess	Layer Type
Metal-1	Metal	Copper	1.2	Signal
Dielectric-1	Dielectric	FR4	5	
Metal-2	Metal	Copper	1.2	Plane
Dielectric-2	Dielectric	FR4	5	
Metal-3	Metal	Copper	1.2	Signal
Dielectric-3	Dielectric	FR4	5	
Metal-4	Metal	Copper	1.2	Plane
Dielectric-4	Dielectric	FR4	5	
Metal-5	Metal	Copper	1.2	Plane
Dielectric-5	Dielectric	FR4	5	
Metal-6	Metal	Copper	1.2	Signal
Dielectric-6	Dielectric	FR4	5	
Metal-7	Metal	Copper	1.2	Plane
Dielectric-7	Dielectric	FR4	5	
Metal-8	Metal	Copper	1.2	Signal

#### Parameters:

Drill size:	16 mils
Via pad:	24 mils
Anti-pad:	32 mils
Trace width:	5 mils
Trace length:	100 mils



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## **3D Electromagnetic Modeling**



Standard via with GND return via

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#### Coaxial via

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### **Insertion Loss Performance**



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## **Coaxial Via Outer Wall Drill Size Sensitivity**



Insertion Loss (32mil drill size)

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## **Design of Coaxial Via Based Microstrip Line**

Name	Туре	Material	Thickess	Layer Type
Metal-1	Metal	Copper	1.2	Signal
Dielectric-1	Dielectric	FR4	5	
Metal-2	Metal	Copper	1.2	Plane
Dielectric-2	Dielectric	FR4	5	
Metal-3	Metal	Copper	1.2	Signal
Dielectric-3	Dielectric	FR4	5	
Metal-4	Metal	Copper	1.2	Plane
Dielectric-4	Dielectric	FR4	5	
Metal-5	Metal	Copper	1.2	Signal
Dielectric-5	Dielectric	FR4	5	
Metal-6	Metal	Copper	1.2	Plane
Dielectric-6	Dielectric	FR4	5	
Metal-7	Metal	Copper	1.2	Plane
Dielectric-7	Dielectric	FR4	5	
Metal-8	Metal	Copper	1.2	Signal
Dielectric-8	Dielectric	FR4	5	
Metal-9	Metal	Copper	1.2	Plane
Dielectric-9	Dielectric	FR4	5	
Metal-10	Metal	Copper	1.2	Signal
Dielectric-10	Dielectric	FR4	5	
Metal-11	Metal	Copper	1.2	Plane
Dielectric-11	Dielectric	FR4	5	
Metal-12	Metal	Copper	1.2	Signal

12 Layer PCB Stackup Parameters

#### Parameters:

Drill size:16 milsVia pad:24milsAnti-pad:32milsTrace width:5milsTrace length:100 mils



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## **3D EM Modelling of PCB Coaxial Via Crosstalk**



Top view

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Ports set up

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## **Standard Vias with Ground Return Vias**



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#### Ports set up

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## **Comparisons of Far End Crosstalk (FEXT)**



Standard via microstrip line FEXT

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Coaxial via microstrip line FEXT

Coaxial via microstrip FEXT is much lower than standard via

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# Single ended signaling Transmit signal rate is 10 Gb/s Controller to device two coupled data channels Tx 1 is the victim and Tx 2 is the aggressor

Eye diagrams are measured at Rx 1





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## **Receive Eye Diagram Margins**



Case 1: standard vias with GND vias Rx 1 timing margin is 52ps

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Case 2: coaxial via microstrip line Rx 1 timing margin is 59ps

Transmit data rate is at 10 Gb/s

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## **Coaxial Via Manufacturing Process**

#### **Sequential lamination process:**

- For internal layers:
  - $\,\circ\,$  First step is to drill the larger outer via
  - $\circ$  Second step is to plate this larger through hole via
  - Third step is to fill the this hole with dielectric material
- Construct the top and bottom layer with traces
- Add the top and bottom layers to internal layers and press together
- Drill the smaller inner via from top to bottom layers
- Plate this smaller through hole via





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## Summary

- Coaxial via based microstrip line is space efficient
- Superior crosstalk isolation
- Improved eye diagram timing margins
- Compatible with current PCB manufacture process



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