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Session 6A Presentation 3

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Testing Challenges for Cu Pillar Wafer by Spring Probe

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Content

- Cu Pillar WLCSP Introduction
- Existing Test Method and Challenges for Probing Cu Pillar Wafer with Spring Probes.
- Extensive Studies on Spring Probe Mark Analysis on Cu Pillar Wafer
- FDR Result
- Recommendation and Summary

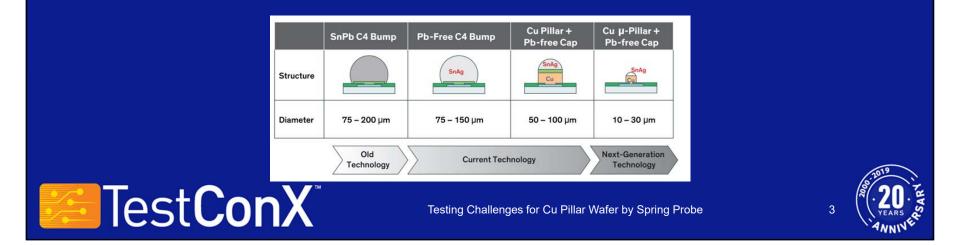




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Cu Pillar Introduction

- WLCSP solder bump has reached its minimum limit in bump size and pitch
- The trend is increasing the number of IO pins in smaller die size at smaller pitch
- Cu Pillar is the next generation bump technology for greater density in smaller pitch
 - Lower cost
 - Ability to mix smaller more flexible shape with thin SnAg cap in finer pitch
 - Superior electrical and thermal performance than that of conventional solder bumps.

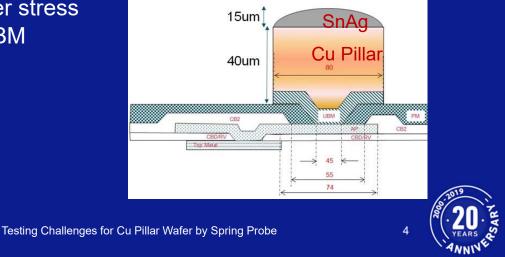


Cu Pillar Test Requirement

Probing on Cu Pillar:

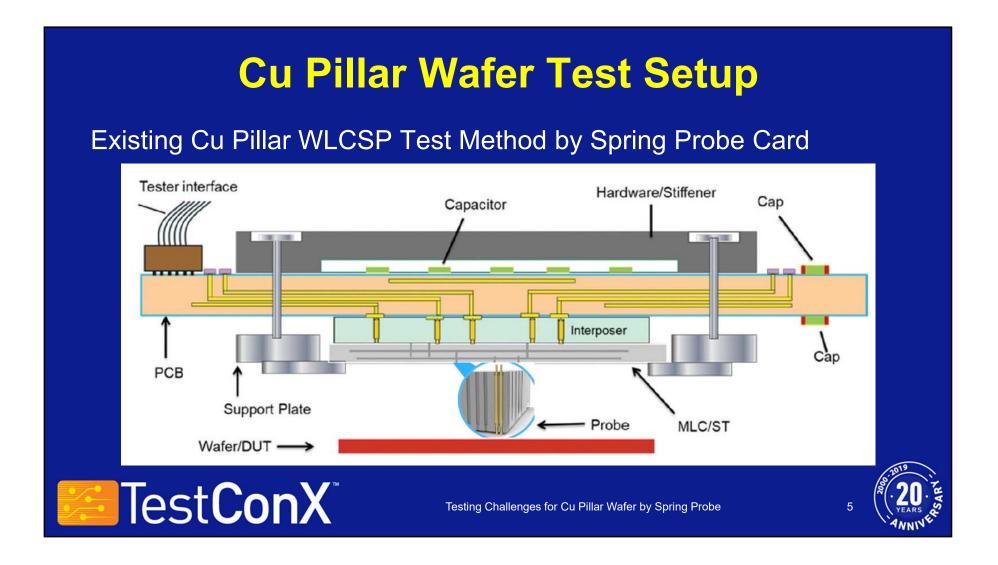
- Spring Probes only need to penetrate the thin SnAg Cap for good Cres performance
- Spring Probes should not expose Cu Pillar, to prevent oxidation or create voids, as defects may occur in final SMT reflow process
- Spring Probe Force should not over stress Cu Pillar to avoid damaging the UBM (Under Bump Metallurgy) layer

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Cu Pillar Test Challenges with Spring Probe

- Probe Head with Spring Probe design must meet mechanical and electrical Cu Pillar test requirements
- Effect of contact mark by Spring Probe on Cu Pillar integrity
- Use FEA and FDR to confirm Spring Probe Design can meet test requirements



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- Thin cap of SnAg on Cu Pillar is much smaller than conventional solder bump which requires optimized spring probe design.
- Spring Probe must meet all minimum mechanical reliability requirements and at the same time to maintain good Cres performance.

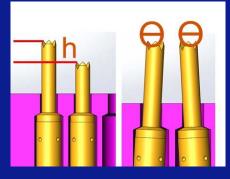




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Probe Head Design and Manufacturing Challenges

- Spring Probe Tip Tilting and Tip co-planarity
- Spring Probe Tip Material and Geometry
- Probe Head Deflection



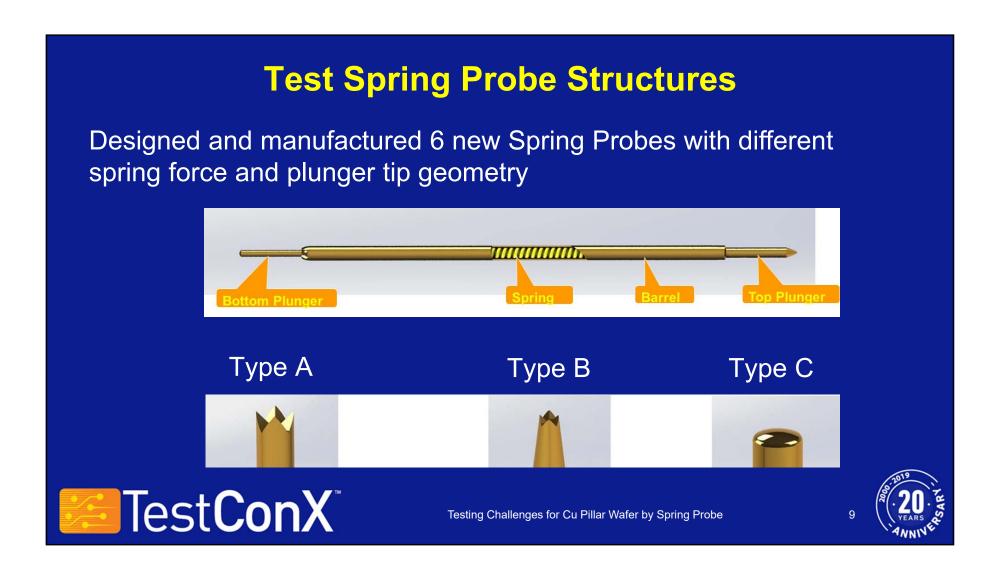
- Probe Head design needs to tolerate and consider the effective force of 1st to last touch and tip co-planarity due to manufacturing process.
- Spring Probe Tip material and geometry must optimize to minimize the effect of probe mark on Cu Pillar.





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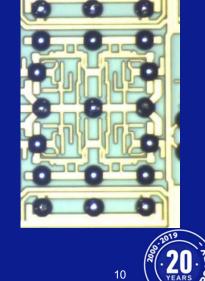
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Cu Pillar Prober Test with Spring Probe

Extensive Probe Mark Analysis DOE

- Cycle 6 Probe Head with 3 different Plunger tip (A, B and C) with 2 different gram force springs on fresh wafer row each time, using Cu Pillar wafer.
- Analyze Probe Mark size and depth after each 1, 3 and 5 touch down, at 100 to 160um of over drive

Example of probing 9 Cu Pillars on one Die ID# Y33 – X58 5TD at 130um OD

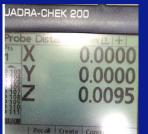








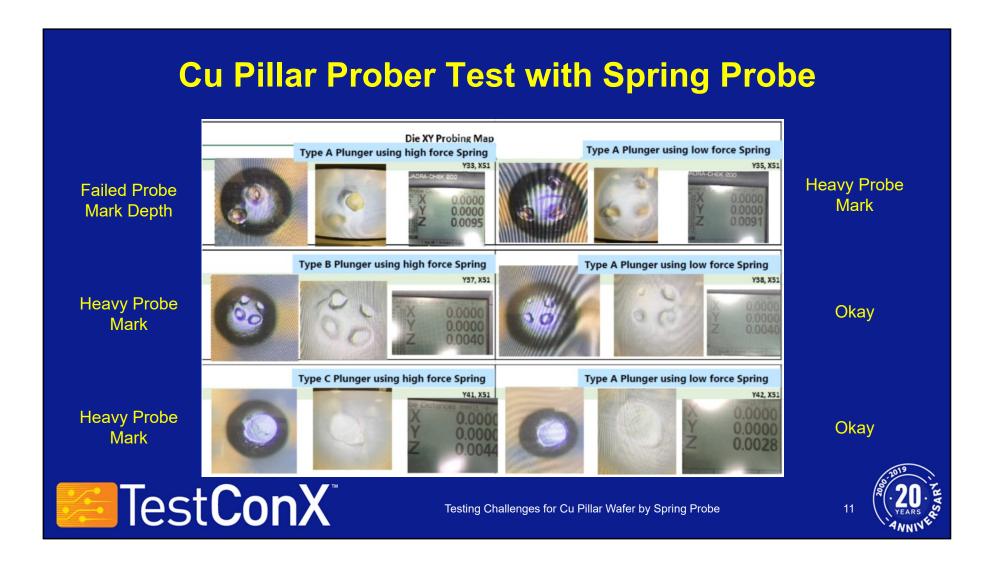
Probe Mark Depth



Testing Challenges for Cu Pillar Wafer by Spring Probe

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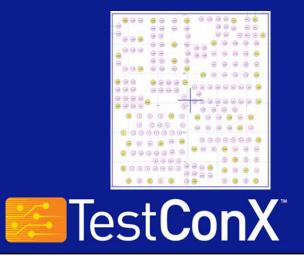


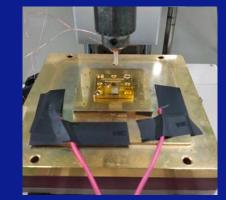
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Cu Pillar Single Die Test with Spring Probes

Test Setup

- Designed a test fixture to align with single die and use FDR Tester and short some Cu Pillar to FDR Tester GND (Sense) Channel.
- Designed FDR Pin Adapter to hold Spring Probe (in preload condition) and connect the plunger to the FDR Force Channel.
- Align Cu Pillar with each type of Spring Probe and obtain FDR to highlighted Cu Pillars.
- Analyze Probe Mark and Cres vs Deflection vs Force for each type of spring probe.



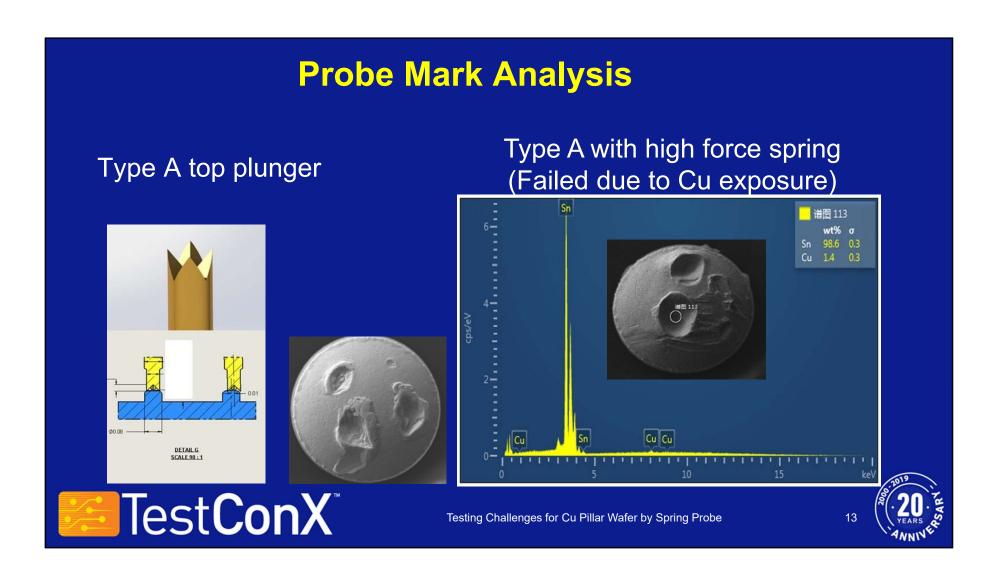


Testing Challenges for Cu Pillar Wafer by Spring Probe



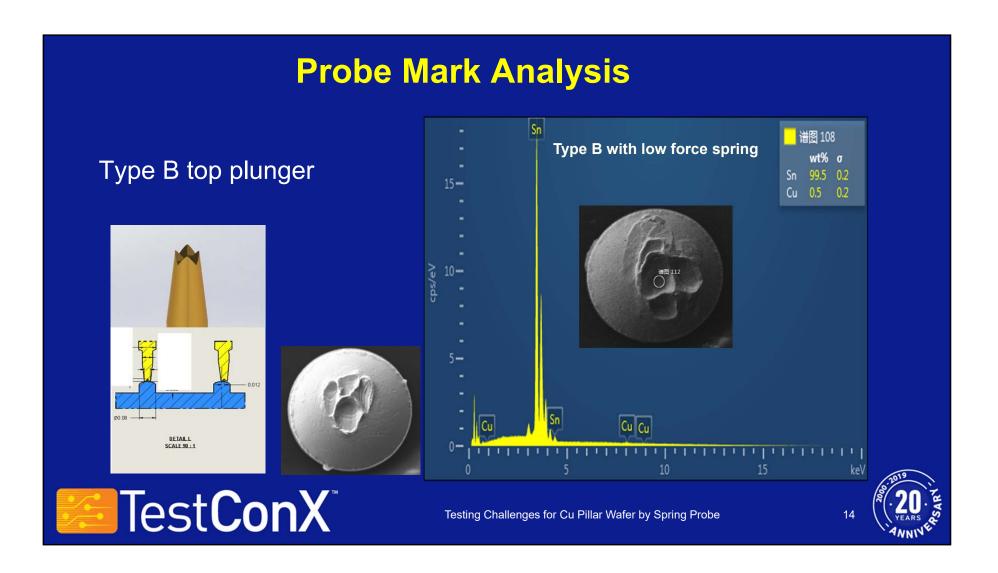
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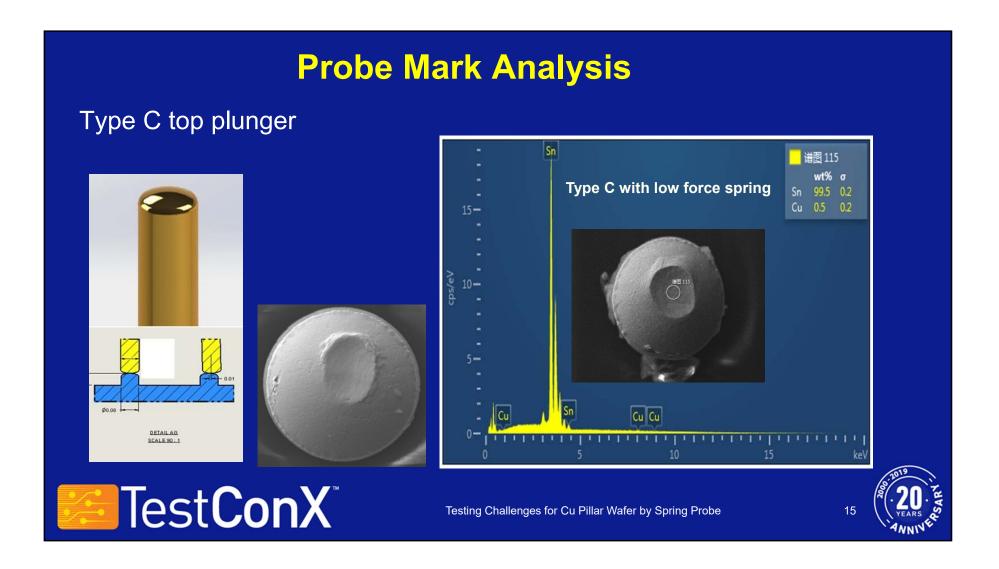
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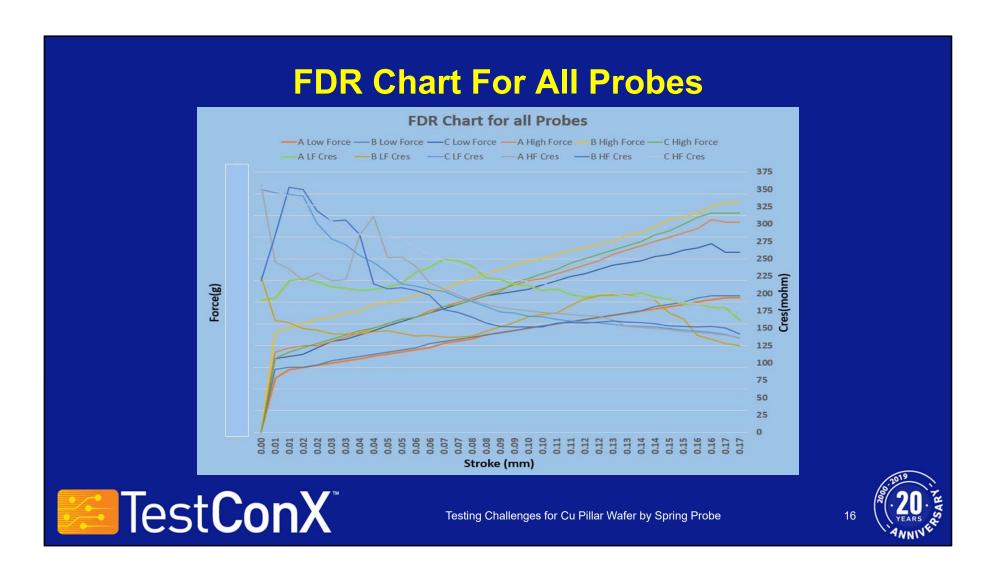
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Spring Probe Tip Type		Cres (mOhm)
Type A with High and Low Spring Force		179.9
		154.8
Type B with High and Low Spring Force		152.4
		128.4
Type C with High and Low Spring Force		183.8
		142.4
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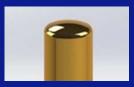
Recommendation and Summary



- Type A causing deep mark > 9 um too close to expose Cu and cause defect.



Type B with optimized force is showing good Cres, acceptable probe mark, and will be released to production to evaluate life verse yield and performance.



Type C with optimized force is showing good Cres, acceptable probe mark, and will be released to production to evaluate life verse yield and performance.

**** 2 PH with Type B and C will be released in HVM this spring for field validation.



