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Stretching the Performance Envelope of ATE PCBs

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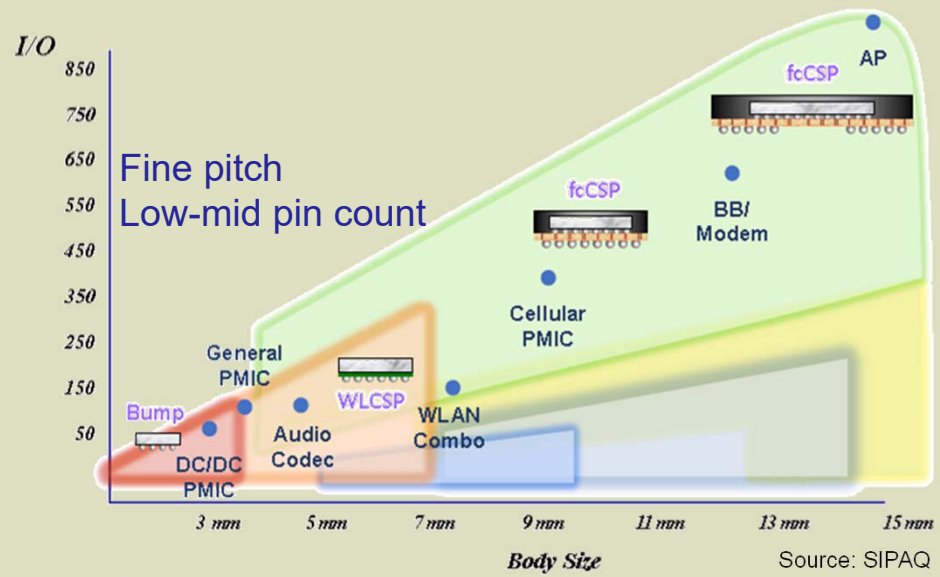
Contents

- Overview of industry trends
- Challenges presented to ATE PCBs
- Fabricator response to those challenges
- Viabond: The latest tool in our toolkit
- Summary

Industry Trends

- IC package size, pitch, IO count & parallelism drive complexity into the ATE interface



High power
High data rate IO
High pin count

Source: SIPAQ

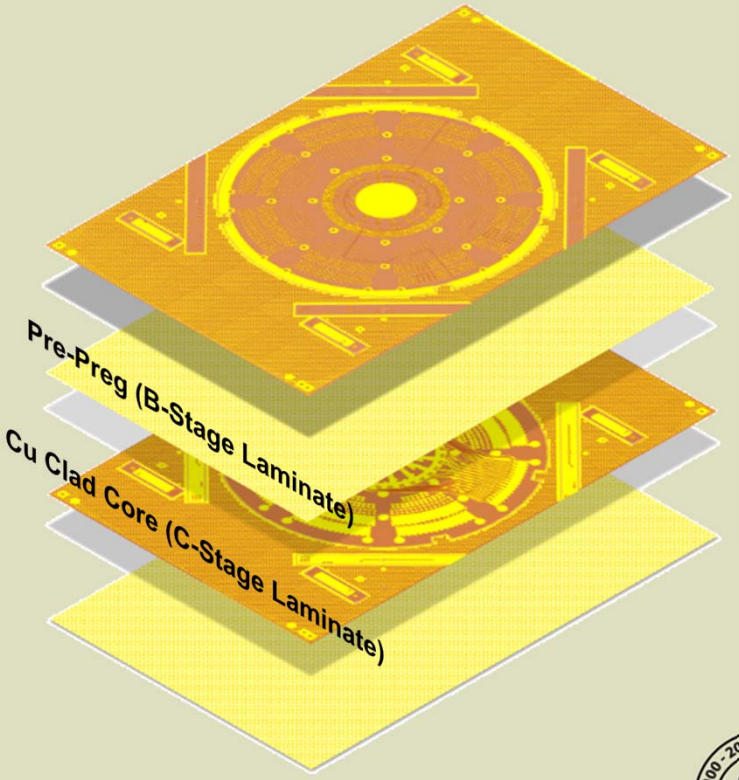
Impact on Production Test ATE Interface

- Basic and even advanced PCB manufacturing techniques need augmenting just to keep up

Complexity	Device Pitch	Device Ball Count	Parallel Test	Power (Current)	Speed	Test Cell Configuration
Low	0.5mm - 1mm	100	1up – 4up	< 1A	<1GBS	Singulated package test Staggered die
Med	0.40mm 0.35mm 0.30mm	200+	4up – 16up	100A / DV 50mv	10GBS	WLSCP Extended temp range (Automotive)
High	< 0.30mm	6000	16up - 128x	400A / DV <25mV	28GBS NRZ / 112GBS PAM4	Direct Attach 1 mil Flatness pad condition OTA 5G

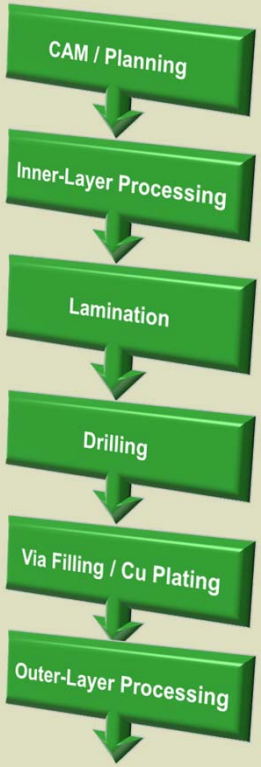
PCB Fabrication Basics

- The basic building blocks of the PCB are the same as they have been for years
- Controlled impedance multi-layer stack-up building block
- Repeat this basic structure over and over as necessary to complete the multi-layer PCB



PCB Fabrication Basics

- Controlled impedance layers; add some power planes
- Balanced stack-up to minimize warpage
- So far, so good, ~5 day turn



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PCB Thickness vs Drill Flute Length

- Now ramp up the complexity factors:
- DUT pin count / parallelism drives up layer count
- Layer count drives overall PCB thickness
- Encounter limitations of PCB drill dimensions, specifically Flute Length
- Flute Length limits PCB Thickness

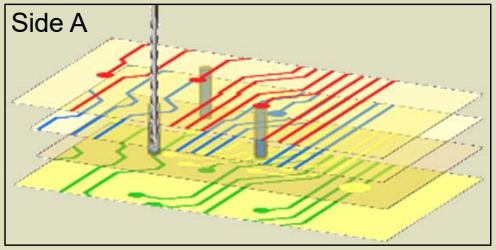
- Note that Flute Length varies with drill diameter Smaller the drill diameter, shorter the flute length
  - 10 mil drill, flute length = 0.220”
  - 6 mil drill, flute length = 0.120”

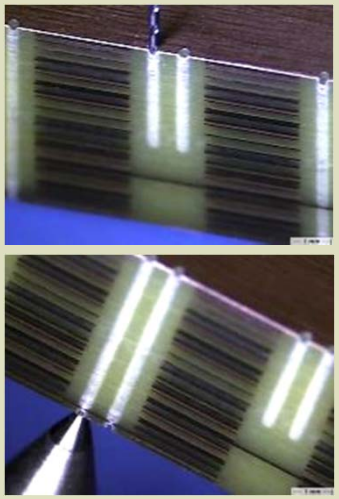
Drill Size	Dimensions (in) D	d	ℓ	L	Point Angle
.10mm	0.0040	1/8	0.0700	1 1/2	118°
.13mm	0.0050	1/8	0.0700	1 1/2	118°
#97	0.0059	1/8	0.1200	1 1/2	118°
#96	0.0063	1/8	0.1200	1 1/2	118°
#95	0.0067	1/8	0.1200	1 1/2	118°
#94	0.0071	1/8	0.1500	1 1/2	118°
#93	0.0075	1/8	0.1500	1 1/2	118°
#92	0.0079	1/8	0.1500	1 1/2	118°
#91	0.0083	1/8	0.1500	1 1/2	118°
#90	0.0087	1/8	0.1500	1 1/2	118°
#89	0.0091	1/8	0.2200	1 1/2	118°
#88	0.0095	1/8	0.2200	1 1/2	118°
.25mm	0.0098	1/8	0.2200	1 1/2	118°
#87	0.0100	1/8	0.2200	1 1/2	118°

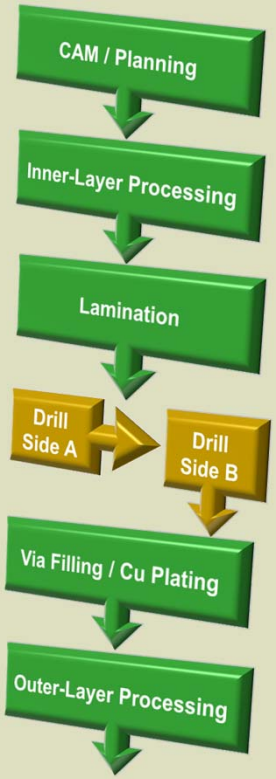
http://www.kyoceramicrotools.com/micro/drilling/Series-105-6

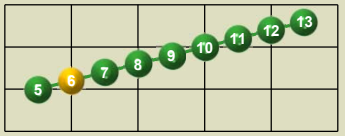
Technology Extender: Flip Drill

- Drill side A, flip PCB, drill from side B
- Doubles the PCB thickness which can be drilled
- Also doubles the number of holes to drill









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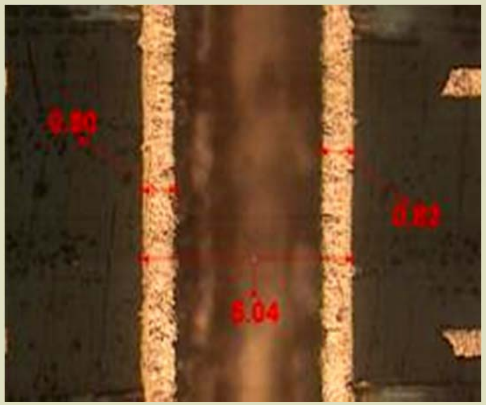
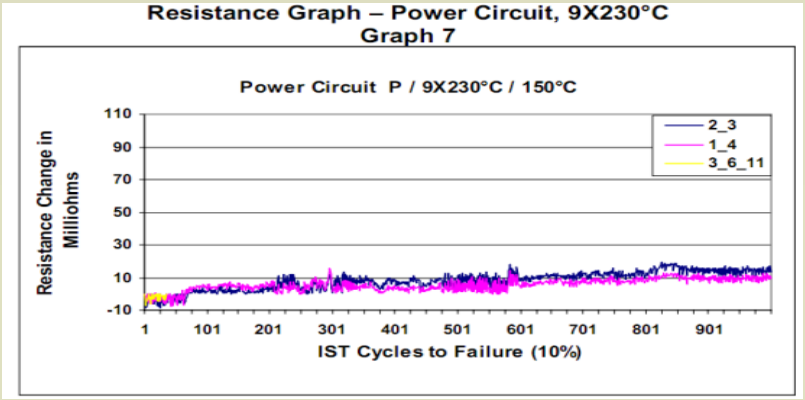
Plating High Aspect Ratio Vias

- Small diameter holes through thick PCBs make for aspect ratios in excess of 30:1
- Technology extender: pulse plating
- Plating the holes adequately is non-trivial, but well understood
- However, pulse plating techniques add to processing time





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WLCSP Planarity Requirements

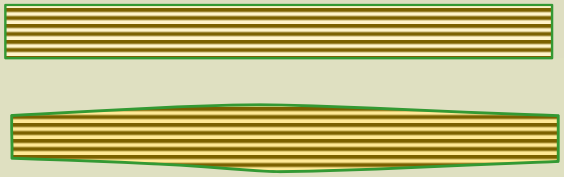
- Multi-site testing effectively increases area of DUT site
- So-called 'Direct Attach' applications which require excellent planarity (1 mil across entire DUT area)
- In the PCB, Cu density is usually greatest at center / DUT sites
- Prepreg squeezes out the edge of the panel during lamination
- Rate varies with Cu density
- Creates a board with 'crown' at / near center of PCB

PCB Crown with standard manufacturing process

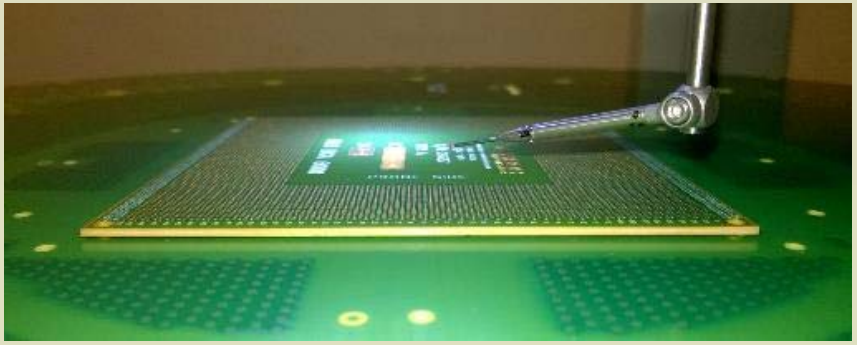
Technology Extender: UltraFlat™

- Improves flatness / warpage across the DUT area and across the entire board
  - 0.1%-0.15% (0.001”-0.0015”/inch) on most applications
  - 0.2% on dual lamination
- Adds processing time

Harbor UltraFlat™ Technology

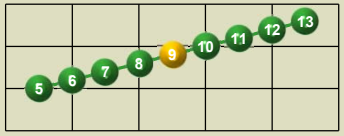


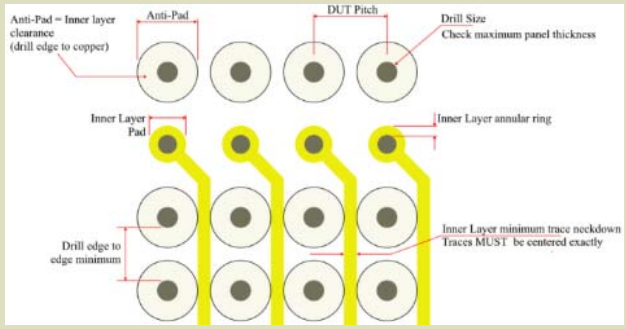
PCB Crown with standard Mfg. Process

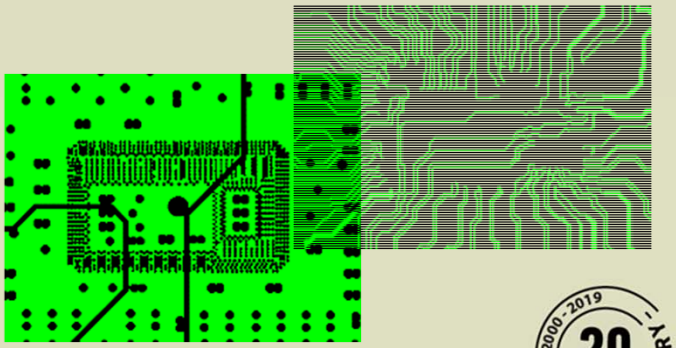


Routing Lanes, Fine Pitch DUTs

Technology Extender			
Registration Geometries	0.4mm pitch	0.35mm pitch	0.30mm pitch
Drill Diameter	0.13mm (0.0051”)	0.13mm (0.0051”)	0.10mm (0.0041”)
Anti-pad	0.322mm (0.0127”)	0.0307mm (0.0121”)	0.236mm (0.0093”)
Trace/Web	0.0762mm (0.003”)	Trace: 0.0635mm (0.0025”) Web: 0.0445mm (0.00175”)	0.0635mm (0.0025”)
Thickness	5.08mm (0.200”)	5.08mm (0.200”)	2.286mm (0.090”)
Layer Count	≤ 50	≤ 50	≤ 22
Registration Challenges	- Lay-up precision - Material movement	- Same drill size as 0.4mm - Narrower trace width - Narrower web	- Smaller drill diameter allows relief to trace width and web

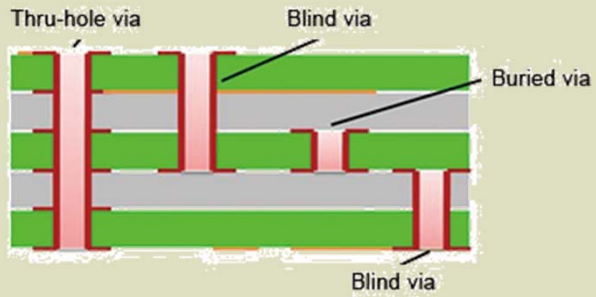


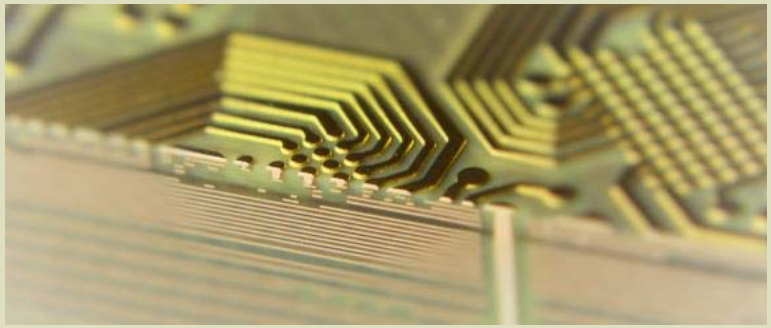


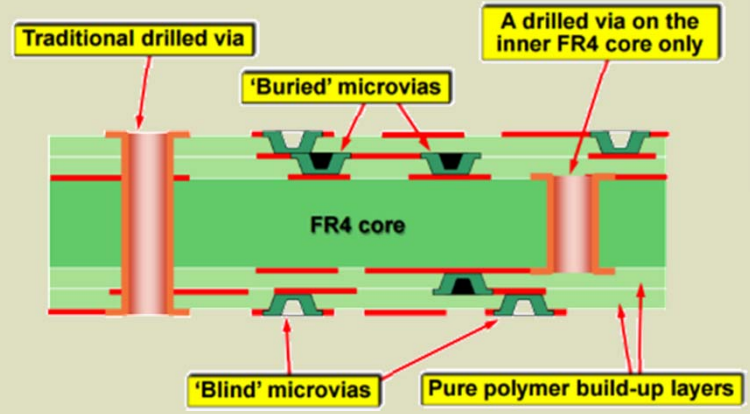


Blind & Buried Vias to Increase Routing Area

- Improves available routing lanes when via does not go all the way through the PCB







- Laser drilled micro vias for HDI implementations

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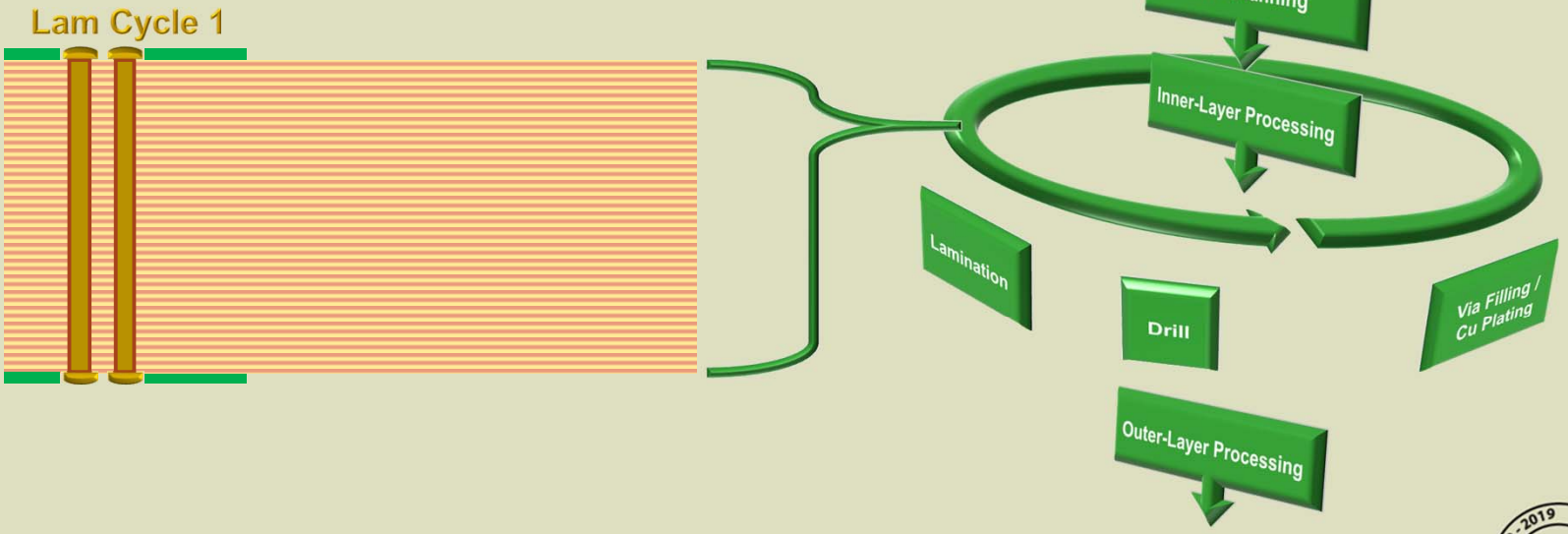
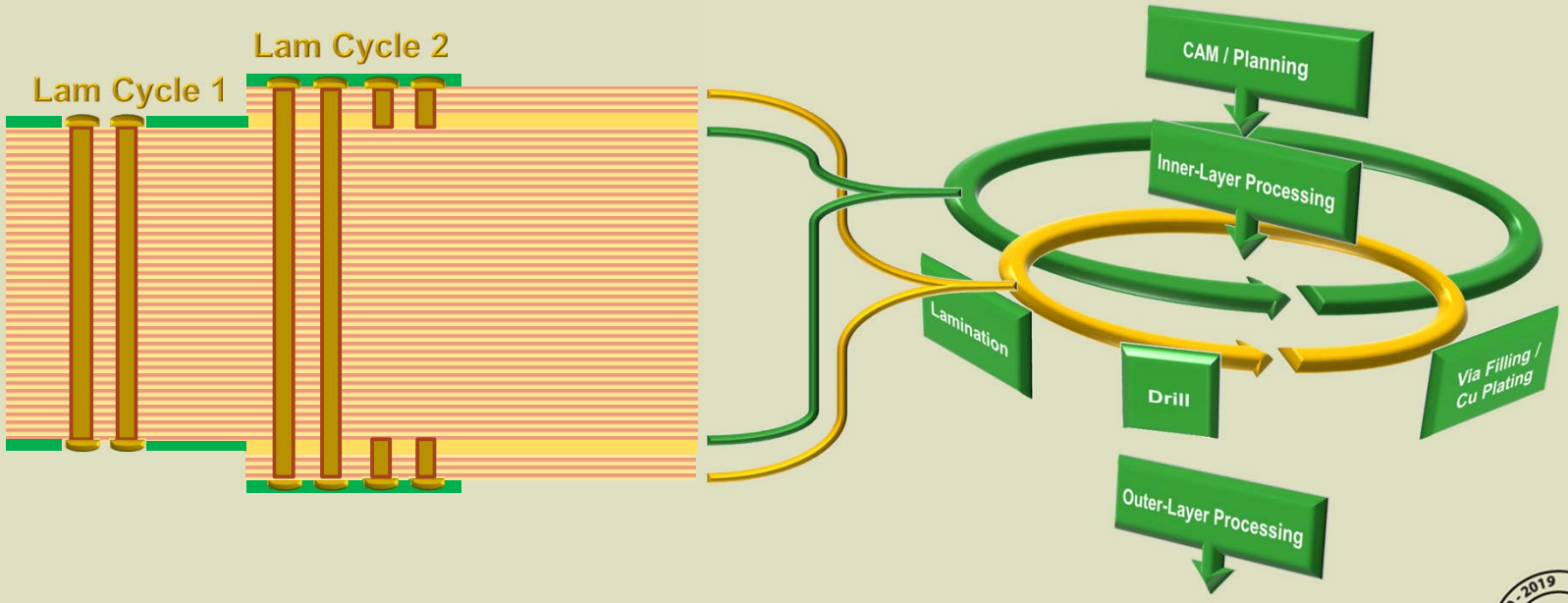
Technology Extender: Multiple Lamination Cycles

- Blind & buried vias are realized using multiple laminations
- Laminations are sequential, where an additional lamination step adds a pair of layers to the base core book



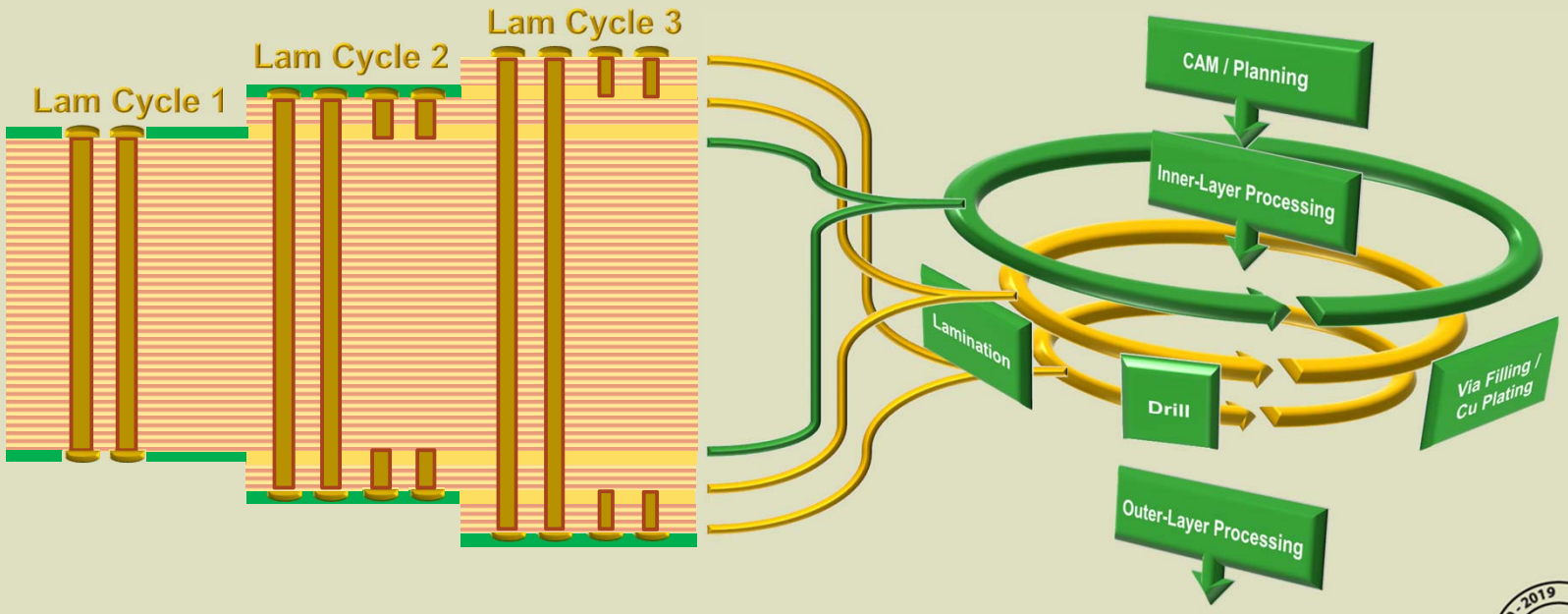
Technology Extender: Multiple Lamination Cycles

- HDI techniques: additional lamination step for each pair of layers attached on either side of the core book

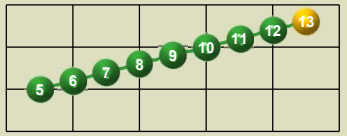


Technology Extender: Multiple Lamination Cycles

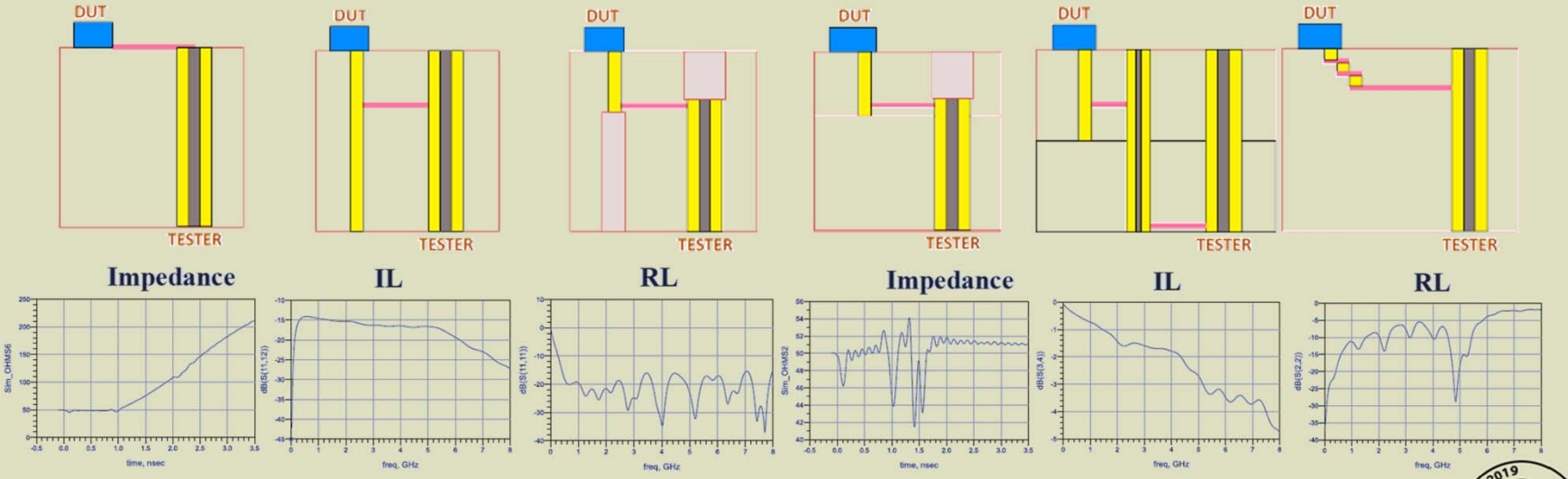
- Overall thickness may still be an issue for the through-vias



Signal Integrity

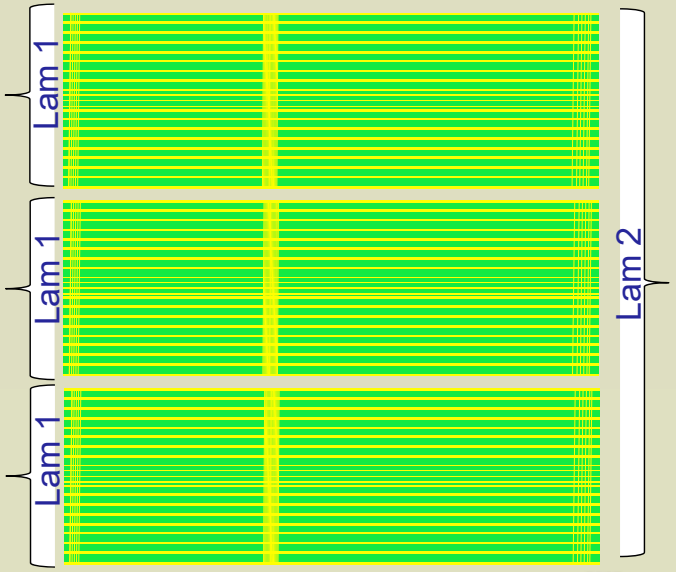


- Signal Integrity Requirements are always in play
  - Single lam, with backdrill, dual-lam, with backdrill, multi-lam
  - In all cases, the thickness of the PCB or “book” is limited to some degree by drill flute length



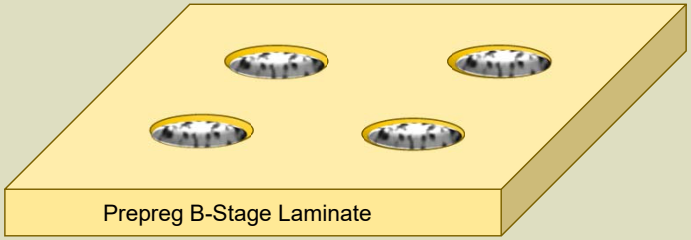
Technology Extender: Viabond

- Viabond uses sintering paste to bond PCBs together
- Maximum PCB thickness is no longer limited by drill flute length, as each “book” is drilled individually
- Flute length limits thickness of the sub books, but the overall PCB can be 300, 400, 500, even 600 mils thick, if necessary
- Adds just one lamination cycle to fab time, as books 1, 2 and 3 are processed independently and in parallel, then the three boards/books are bonded together in a 2nd lamination step



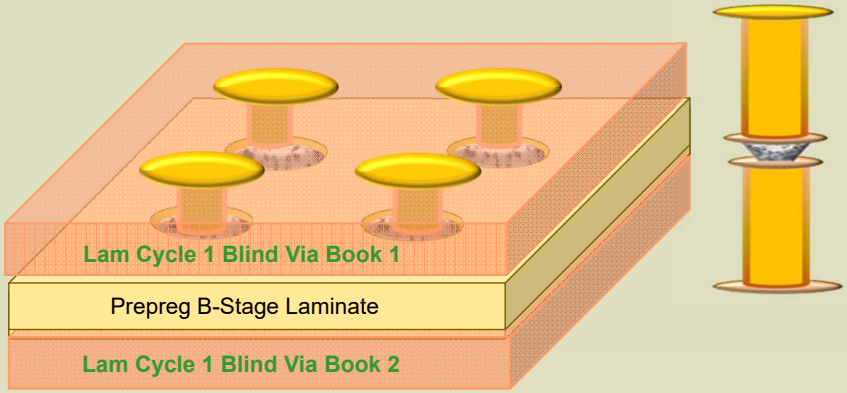
Viabond Process

- Begin with a sheet of prepreg
- Laser drill holes in the prepreg
- Fill holes with sintering paste



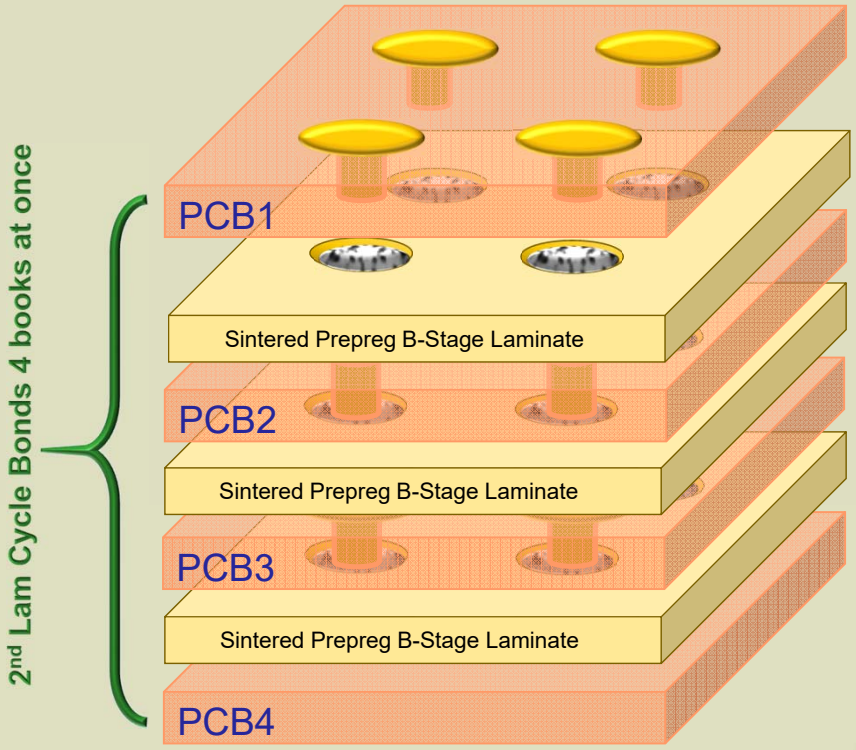
Viabond Process

- Begin with a sheet of prepreg
- Laser drill holes in the prepreg
- Fill holes with sintering paste
- Bond books together with sintered prepreg



Viabond Process

- Drill Flute length limits PCB thickness only in individual books
- Overall thickness can now be 400, 500, even 600 mils
- 2 lamination cycles
  - Books 1 - 4 are processed independently and in parallel
  - 4 boards/books bonded together in a 2nd lamination step



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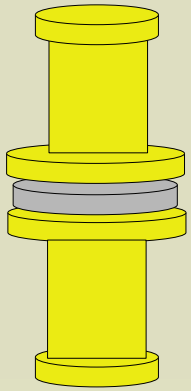
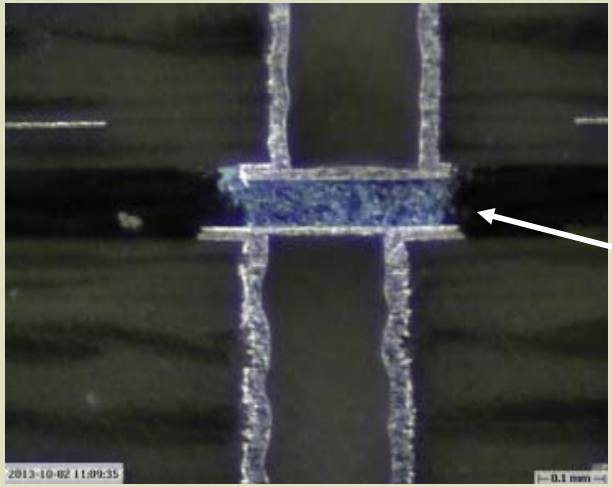
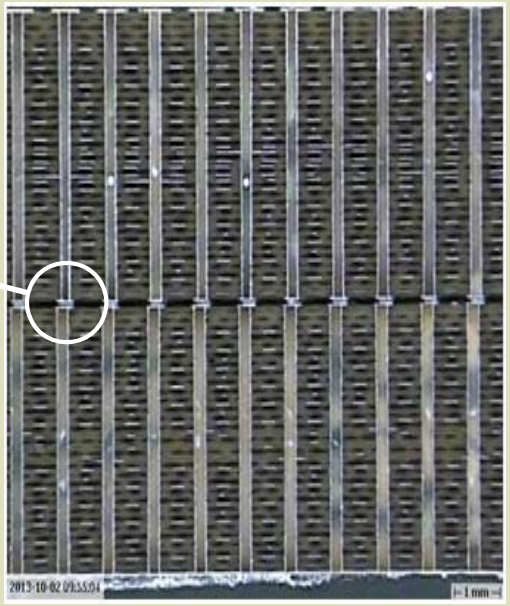
Technology Extender: Viabond

- Vias are bonded together using sintering paste

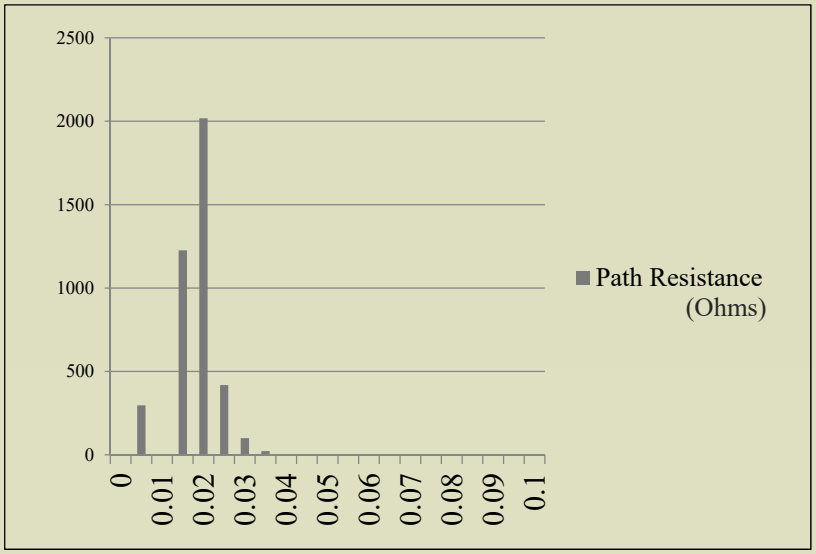


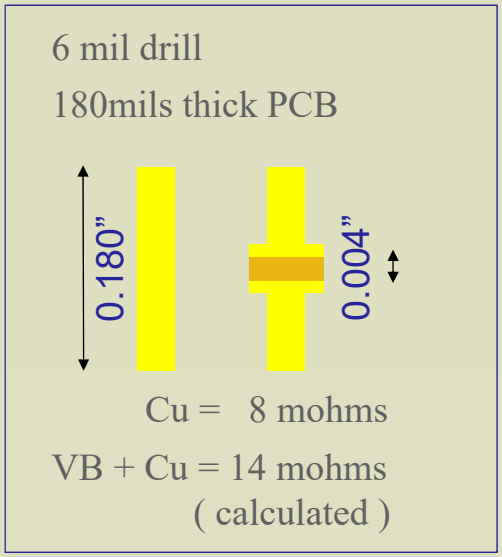




Viabond Path Resistance

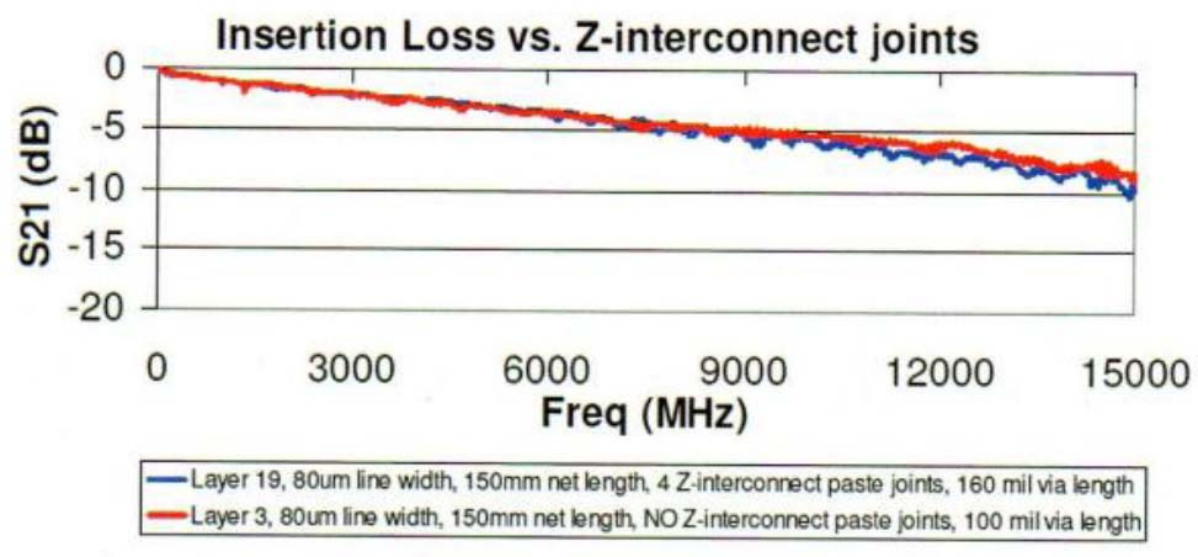
- Delta in path resistance between Cu and Viabond is negligible for signal integrity (SI) purposes, but may not be negligible for power integrity (PI) purposes

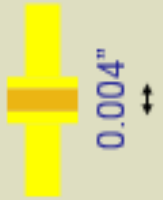




Viabond Signal Integrity

- Maintains signal integrity through 15Ghz when signal path traverses vias, Cu-only vs Cu + sintering paste



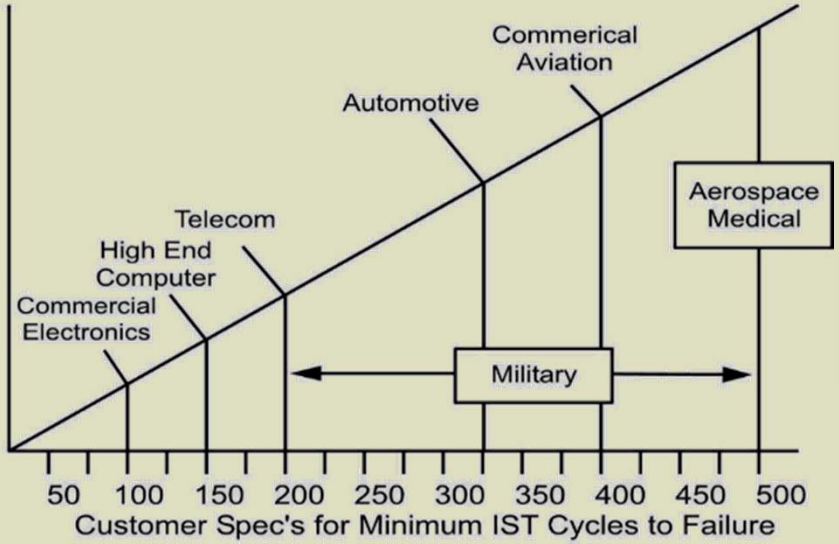


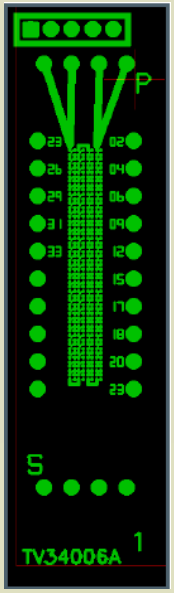
~ 150um
~ 1ps prop delay
~ Invisible to 100GHz

Source: Endicott Interconnects

Viabond Reliability

- Interconnect Stress Test (IST) to same standard as Harbor's traditional PCBs
  - IPC-TM-650, Method 2.6.26
  - Precondition: 9 x lead free reflow cycles
  - Test: 1000 x 25°C-125°C thermal cycles
- 0 failures





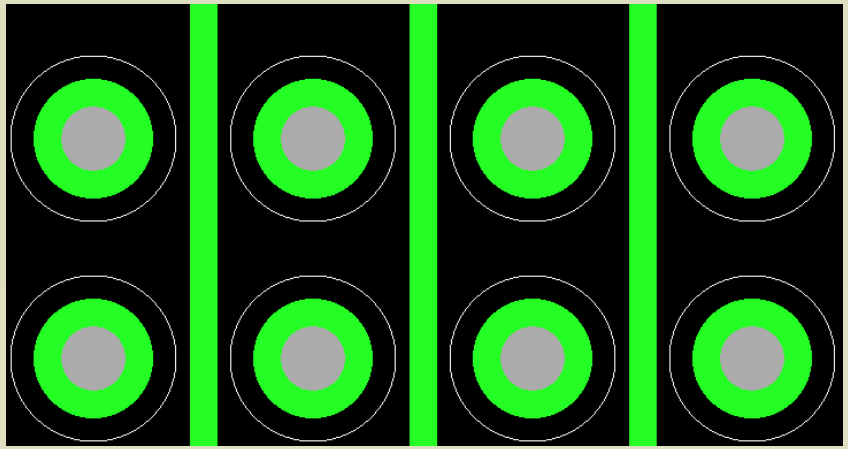
Source: PWBcorp

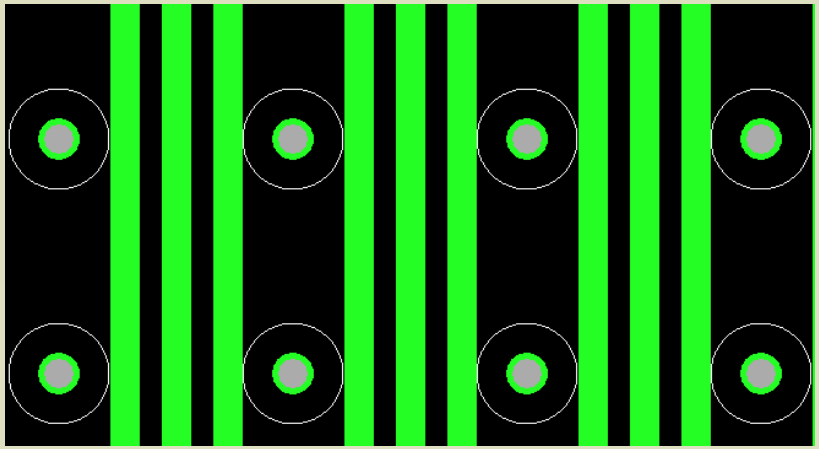
Viabond Yield

- Yield presented the biggest challenge, took a long time to get right
- Now approaching parity with the more traditional PCB fabrication techniques
  - Sintering paste recipes are straightforward
  - Applying to ATE PCBs is another matter
  - Large form factor PCB, large number of vias
  - In-process metrology is key (AOI, Kelvin flying probe test)

Viabond Applications

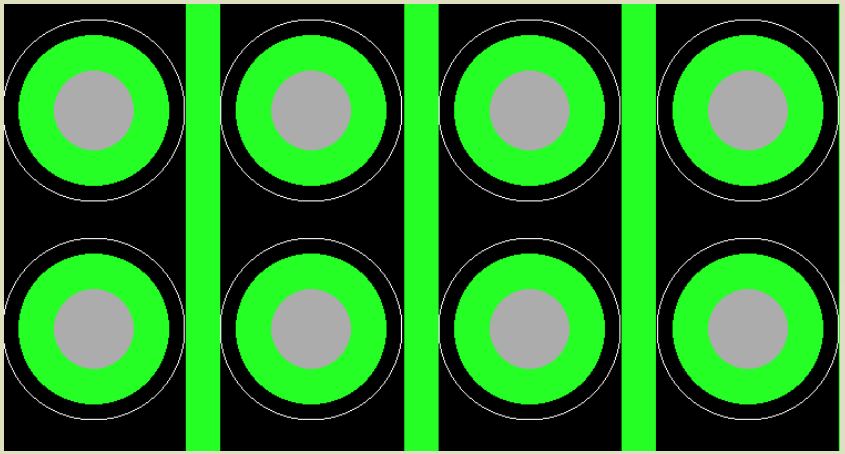
- Overall layer count can be reduced by improving DUT area breakout routing density
- 1mm pitch: 3:1 layer reduction in signal layers

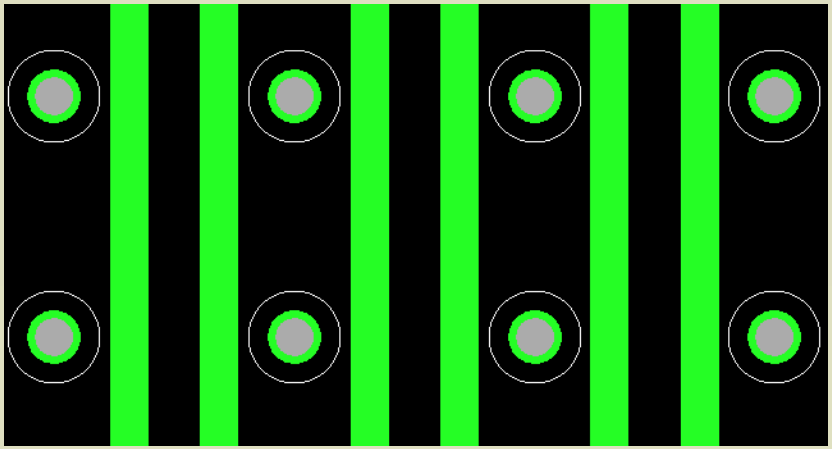




Viabond Applications

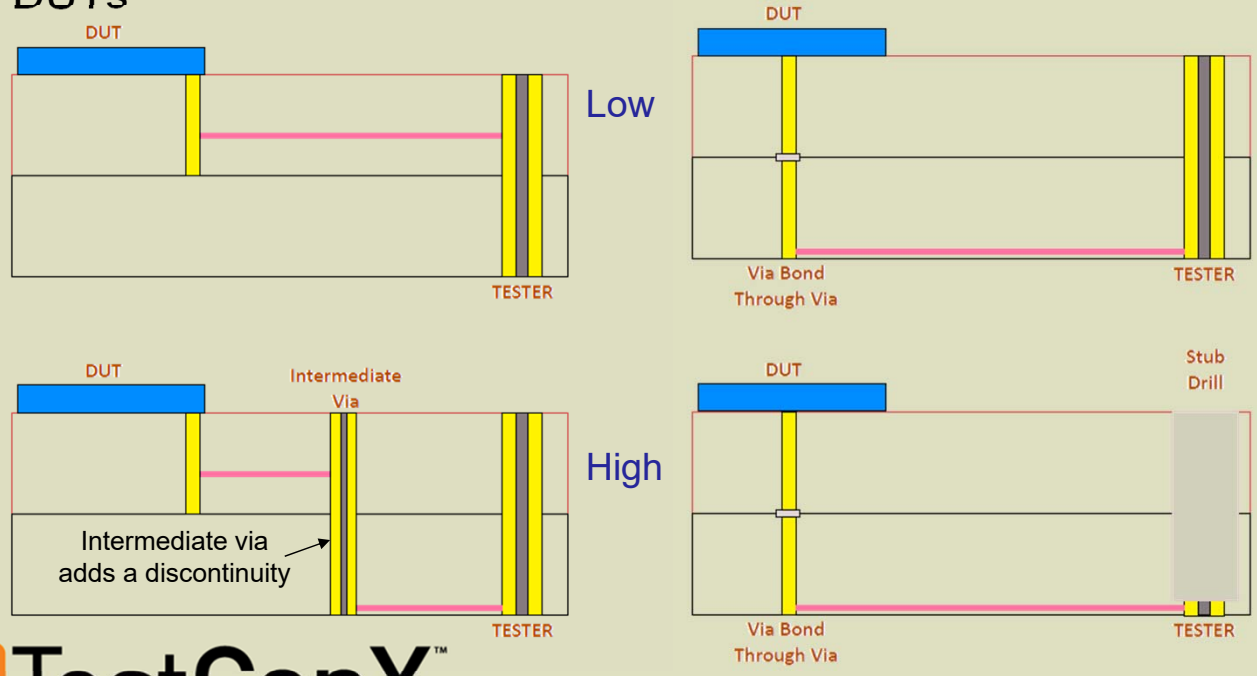
- 0.8mm pitch, 2:1 layer count reduction





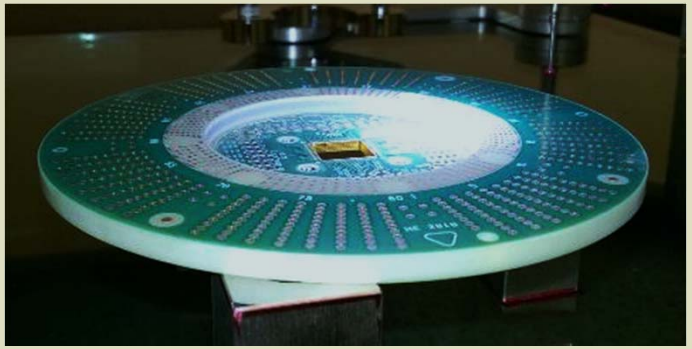
Viabond Applications

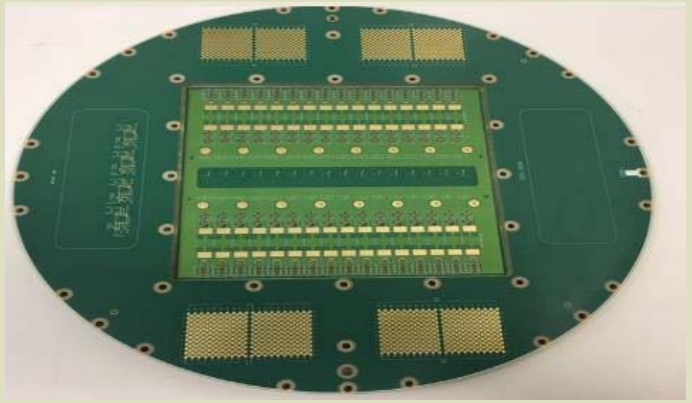
- Simplifies fanout, improves signal integrity for fine pitch / High pin count DUTs



Noteworthy Viabond Applications

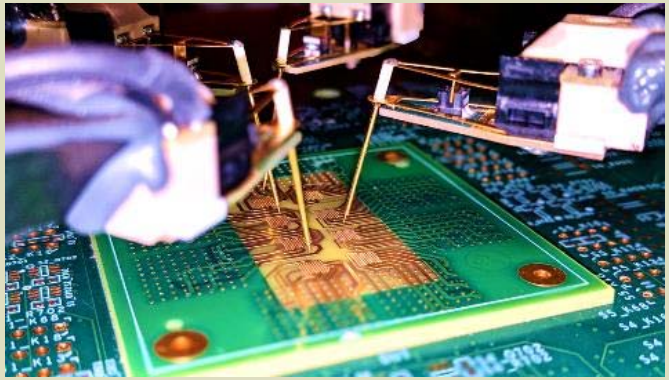
- Multi-tier PCB
  - 0.65 mm pitch, 0.590” thick PCB
  - Recessed cavity
  - 10,000 Viabond interconnections
  - Board alone weighs 25 pounds!
- Multi-tier PCB
  - 0.35mm pitch, 0.310” thick PCB
  - Recessed cavity, 16x site
  - 36 layers





Noteworthy Viabond Applications

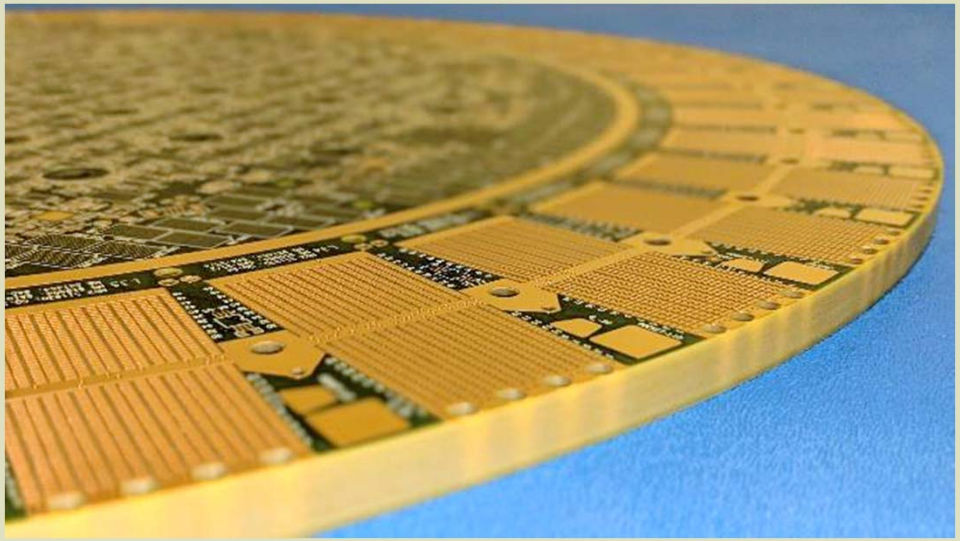
- Motherboard – Daughterboard
  - Daughterboard:
    Fine pitch, higher cost PCB
  - Motherboard:
    Gross pitch, low cost PCB



  - Space transformation from PCB pitch to IC package pitch
    - At DUT site or to adapt to specialty component footprints

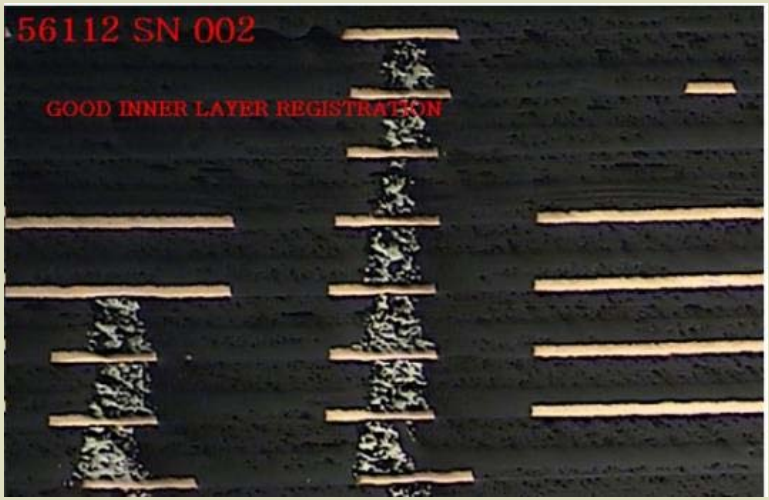
Noteworthy Viabond Applications

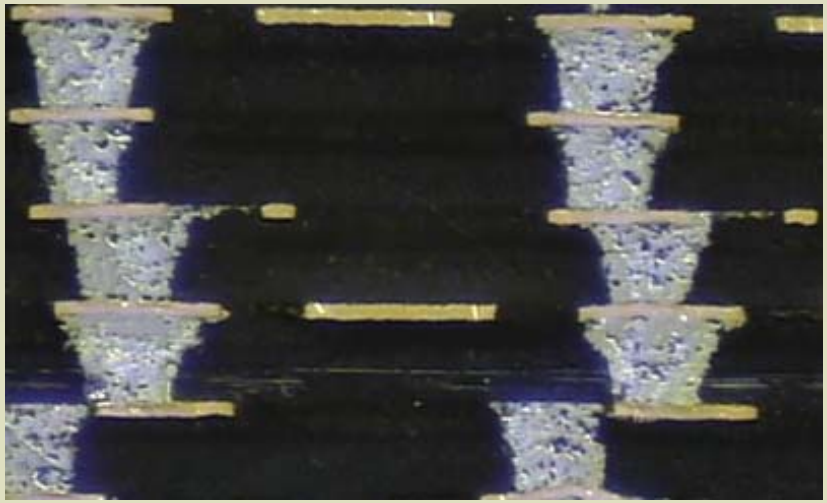
- Memory test application
  - 0.335” thick PCB
  - 0.50mm pitch
  - 81 layers
  - 3 books, 2 Viabond layers
  - 100,000 Viabond junctions



Future Applications for Viabond

- Stacked microvias using Viabond
  - Alternative to traditional HDI (multi lamination) techniques
  - Development is WIP / Ongoing





Future Applications for Viabond

- Incorporate fully additive 3D printed solutions
  - Conductor dimensions at 3mil line and space now
  - ATE XYZ dimensions not yet available, ATE layer counts not yet available
  - Hybrid structures may have legs:
    - 3D printed small feature structure laminated to standard PCB using Viabond
- To Be Determined
  - Depends on Customer Creativity

Viabond Next Steps

- In-depth Power Integrity characterization
- Signal Integrity / via tuning
- Simulation to measurement correlation
- In-process metrology continuous improvement
- Stacked via characterization
- Space transformer integration studies
  - Flatness
  - Design & fabrication timeline compression

Summary:

- Viabond extends the reach of what can be achieved in the ATE Interface PCB
  - Thicker, high aspect ratio, high layer count PCBs
  - Fine pitch holes (small drills) through thick PCBs
  - Alternative to sequential lamination, with fewer lamination cycles

	Flip Drilling	Multiple Laminations	Backdrilling	UltraFlat	Viabond
Layer Count	⊗	⊗	⊗		⊗
DUT Pitch	⊗	⊗	⊗		⊗
Routing Density		⊗	⊗		⊗
Signal Integrity		⊗	⊗		⊗
Power Delivery	⊗	⊗			⊗
Direct Attach				⊗	⊗