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Archive



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## Applications of AI and Machine Learning in Interposer PCB Design

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## Agenda

- Interposer, design process, and bottlenecks
- Challenges of manual layout
- Limitations of legacy auto and interactive routers
- New AI-based smart router architecture and themes
- Case studies
- Summary
- Next steps

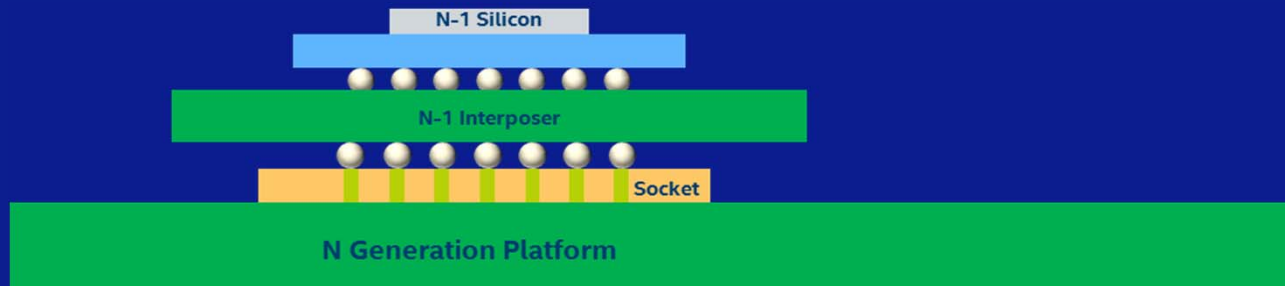


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## Interposer Usage Model



- Use of N-1 interposer with previous generation silicon to validate next generation platform
- Facilitate platform checkout and early deployment before new silicon arrival

## N-1 Interposer Design Process

- Collect customers' requirements
- Define the pin mappings between N and N-1 silicon chips
- Netlist generation using System Architecture or scripts
- PCB board stackup planning
- Layout constraints creations
- Board components placement and routings
- Layout review including Signal Integrity (SI) and Power Integrity (PI) optimizations



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## Technical Challenges

- High density and high pin count package
- Very small Interposer geometry and limited routing space
- Irregular routing patterns
- Complex and stringent constraints including SI/PI requirements
- Iterative process to get the optimal routing solution

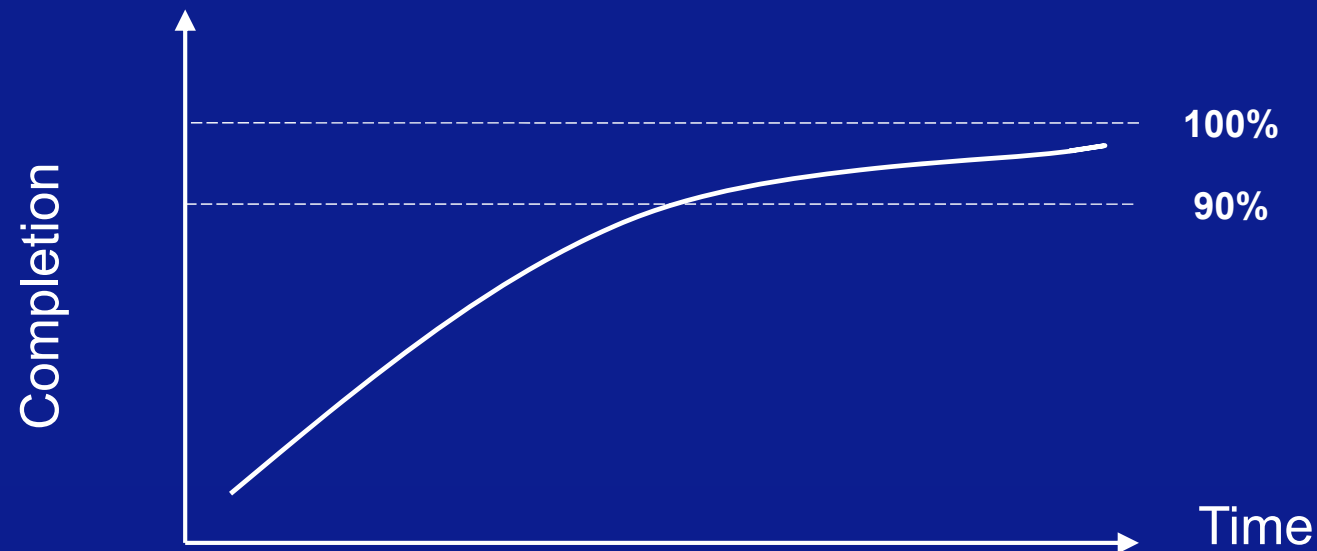


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## Layout Efficiency Bottlenecks





## Manual Routing Challenges for Complex Design

- Most of the time is spent to route the remaining 10% nets
- If no satisfactory solution is found, most of previous routings have to be erased
- Have to explore new strategies and start over
- This manual trial and error process continues until all nets are routed



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## Manual Routing Inefficiency

- Iterative process and needs user intervention
- Sequential process and only one strategy can be done at a time
- Very labor intensive
- Costly on time and layout resources
- Low return on investment

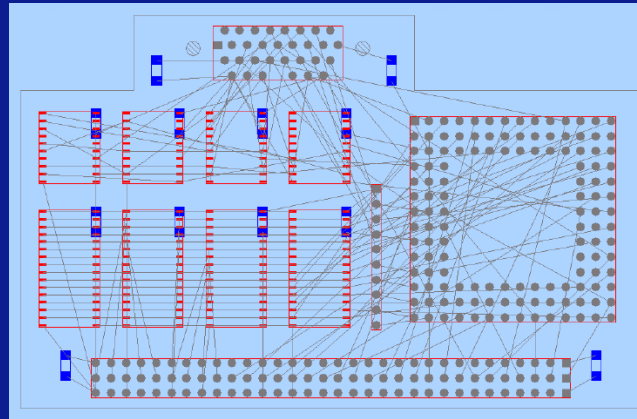


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## Legacy Auto Routing Process



- Use GUI and Do script files. Ok for very simple board
- Significant time has to be spent on debugging DO file and scripts
- Multiple steps process

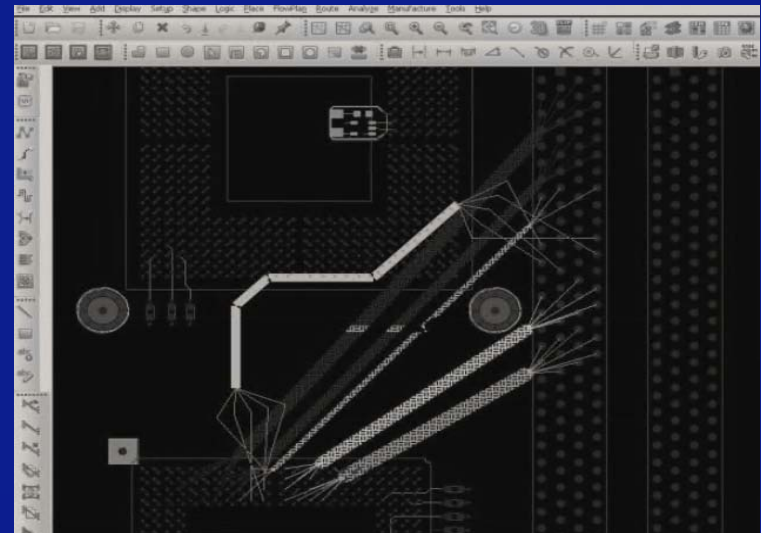
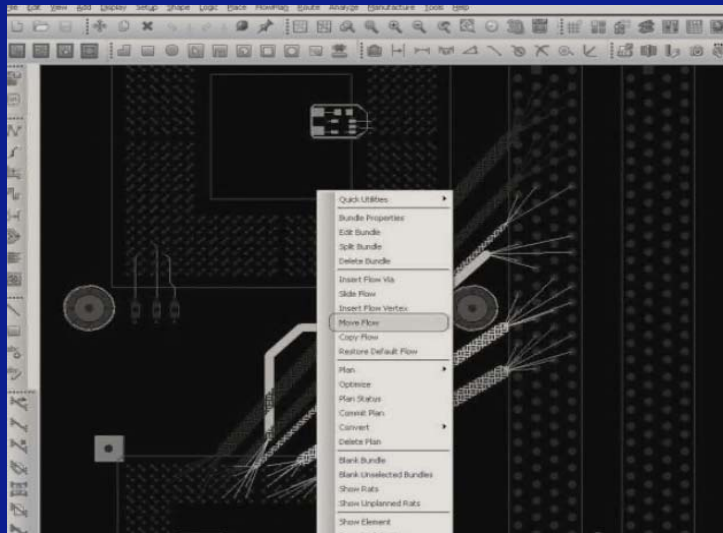


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## Modern Interactive Routers (GRE)



Use of bundles to pass design intent. Time consuming. Need user interventions.



## A New AI Smart Router

- Ultimate one click operation, smart and fully automatic
- No user involvement once setup is completed
- Can handle complex irregular PCB layout such as interposers
- AI smart router integrates multiple tools such as OrbitIO, package router, and PCB editor

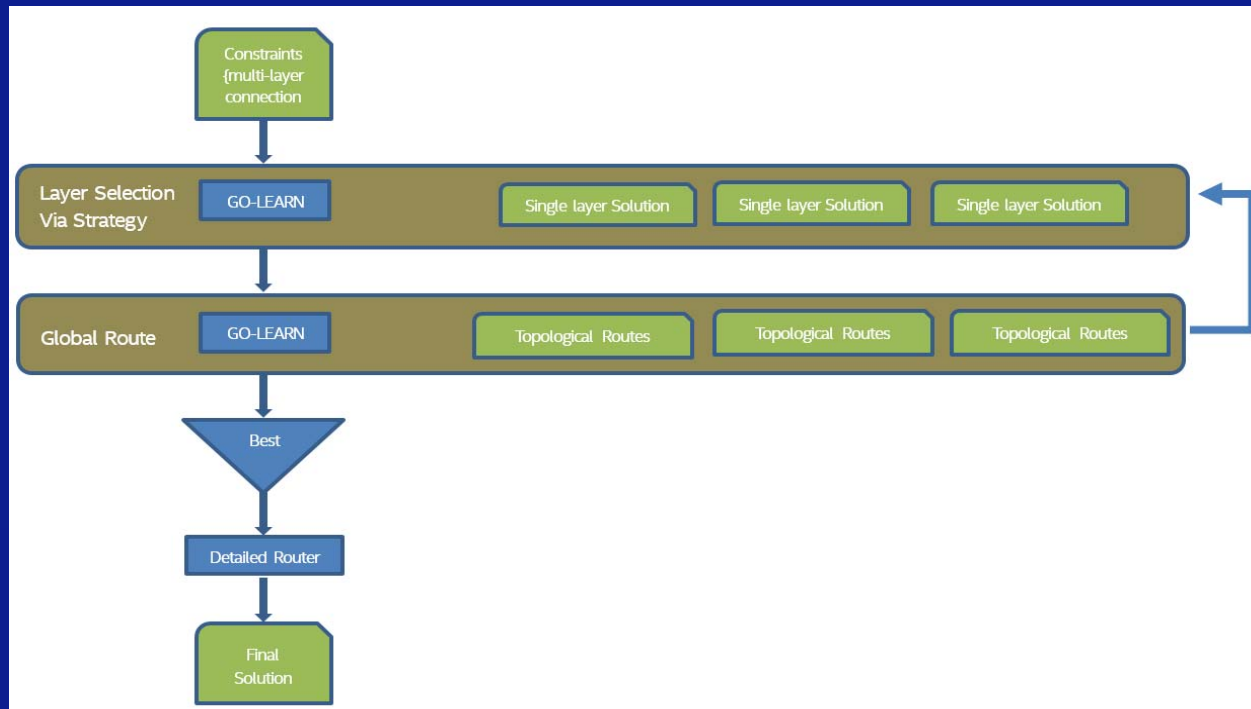


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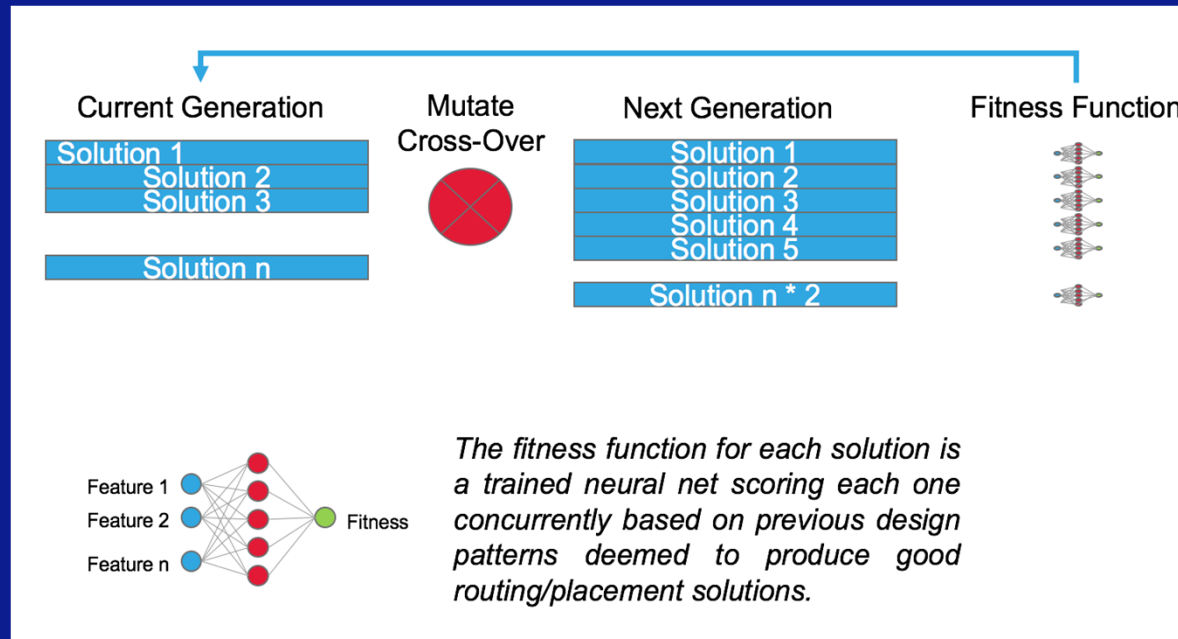
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## AI Smart Router Flow



## Machine Learning Based AI Router



## AI Routing Process

- AI global router is used for topological routing
- Via patterns exploration and learning
- A detailed router transforms the topological routes into serpentine routes
- Delay and phase tuning
- Global and detailed routers co-optimization



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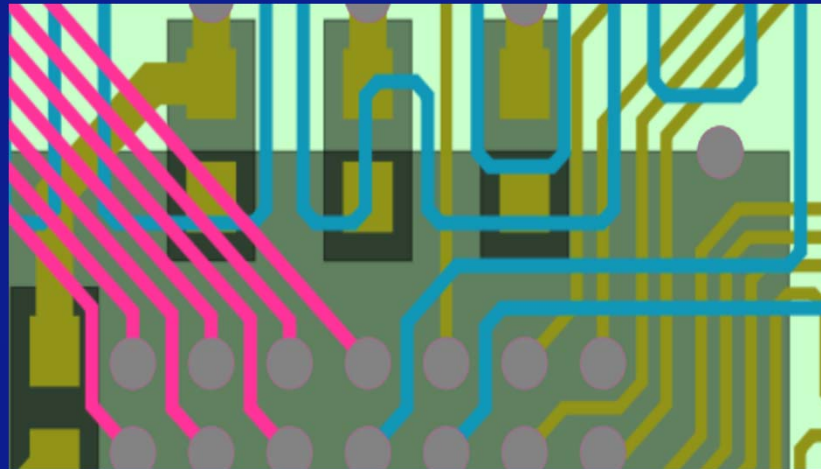
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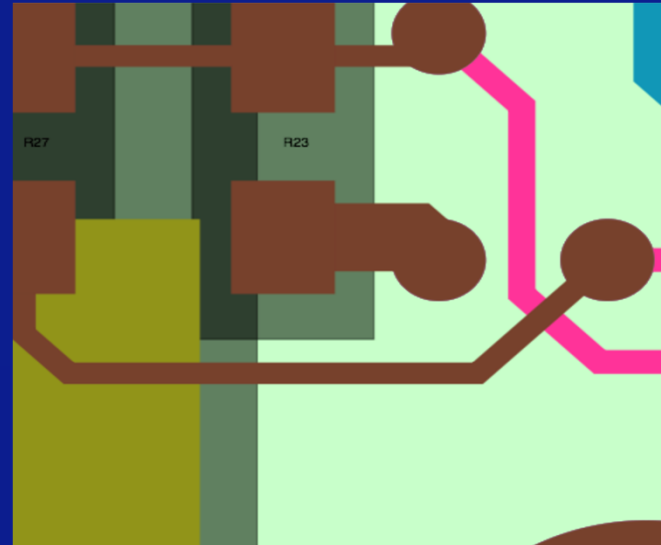
## Via Patterns Learning

- Dense BGA escape patterns, where concentric rings of pins must escape to different layers

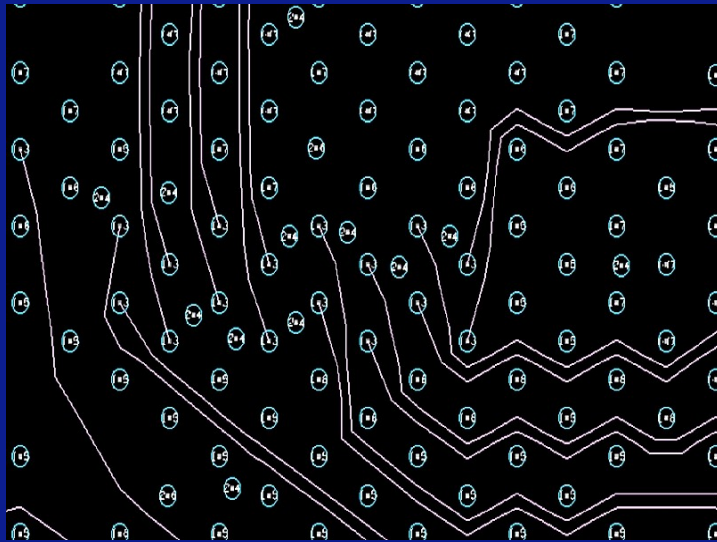


## Via Patterns Learning

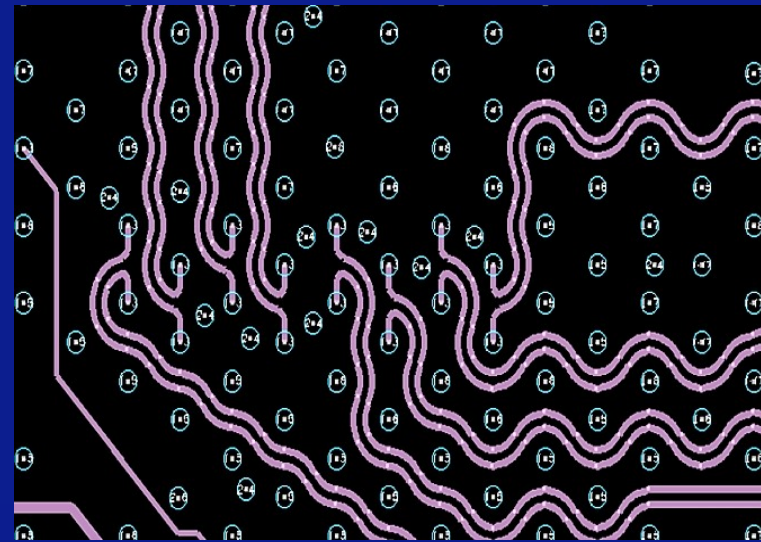
- Via transitions to use layer directionality to relieve congestion



## Routing Process Comparison

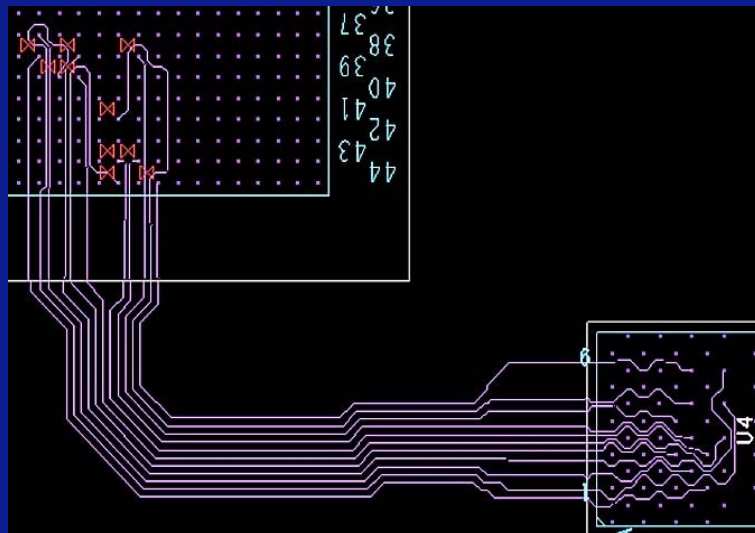


Topological routes as a result of the AI global router

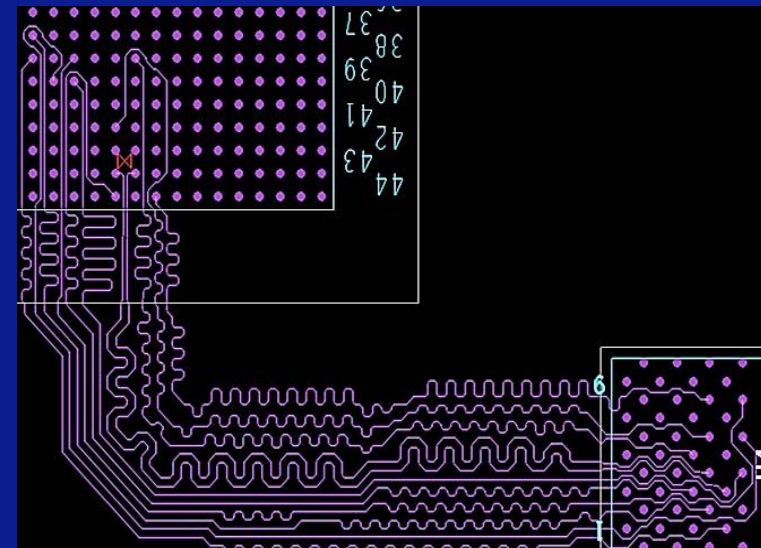


Transformed snake routes from the detailed router

## Delay and Phase Tuning



Routings prior to delay and phase tuning



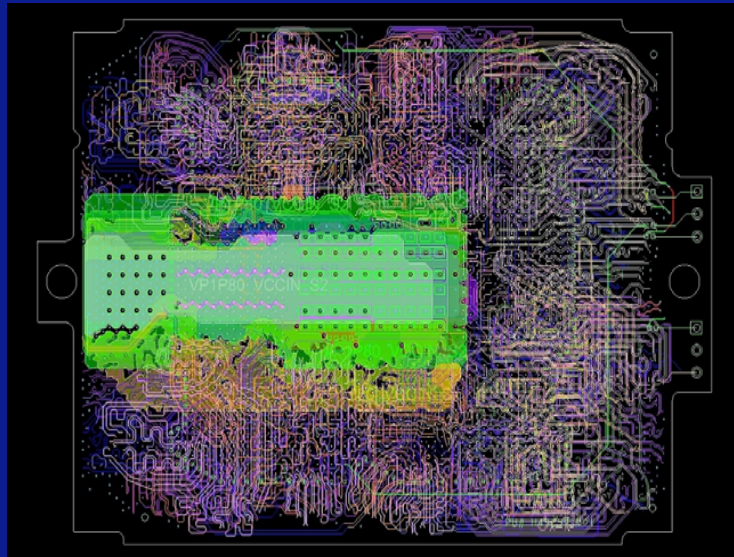
Routings after delay and phase tuning



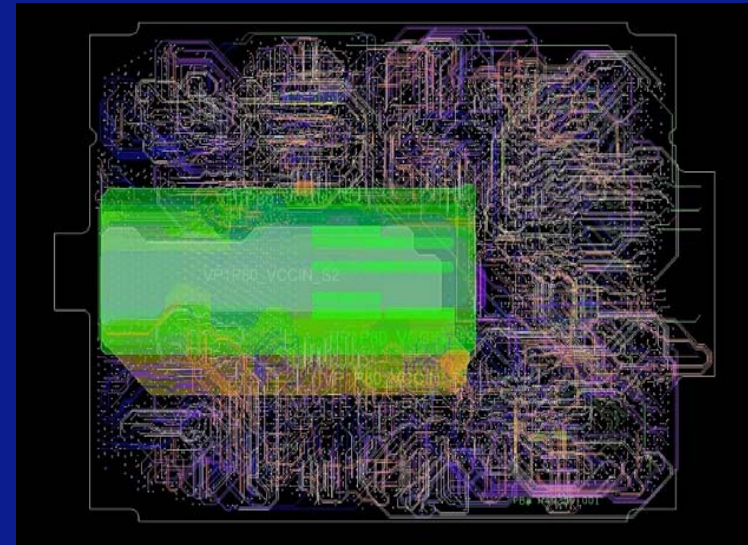
## Routing Methods Comparison

	Manual Routing	Legacy Auto Router	AI Smart Router
Stackup planning	✓	✓	✓
Constraints creation	✓	✓	✓
Components placement	✓	✓	✓
Routing	Manual and interactive	Using DO files and need debugging	No any user involvements
Speed	Labor intensive. Very slow	Improved speed for some simple designs	Full automatic and very fast

## Auto Router Comparisons- Test Case 1



Manually routed and tuned N-1 CPU interposer  
Routing time: ~120 hours



Automatic routings using the AI Global router.  
Routing time: ~ 30 minutes

**Total number of routed nets > 1000**

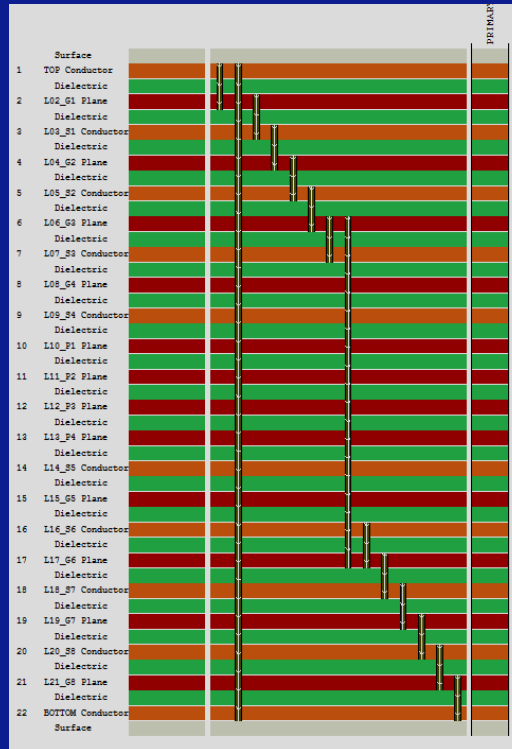


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## Interposer Stackup and Routing Constraints



Worksheet Selector ... skx\_ep\_ppo1

Physical		Objects	Referenced Physical C Set
Type	S	Name	
Bus		DMI_TX_DP (4)	85OHM_DIFF
Bus		PCIE_P1_RX_DN (8)	85OHM_DIFF
Bus		PCIE_P1_RX_DP (8)	85OHM_DIFF
Bus		PCIE_P1_TX_DN (8)	85OHM_DIFF
Bus		PCIE_P1_TX_DP (8)	85OHM_DIFF
Bus		PCIE_P2_RX_DN (16)	85OHM_DIFF
Bus		PCIE_P2_RX_DP (16)	85OHM_DIFF
Bus		PCIE_P2_TX_DN (16)	85OHM_DIFF
Bus		PCIE_P2_TX_DP (16)	85OHM_DIFF
Bus		PCIE_P3_RX_DN (16)	85OHM_DIFF
Bus		PCIE_P3_RX_DP (16)	85OHM_DIFF
Bus		PCIE_P3_TX_DN (16)	85OHM_DIFF
Bus		PCIE_P3_TX_DP (16)	85OHM_DIFF
Bus		QPI_P0_RX_DN (20)	85OHM_DIFF
Bus		QPI_P0_RX_DP (20)	85OHM_DIFF
Bus		QPI_P0_TX_DN (20)	85OHM_DIFF
Bus		QPI_P0_TX_DP (20)	85OHM_DIFF
Bus		QPI_P1_RX_DN (20)	85OHM_DIFF
Bus		QPI_P1_RX_DP (20)	85OHM_DIFF
Bus		QPI_P1_TX_DN (20)	85OHM_DIFF
Bus		QPI_P1_TX_DP (20)	85OHM_DIFF
DPr		A_CPU_VCCIN_SENSE_	SENSE_DIFF
DPr		DDR_CH0_CLK_0	38OHM_DIFF
DPr		DDR_CH0_CLK_1	38OHM_DIFF
DPr		DDR_CH0_CLK_2	38OHM_DIFF
DPr		DDR_CH0_CLK_3	38OHM_DIFF
DPr		DDR_CH0_DQS_0	38OHM_DIFF
DPr		DDR_CH0_DQS_1	38OHM_DIFF
DPr		DDR_CH0_DQS_2	38OHM_DIFF
DPr		DDR_CH0_DQS_3	38OHM_DIFF
DPr		DDR_CH0_DQS_4	38OHM_DIFF
DPr		DDR_CH0_DQS_5	38OHM_DIFF
DPr		DDR_CH0_DQS_6	38OHM_DIFF
DPr		DDR_CH0_DQS_7	38OHM_DIFF
DPr		DDR_CH0_DQS_8	38OHM_DIFF
DPr		DDR_CH0_DQS_9	38OHM_DIFF
DPr		DDR_CH0_DQS_10	38OHM_DIFF
DPr		DDR_CH0_DQS_11	38OHM_DIFF
DPr		DDR_CH0_DQS_12	38OHM_DIFF
DPr		DDR_CH0_DQS_13	38OHM_DIFF
DPr		DDR_CH0_DQS_14	38OHM_DIFF
DPr		DDR_CH0_DQS_15	38OHM_DIFF
DPr		DDR_CH0_DQS_16	38OHM_DIFF
DPr		DDR_CH0_DQS_17	38OHM_DIFF

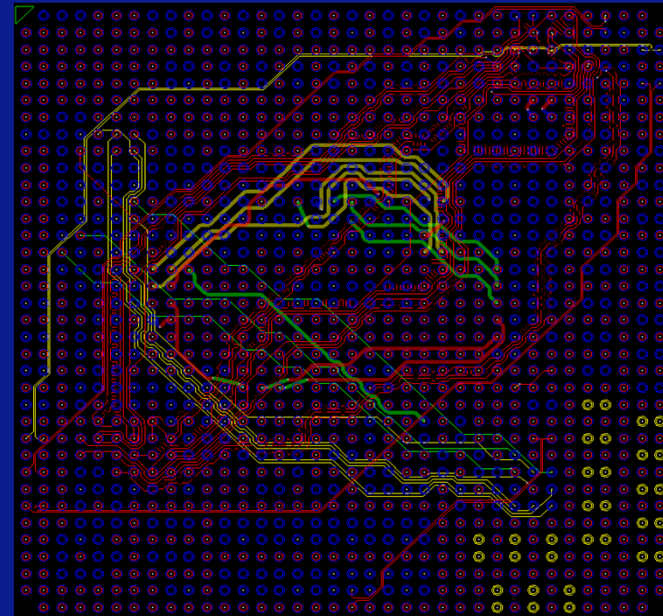
Physical Constraint Set  
 Net  
 Region  
 All Layers  
 All Layers

Spacing  
 Same Net Spacing  
 Assembly  
 Manufacturing  
 Properties  
 DRC

## Auto Router Comparisons- Test Case 2



Manual layout time: ~16 hours



AI smart router routing time: ~5 minutes



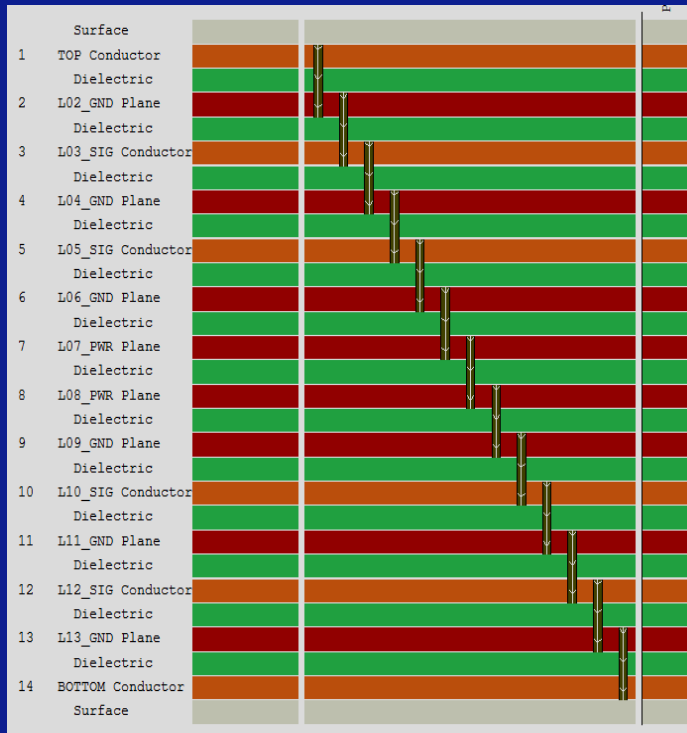
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## Interposer Stackup and Routing Constraints



Worksheet Selector ..

Electrical

Physical

Physical Constraint Set

- All Layers
- Net
- All Layers
- Region
- All Layers

Spacing

Same Net Spacing

Assembly

Manufacturing

Properties

DRC

alb\_ivy\_n-1\_interposer

Type	S	Objects	Referenced Physical CSet
Type	S	Name	
Dsn	*	alb_ivy_n-1_interposer	DEFAULT
NGrp	⊞	JTAG (5)	45OHM_SE
NGrp	⊞	PCIE (32)	80OHM_DIFF
NGrp	⊞	RCOMP (17)	254MICRON
NGrp	⊞	VISA_GRP0 (9)	45OHM_SE
NGrp	⊞	VISA_GRP1 (9)	45OHM_SE
DPr	⊞	A_VCCANA_PCIE_SENSE	254MICRON
DPr	⊞	B_CLK_PGC	80OHM_DIFF
DPr	⊞	B_CLK_25M	80OHM_DIFF
DPr	⊞	B_CLK_133M	80OHM_DIFF
DPr	⊞	PCIE_HIP_BI_COM0_RCLK	80OHM_DIFF
Net		CO10_TCP_POWERGOOD	45OHM_SE
Net		CO10_TCP_RST_L	45OHM_SE
Net		C10_TCP_STRAP0	45OHM_SE
Net		C10_TCP_STRAP1	45OHM_SE
Net		EDM0	45OHM_SE
Net		EDM1	45OHM_SE
Net		GND	508MICRON
Net		PCIE_HIP_BT_COM0_DFX_DMON0_OBS	45OHM_SE
Net		PCIE_HIP_BT_COM0_DFX_DMON0_OBS	45OHM_SE
Net		THERMDA	45OHM_SE
Net		THERMDC	45OHM_SE
Net		VP0P85_VCCDIG_PCIE_PAD_LV	508MICRON
Net		VP1P0_VCCANA_PCIE_PAD_LV	508MICRON
Net		VP1P0_VCCA_CLK_DEF_100_PAD_LV	508MICRON

All Layers

## Summary

- Interposer PCB layout is a complex and time consuming process
- Manual and legacy routing methods are not efficient
- AI smart router revolutionizes this process and achieves significant time and resource savings



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## Next Steps

- Extend AI routing capability to generic PCB board layout
- Components placement optimization
- Provide flexible routing control options such as routing by interfaces or regions



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## Acknowledgements

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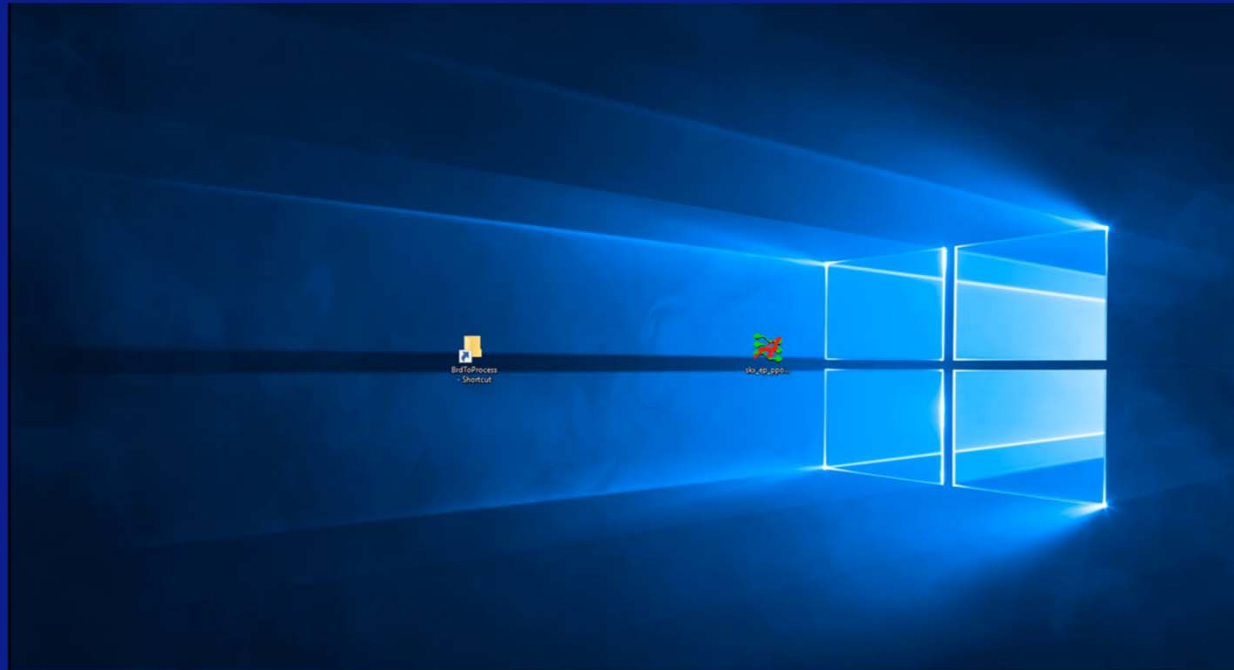


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## AI Smart Router Server Demo



Please see online demo at:



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