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Motherboard, Daughter Cards, and Lowering the Cost of Test

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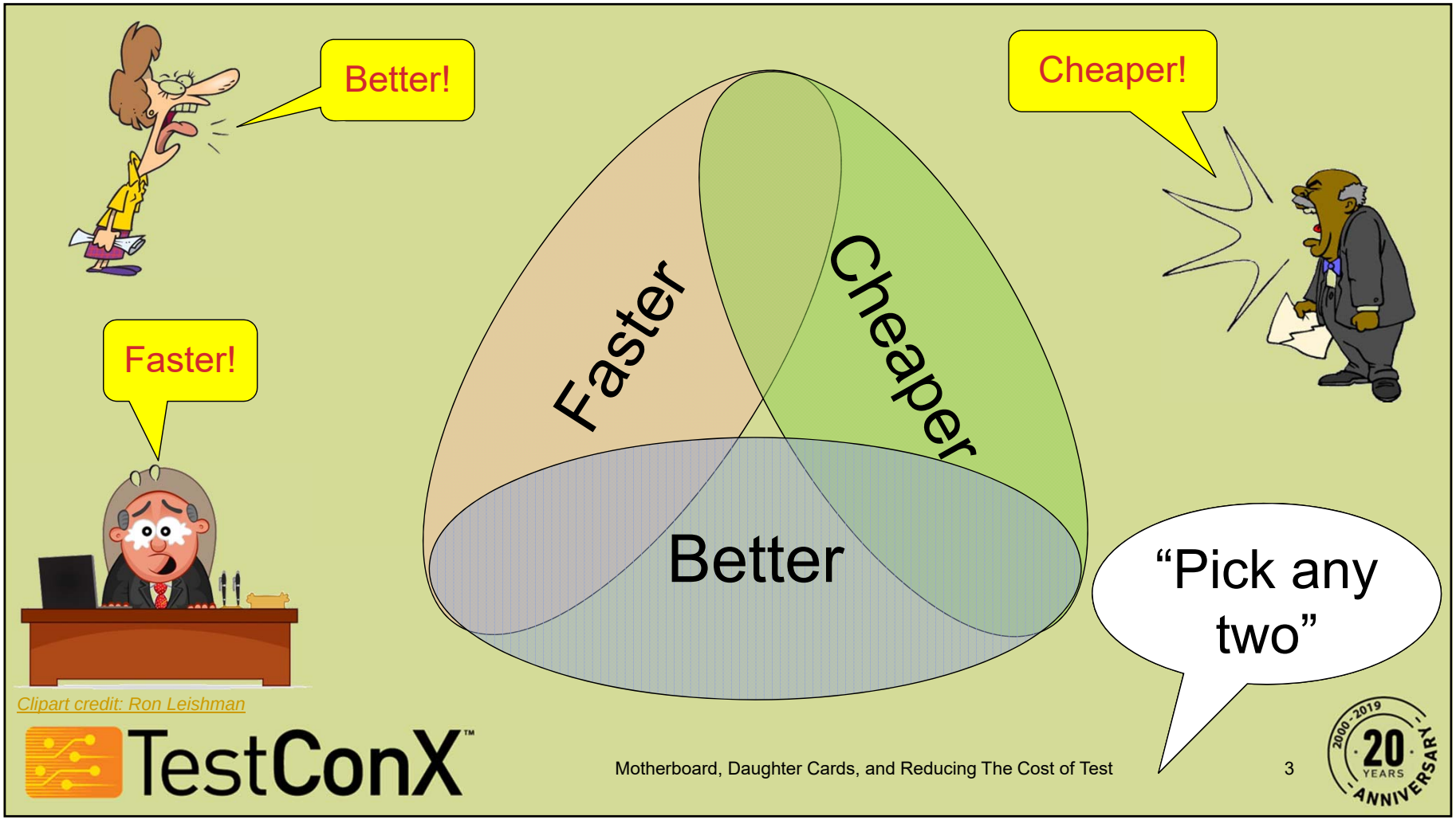
The Story

Broadcom came to R&D Altanova 5 years ago with the desire to build a Motherboard (MB) / Daughter-Card (DC) solution to lower the cost of test. Since that time they've continued to use this strategy to save hundreds of thousands of dollars.

There are been many improvements and modifications to keep this solution working for each new generation of test requirements.


Better!
Cheaper!
Faster!
Faster
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Better
"Pick any two"
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Motherboard, Daughter Cards, and Reducing The Cost of Test
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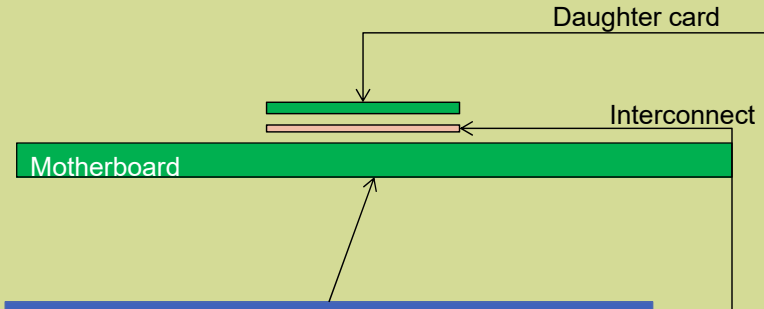
How does a MB / DC help us?

Package Test Solution Shown



Daughter Card
- Application specific
- Can be a simple space-transformer

Motherboard
- Reusable
- Superset motherboard
- Includes common circuits
- Normalized power schemes

Interconnect
- Reusable
- Breakable

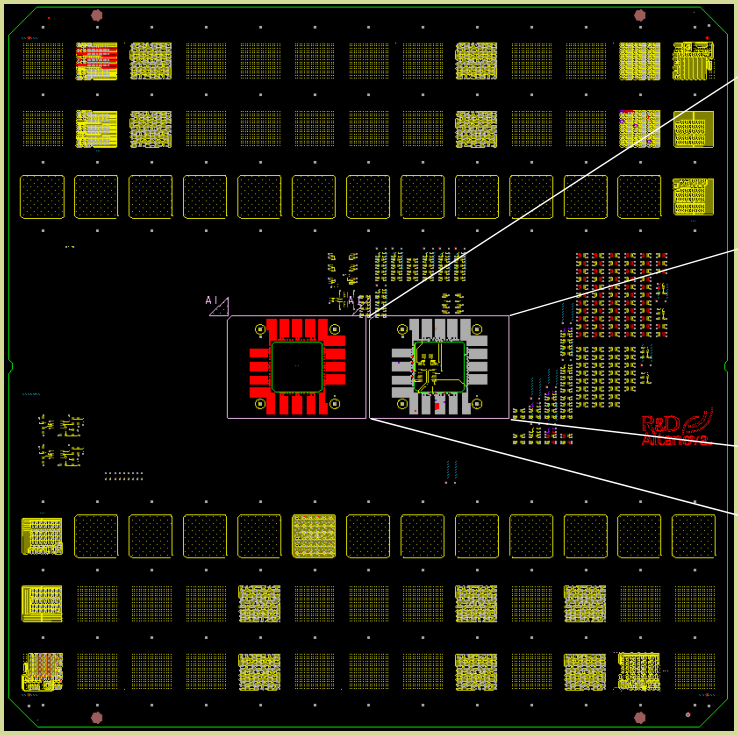
Modern Market Demands for New Designs

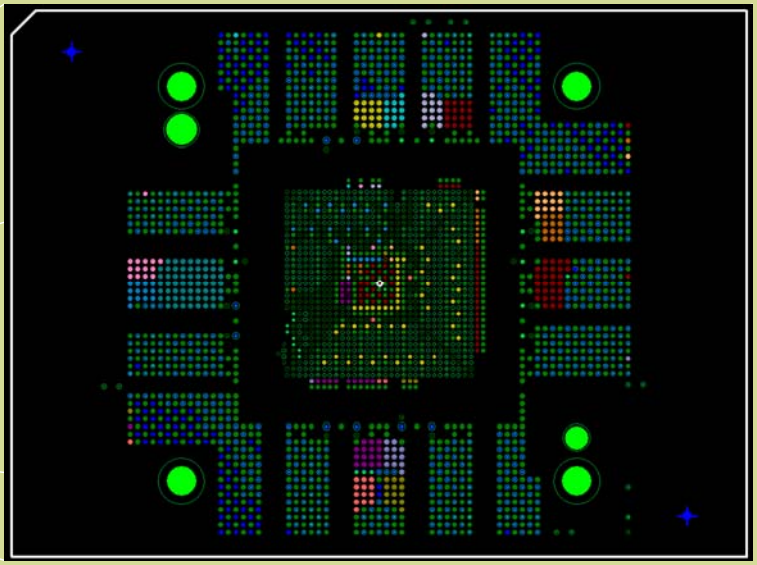
- More complex designs
- Higher performance (Signal speed & power integrity)
- Faster (Quicker design and fab)
- Cheaper

Motherboard / Daughter card concept helps these two market needs!

Extra interconnects can only hurt performance, so how do we minimize MB / DC performance impacts?

Example MB / DC Design Solution





- Multi-site solution
- 16 Gbps design
- ~1000 pin DUT

Motherboard / Daughter-Card Benefits

- Daughter Card Design Cycle
  - DC design time | 3-7 working days
  - Fabrication time | 3-10 working days
  - Assembly | 1-2 working days
  - Test | 1 day

A critical board can go from concept to FedEx in as little as 8 working days!

Where Does This Make Sense?

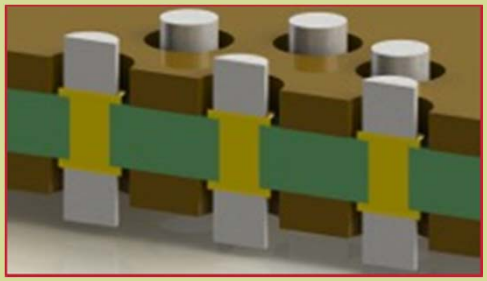
- Designs require a fixed motherboard that has normalized tester instrument requirements
- Families of parts with similar requirements
- Repetition of circuits on the motherboard

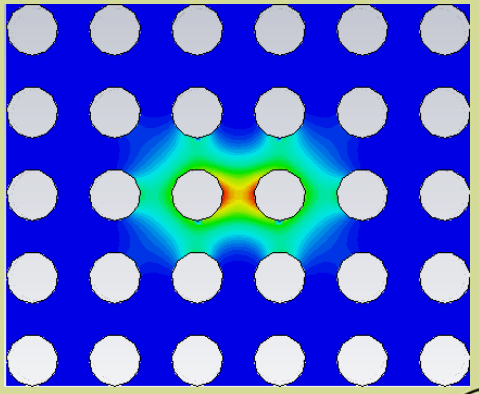
Limits of the MB / DC

- Upper limits are impossible to qualify so we can only list current boundaries
  - 8 site MBs
  - 24 Gbps
- Custom circuits
- Not a great fit for part characterization

Signal Integrity Challenges: Interconnect

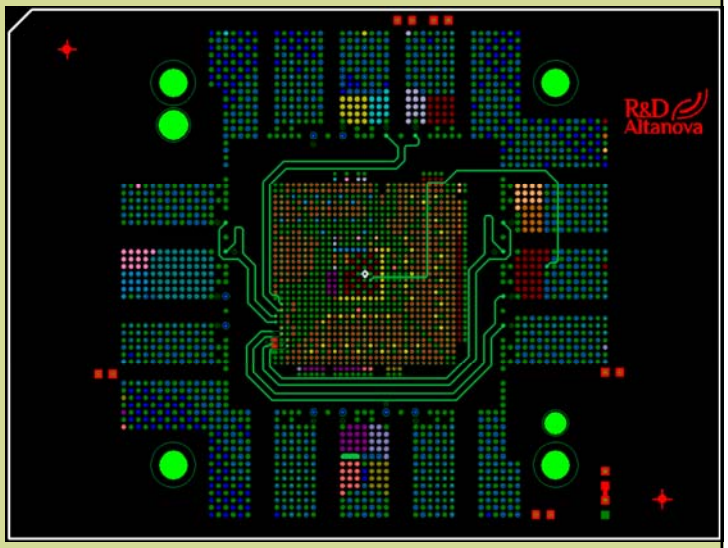
- Using an Invisipin® interconnect
- Optimizing the MB / DC connection
  - MB interconnect is arbitrary, so high speed signals can be simulated and optimized
  - This significantly minimizes the impact of the interconnect
- Elastomer interconnects are very short and have low inductance giving minimal impact to power integrity





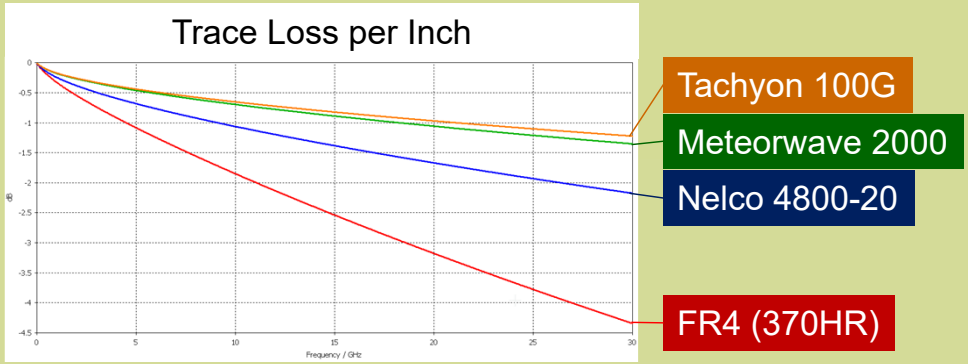
Signal Integrity Challenges: Indirect Routing

- Generic motherboard will always be inefficient in for a specific application
- Example: High speed signals are spread out around the perimeter in MB but they all route to a single location on the DUT



Signal Integrity – Trace Loss

- To reduce trace loss you must increase trace width or use a high performance dielectric
- Because MBs are reused its costs are amortized so it makes more sense to use high performance dielectrics



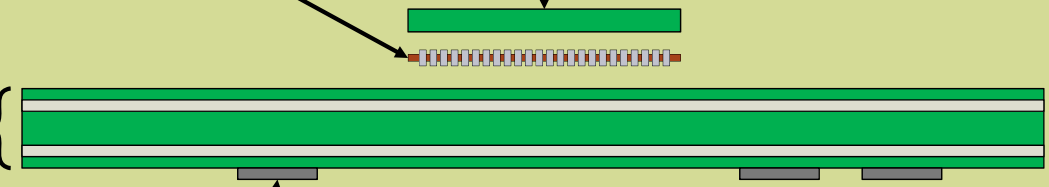
Power Integrity

- Power integrity can be improved by adding more power planes, but there will be an negative impact in motherboard vias from thicker boards
- Solutions that help with PI
  - Capacitors on DC
  - Embedded Capacitors in DC
  - Additional planes in DC
- PI solutions can reduce the advantage of the MB-DCs

Technology Summary

- Strategic layout for DC routing
- Low inductance pin for PI
- Optimized impedance for SI

- Simple space transformer
- Capacitors under DUT



- Increased layer count is ok
- Thicker high speed traces
- High performance dielectrics
- Simulated and optimized performance

- Reusable circuits
- Fixed Instrument set

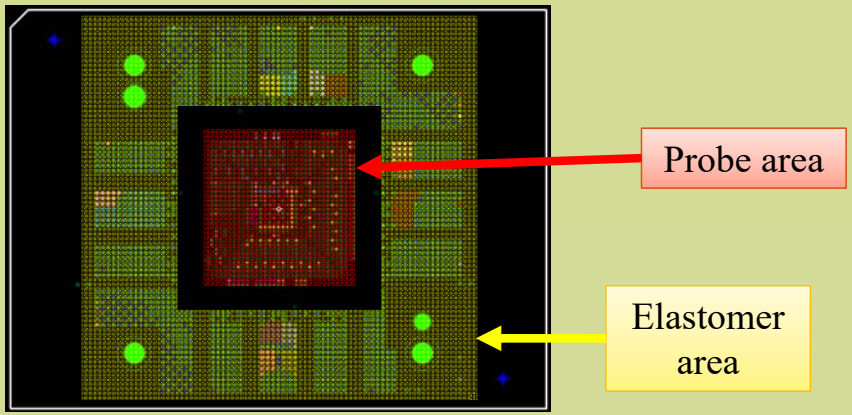
More complexity in motherboard, less in daughter-card

Other Advantages

- MB / DC designs have also been used
  - Add fine pitch probe WLCSP solutions
  - MB / DC packaged solutions down to 0.25mm pitch (usually not reusable designs!)
  - Add fine pitch memory near DUT

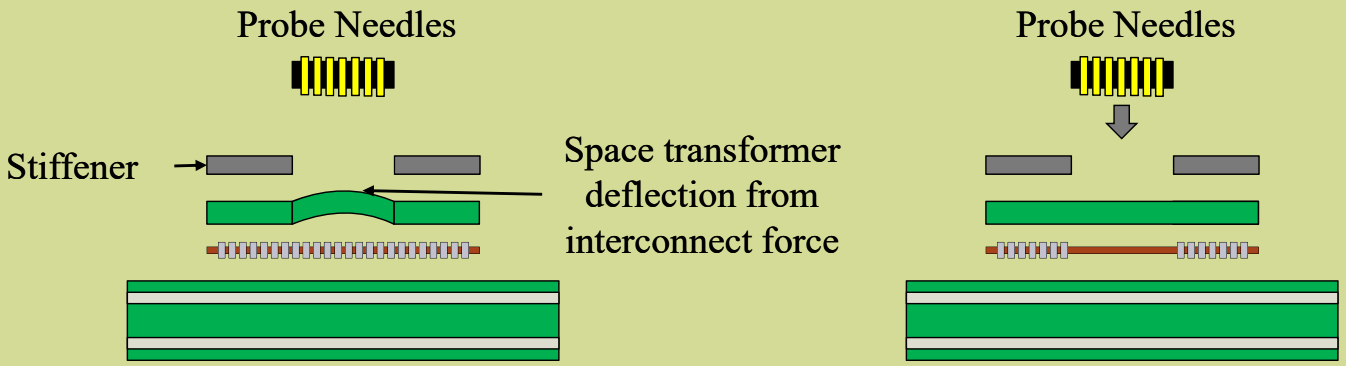
Mechanical Concerns

- Using MB / DC for wafer sort requires a focus on mechanical forces
  - Probe solutions require extreme flatness over probe area (Typically ≤ 50 um)
  - Elastomer interconnects require constant force to make connection and can lead to deflection



Simplest solution is to have elastomer interconnects and DUT interconnects offset in the Z-axis

Probe Card Considerations



- Moving compression interconnects out from under the DUT helps flatness specs
- If the space transformer is rigid enough then this is not required

Can We Build a Combination Final Test & Wafer Sort Motherboard?

- This is primarily limited by site-count and cost
- For a one or two sites Final Test (FT) board, we can build a superset Wafer Sort (WS) motherboard
- Large area substrates are expensive and our primary goal is to reduce cost
  - FT sites are positioned according to handler rules
  - Larger site counts will lead to unnecessarily large space transformers driven by handler rules
  - WS requires a space transformer, FT space transformer are per site

Lessons Learned at Broadcom

- It takes months to create a superset MB
- Managed to use only a few flavors of MBs to support the majority of their group's projects
- Some test requirements had to be cut in order to fit within the pre-defined MB options
- The strategy could not be used for any DUTs that required special circuitry. At these times they just reverted to single board load boards.
- They are struggling to go past 24 Gbps

- This has saved Broadcom hundreds of thousands of dollars since they implemented this solution and they consider it a success