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Functional Stress Failures on HVS, Burn-In and ESD/EOS

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Contents

Acronyms

- **HVS/DVS/BVS:** High / Dynamic / Bump Voltage Stress/Screen
- **ESD:** Electro Static Discharge
- **HTOL:** High Temperature Operating Life
- **GIDL:** Gate Induced Drain Leakage
- **DIBL:** Drain Induced Barrier Lowering
- **ET:** Electrical Test; **FT**: Functional Test
- **EFA/PFA:** Electrical / Physical Failure Analysis
- **APU/GPU:** Application / Graphics Processing Unit
- **LT/RT/HT**: Low/Room/High Temperature
- **CUP/SUP:** Circuits/Structures Under Pad

- **EOS:** Electrical Over Stress
- **PPM:** Parts Per Million
- **WST:** Wafer Sort Test
- **FA:** Failure Analysis
- **TSV:** Through Silicon Via
- **ELF:** Early Life Failures
- **DRC:** Design Rule Compliance

Abstract

Different screens are important part of product's flow.

Product and reliability teams observe fails during:

- A new technology in development
- Changes to existing processes
- A new design/product is introduced.

Fail cases presented, one for each type on:

(1) HVS or DVS (2) Burn-in or HTOL (3) ESD/EOS

HVS/DVS: High / Dynamic Voltage Screen
HTOL: High Temperature Operating Life
ESD: Electrostatic Discharge; **EOS:** Electrical Over Stress

Screens Introduction

Several screens used by Reliability & Test teams:

- First Chip probe (CP) or wafer sort test (WST) at Room Temp.
- Done at higher voltage: 1.4 to 2 x Vnom, LT/RT/HT

Purpose: Screen early defects not caught by sort.

- Screens can also be at package level.
- But wafer level saves efforts, time & costs:
  - If higher screen loss – reduces packaging
  - Separates Fab Vs Assembly fails – to focus.

Different Screens & Types

EVS/HVS/OVS: Enhanced / High / Over Voltage Screens:

- Elevated Voltage ➔ DC/Static ➔ milli. secs to few secs.

DVS/BVS: Dynamic / Bump Voltage Screen: with Dynamic patterns

CCS & CVS: Constant Current or Constant Voltage Stress

Other Screens: Pre Vs Post, Parametrics & Shifts:

- **Iddq/Istby:** GIDL, DIBL, IR Drop, Delta Tj
- **Scans**: Vmin-Vmax, Vdip, Vdroop (block/global) shifts
- **At Speed:** Access / RC Delay & Timeout screens
- **Patterns:** Different backgrounds: Wiggle, In/Ex-Test
- **Temp:** Above combinations at different Temperatures.

GIDL: Gate Induced Drain Leakage
DIBL: Drain Induced Barrier Lowering

Different Level's of Screens - 1

- **Level-1: Wafer Level:** ET, Sort, HVS/DVS/BVS/OVS
  - 100's of m. secs to few sec: Static/Dynamic, Dip/droop/Scan delays.
  - To screen general outliers, random and weak defects.
  - For all post Fab Wafers: Consumer, Residential applications.

ET: Electrical Test; **FT:** Functional Test

- **Level-2: Module Level**: FT, Production and shipment Burn-In
  - Several secs to few mins/hours: Dynamic, High voltage & temp.
  - For Value add products: CPU/APU to screen ELF & Maverick lots.
  - For Medium PPM Apps. Ex: Industrial/Automotive Grades etc.,

ELF: Early Life Fails; **PPM:** Parts Per Million

Different Level's of Screens - 2

- **Level-3: Card/Board Level:** Few chips together: 2.5D/3D/TSV's etc.,
  - For very low PPM, High Value add CPU/APU/GPU/Server Chips.
  - Generally several hours to upto a day, High REL: Military Apps.
- **Level-4: System Level Test** (SLT): Whole system test.
  - High Reliability Apps, Few days to weeks: Cloud Systems, Main Frames etc.
  - Mission critical Applications: Medical, Aero, Space.

TSV: Through Silicon Via

Different Screens Comparison

Screen	Test/Pattern	Voltage Level	Temp.	Duration	Wafer/ Package	Function /Purpose
HVS: (EVS or BVS/ OVS)	Generally Static (DC)	1.8x~2x Vnom	LT, RT (or) HT	Milli seconds to several seconds	Wafer Level at sort or Post Bump	To weed out Voltage & Temp. activated weak parts for TDDB, NBTI/PBTI
	Dynamic With Patterns	1.3x~1.7x Vnom				For Voltage, Temp and current activated weak parts for SM/EM/Leakage
DVS	Generally Dynamic	1.4x~1.6x Vnom	RT or HT		Wafer or module level	Quick Screen at sort for consumer products for early random defects.
Production Burn-In (PBI)	Dynamic with Functional	1.4xVnom or 1.2xVmax	Tj: 125C~ 150C	2, 12, 24, 48 hrs	Module Level	Effectively screen the IM/ELFR weak parts. (early portion of HTOL)
PCB/Card Board/SLT	Dynamic with Functional & At Speed	1.4xVnom or 1.2xVmax	RT or HT	Few hours to days	Card/PCB/ System level	Mini PBI / Chip set BI: Check delays between PCB & other chips. X-talk, Scan/Delays, Iddq

RT – Room temp; LT-Low Temp; HT- High Temp

HVS/DVS Screens: Significance

The HVS/DVS screens are very effective tools:

- To identify fail type & modes quickly
- Impacting quality & yield of a process
- New process or design and their interaction.
- Decide if module level / Burn-in are needed.

Screens can also be good tools for

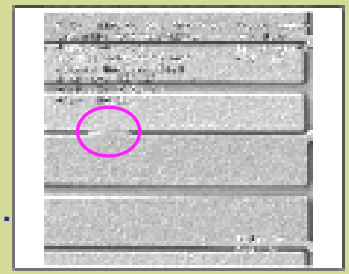
- Line/tool excursions or issues & to isolate them.
- Assess reliability risk on mavericks / random defects
- Decisions to accept & release wafers or to reject.
- To separate process, design Vs assembly & interactions.

HVS/DVS: Case Study - 1

Background: 130nm wafers' yield affected by poly bridging.

FA: Not enough space on Poly silicon lines causing shorts.

Hypothesis: Narrow space at poly lines ➔ higher electric field.



FA on Poly Si Fails

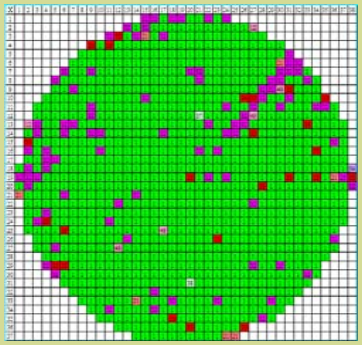
- **DVS** recommended to detect for additional fails.
- **Stress Voltage:** 1.3xVdd. Duration: 150ms.
- **Wafers** with 1% poly bridging fail identified for DVS.
- **WST ➔ DVS (screen stress) ➔ WST**
- To check no DVS impact on chip ➔ good wafer added as control.

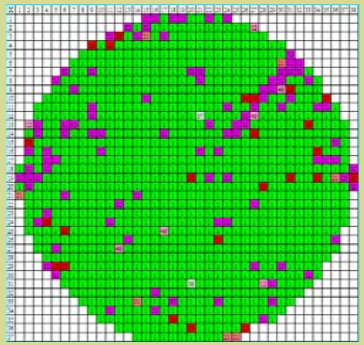
WST: Wafer Sort Test

Pre Vs Post Screen Comparison

Impact Wafer ➔

Good Dies	Count
Bin1's Pre DVS	952
Bin1's Post DVS	943
Pre-Post DVS delta	9



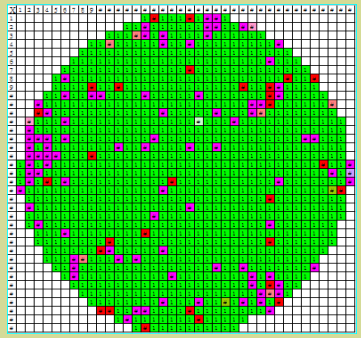


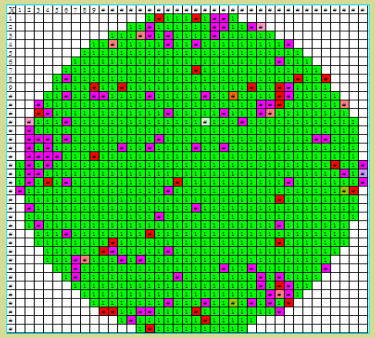
Post WST/Pre DVS

Post DVS

Good Wafer ➔

Good Dies	Count
Bin1's Pre DVS	950
Bin1's Post DVS	951
Pre-Post DVS delta	-1





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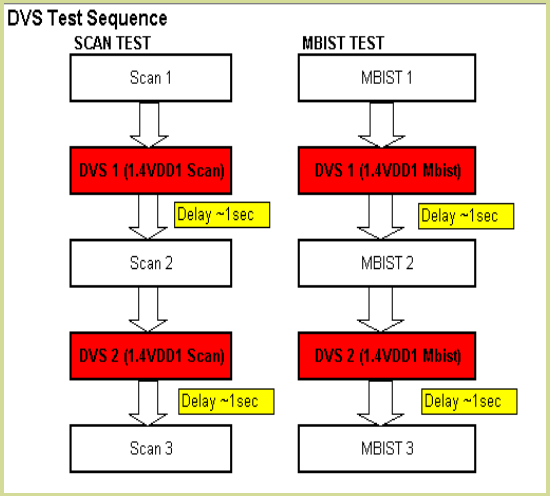
DVS Screen Study-2

Background: Yield loss on MBIST & Scan fails – same customer - another Fab

- Run DVS evaluation to assess reliability risk.
- DVS condition: 1.4xVdd; 1~2secs; Repeat 2x.
- Apply on BIST (memory) & Scan (logic) area.

Screen & Program Setup:

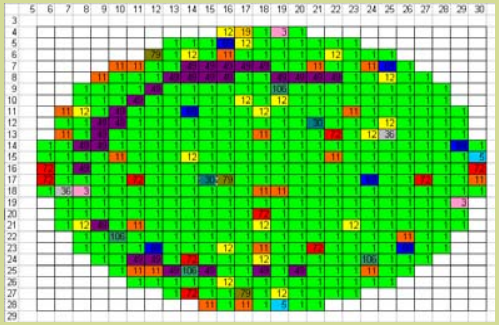
- DVS test program: Single touchdown generated.
- 4 Wafers selected: MBIST: 6~11%, Scan: 8~13%
- A control good wafer added for reference.
- Scan test: 1284msec; MBIST: 375msec for 1x DVS.
- Total Time/one DVS = 1659msec = 1.66sec
- Total Time for 2xDVS = 3318msec = 3.32 sec



DVS Results on Good/Control Wafer #3

Bin	Test Params	First Sort	Sort after DVS	Delta
		Count	Count	Count
1	GOOD	377	387	10
11	FAIL_SCAN	42	43	1
72	FAIL_MBIST1	10	12	2

Before



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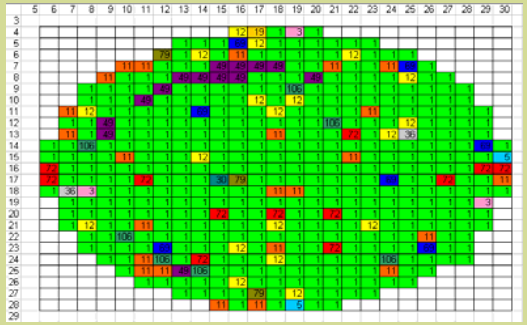
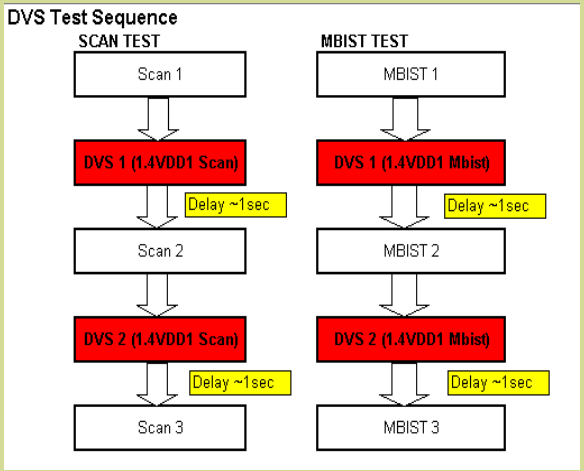


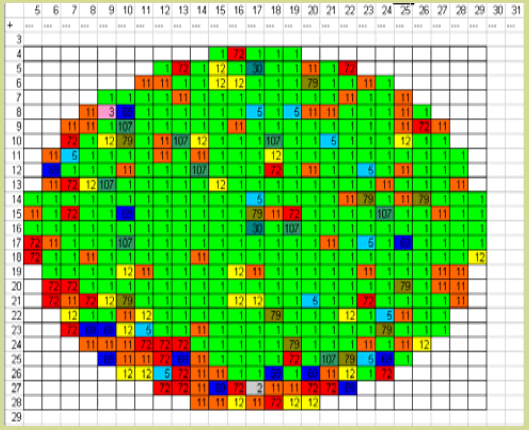


- 1dice Scan variation also seen on control wafer.
- Yield gain is observed.

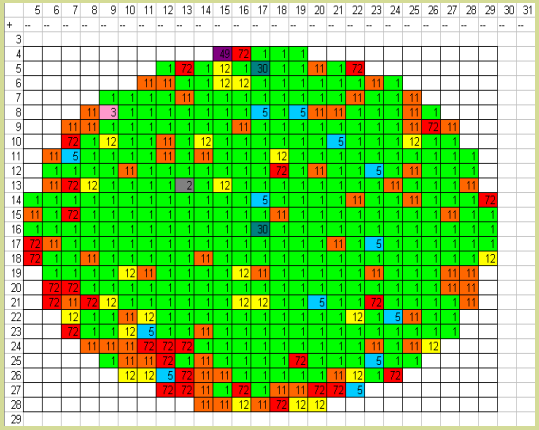
Pre-Post DVS Results: Wafer # 13

Bin	Test Parameters	Wafer # 13		DELTA
		WS1	WS2	WS2 - WS1
1	GOOD	313	344	31
11	FAIL_SCAN	90	90	0
72	FAIL_MBIST1	30	30	0

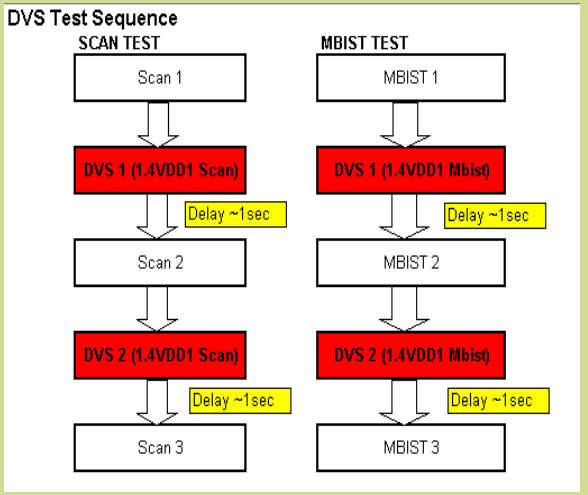
Before



After



DVS Test Program

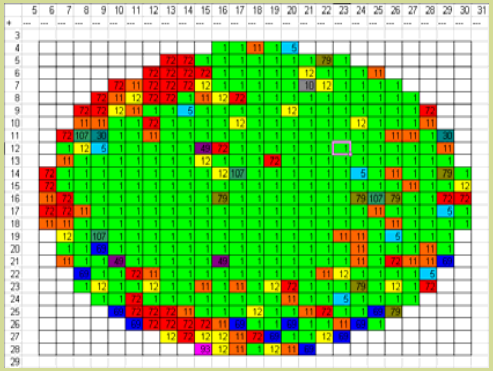


- No additional Scan and MBIST failures observed.
- Yield gain is observed.

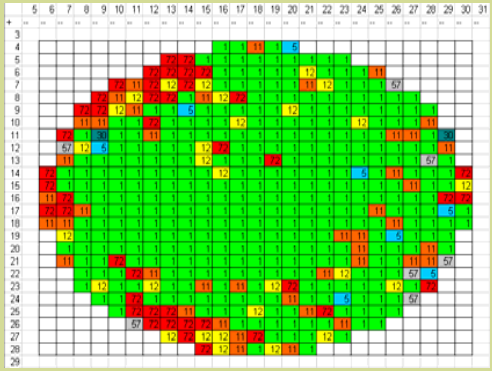
Pre-Post DVS Results: Wafer # 21

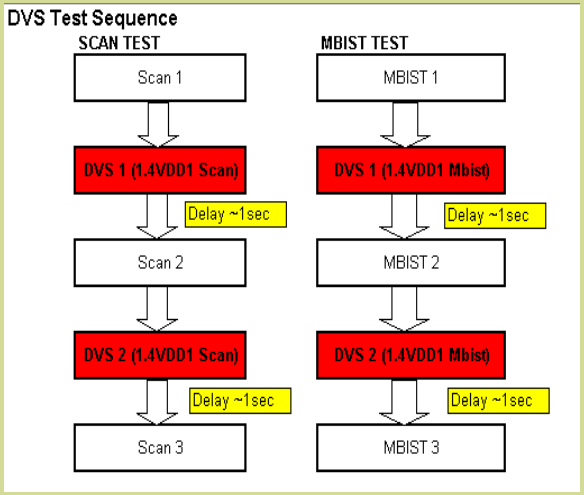
Bin	Test Parameters	Wafer # 21		DELTA
		WS1	WS2	WS2 - WS1
1	GOOD	333	351	18
11	FAIL_SCAN	69	70	1
72	FAIL_MBIST1	43	43	0

Before



After



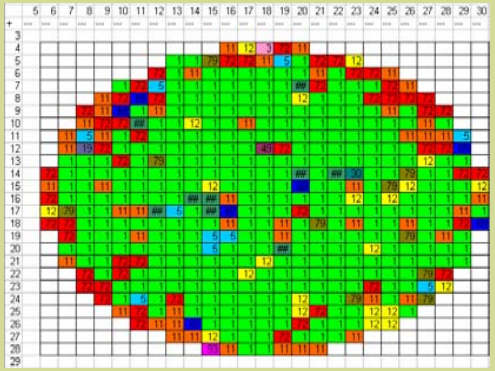


- **No additional "MBIST" fails.**
- **One "Scan" fail => Due to longer scan stress time of 2x1.284 sec.**
- **Yield gain is observed.**

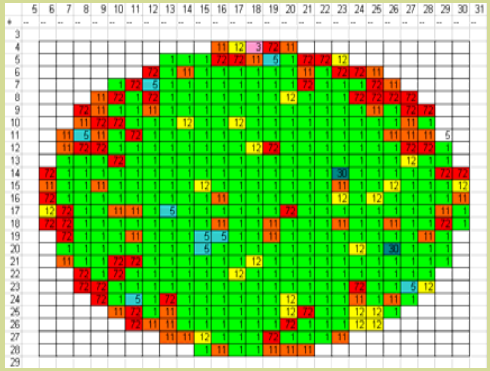
Pre-Post DVS Results on Wafer # 4

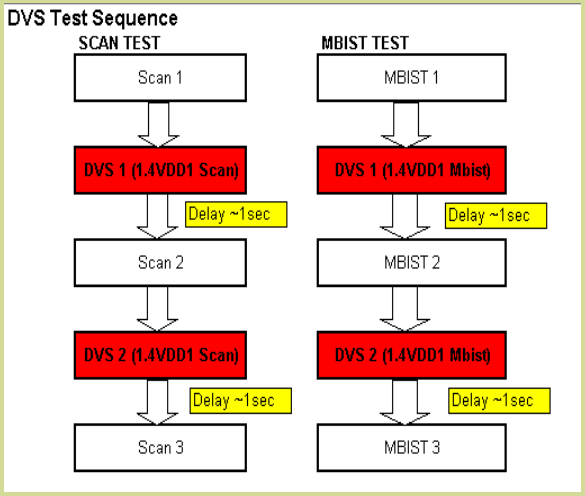
Bin	Test Parameters	Wafer # 4		DELTA
		WS1	WS2	WS2 - WS1
1	GOOD	318	344	26
11	FAIL_SCAN	71	72	1
72	FAIL_MBIST1	53	53	0

Before



After



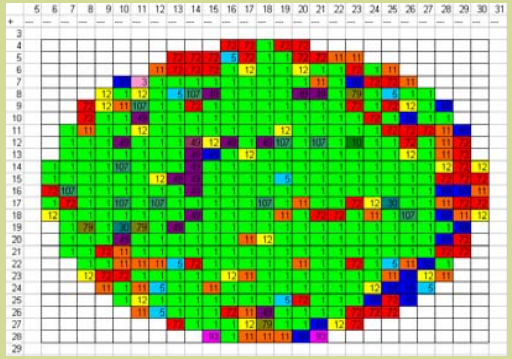


- **No additional "MBIST" failures.**
- **One "Scan" fail => Due to longer stressing Scan time of 2x1.284sec.**
- **Yield gain is observed.**

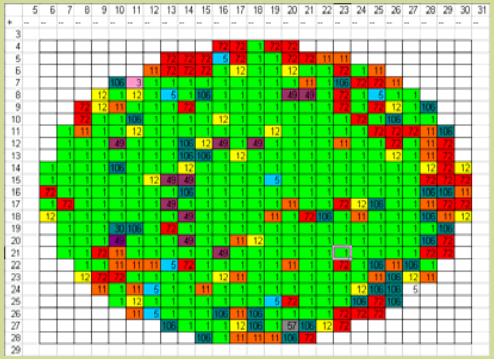
Pre-Post DVS Results on Wafer # 18

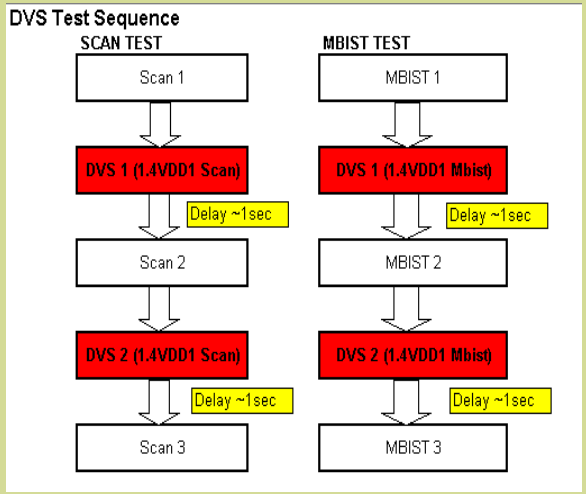
Bin	Test Parameters	Wafer # 18		DELTA
		WS1	WS2	WS2 - WS1
1	GOOD	301	306	5
11	FAIL_SCAN	60	61	1
72	FAIL_MBIST1	55	55	0

Before



After





- **No additional "MBIST" failures.**
- **One "Scan" fail => Due to longer stressing time of 2x1.284sec.**
- **Yield gain is observed.**

Screen Results & Conclusion

Screen Results Summary:

- Overall yield gain on all 4 wafers after DVS.
- No additional MBIST failures observed on all 4 wafers.
- One Scan fail each on 3 wafers. Due to long stress time of 3318msec.
- 1 or 2 dice variation is observed also on control wafer for Scan test.

Conclusion: DVS results show risk of wafers affected by Si bridge is Low.

Screens Summary: Issues/Devices/Nodes

Node	Issue	DVS Used	DVS & HTOL Flow, Criteria & Results	PPM Criteria (Vs Baseline)	Test results & PPM
0.18um	Poly Edge defect	1.4xVdd, 1.8 sec Done on SRAM	Affected wafer, good dies=1014 -> 0 fails Ref. good wafer, good dies: 1404 -> 0 fails	<1000 PPM (baseline)	904 PPM
0.18um	Poly Edge lift	1.4xVdd, 3.8 sec done on product	6 steps studied, 1.3sec enough to screen. Total good dies:4757, 5 fails detected	<1500 PPM (baseline)	1323 PPM
0.18um	M1 random defect	1.4xVdd, 3.68 sec done on SRAM	G1- yield >90%, good dies: 1636 - 0 fails Gp-2- wfr <90% good dies:1012 - 2 fails	<1500 PPM (baseline)	>90% - 560 PPM <90% - 3068 PPM
0.18um	Si defect & leakage	1.4xVdd, 200msec	1 fail found on affected lot: 1/785	0 fails	2667 PPM
0.11um	Via-5 deformation due to BARC material	1.4xVdd, 300m.sec	1 fail on Old TM BARC containment lots & 0 fails on New TM BARC lots.	0 Fails	0 Fails on 168hrs HTOL after DVS.
0.11um	Broken Poly	1.4xVdd, 1638msec	Good lot Wafer - 0 fails Bad lot Wafer - 2 fails	<= 1200 PPM (Baseline)	<1000 PPM
0.13um	CoSi Residue: BIST & SCAN fails	1.4xVdd, 300m.sec Good wfr#3 - 0 fails	Wfr#1: 4 good dies fail (not BIST/SCAN) Wfr#2: 3 good dies fail (not BIST/SCAN)	<1500 PPM (baseline)	0 Fails on 168hrs HTOL after DVS.
0.13um	Product Scan 502/506	1.4xVdd, 300m.sec HTOL T168 -> 0 fails	1~4% yield loss wafers -> 1 Fail 5% loss -> 2 fails -> HTOL 168hrs -> 0 fail	<= 2000 PPM	1000 PPM (2 fails)
65nm	Patch fails at Notch and MBIST Fails	1.65xVnom, 30x loops to 8sec good lot wfr-0 fail	Bad wfr-0 fails at good & 4 fails near notch Another lot: 2 fails at good region	Ink off at affected region	<1000 PPM
65nm	PC-CA short		Good lot Wafer - 0 fails Bad lot Wafer - 2 fails	0 fails at 168hrs after screen.	<1000 PPM
40nm	High Iddq due to SUP/CUP design	1.8xVnom 10x Loop test total 12 sec	Good lot Wafer - 0 fails Bad lot Wafer - 2 fails	0 fails at 168hrs after screen.	<1000 PPM
14nm (OD)	TS-PC, Mx-Jx defects SCAN & BIST fails	1.7-1.8V HVS:2-4sec 1.44-1.6V DVS: 2-4sec	LScan & MBIST are 50-50 fails after screen T168hrs HTOL-0 fails	<500 PPM (Baseline)	<305 PPM

Burn-In/HTOL Fails: Case Study - 3

Background: 40nm HTOL fails on customer's test chip at 1000hrs.

History: 45nm used same test chip & passed 1500hrs HTOL.

Observations: Fails are of high Iddq/leakage – T500 pass.

- Chip has CUP/SUP & Over Drive (OD) by 20%.

Layout Checks: Customer used stringent CUP/SUP design.

EFA: Fails show hot spot below fail pad.

CUP/SUP: Circuits/Structures Under Pad
EFA: Electrical Failure Analysis

Hypothesis: Stringent CUP/SUP design with shrink & OD causing local heating leading to fails under the Pad.

HTOL Fails & FA Findings

Problem: HTOL fails on Customer Test Chip.

- At 500hrs all chips pass – high leakage & Iddq at 1000hrs.
- Chip has CUP/SUP design below pads.
- Using Over Drive stress: 20% more

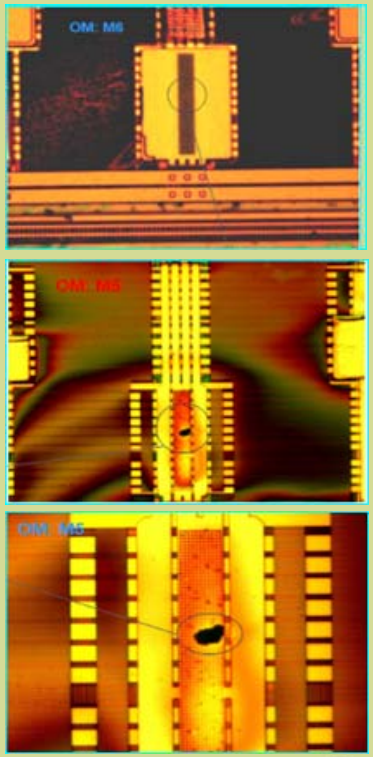
FA: Burn-out damage below pad, similar to short

Layout Checks: Improper CUP/SUP design below Pad.

- Keep-out zone DRC violation ➔ causing local heating in HTOL.
- Leading to short between Vdd & Vss lines under pad.

CA/PA: Customer agreed to use new CUP DRCs for products.

DRC: Design Rule Compliance



ESD/EOS Fails: Case Study-4

Background: Yield loss at sort on products in two tech. nodes.

- Checks on lot's process history didn't show any abnormalities.

Observations: Both nodes have **BEOL dummy fill** – only commonality.

Hypothesis: Static charge gets accumulated in BEOL dummy fills.

- Process steps: Deposition, Polishing, Cleaning, etc.,

- When wafers are tested, accumulated static charge gets discharged.

- Causing damage to active devices underneath, leading to yield loss.

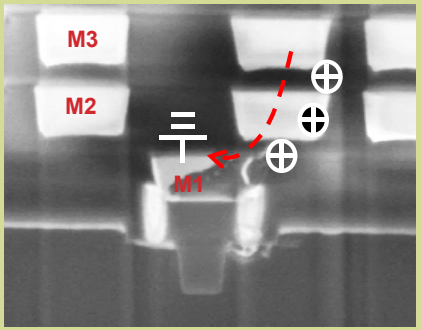
EOS Case-1: Investigations & Findings

Background: Customer reported normalized yield loss of 10% at sort

- Product is from Planar Bulk Process.
- Before and after lots are not impacted.
- Only particular lots have seen impact on sort.

Findings: Clear ESD/EOS like “Discharge” signature.

- Causing damage at the active / gate area.
- Showing EOS like discharge caused failures at sort.



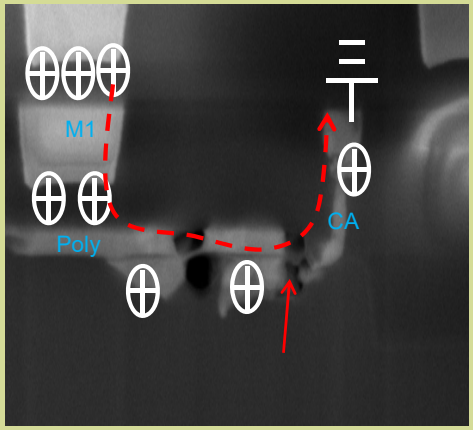
EOS Case-2: Investigations & Findings

Background: Normalized yield loss at sort: 8-15%.

- Product is from planar bulk process.
- No HVS/DVS ➔ standard sort at Vnom & Vmax only.
- Above should not cause this level of yield loss.
- @20K wafers sorted & shipped before for @2yrs.

FA & Findings: Observed clear ESD/EOS like damage.

- Damage found at the Poly/Gate area.
- EOS like damage caused the failures.



Schematics & Design Solution

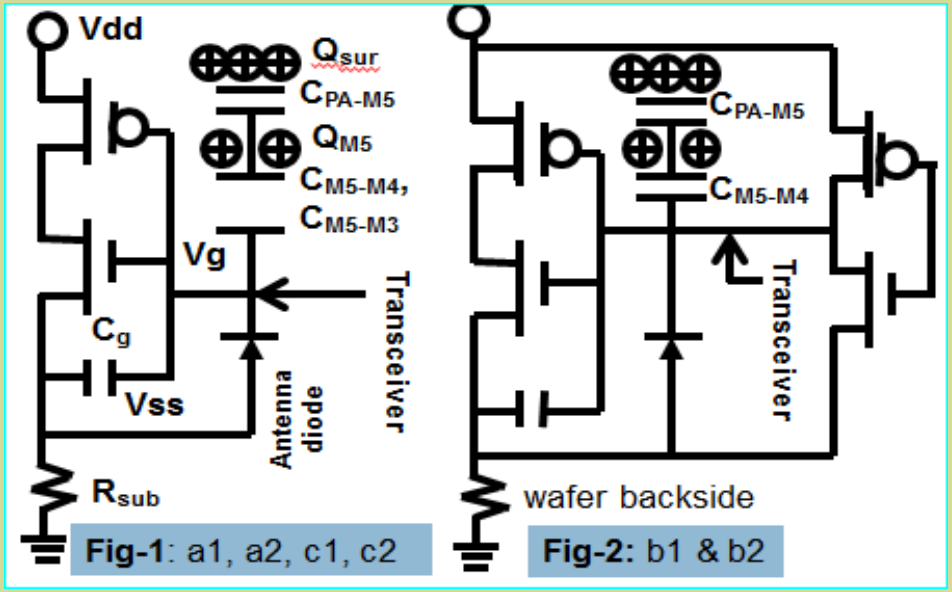


Fig-1: a1, a2, c1, c2 **Fig-2:** b1 & b2

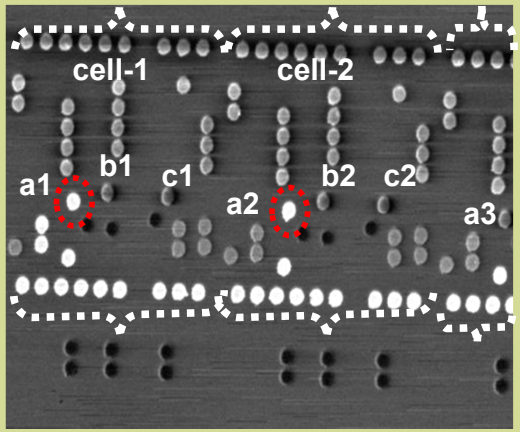


Fig-3: FA Locations

- **Fig-1:** Transistors a1 & a2 will higher Vg ➔ Small antenna diode can't prevent this.
  - Bright spots seen only at gates a1 and a2.
- **Fig-2:** Hot spots not seen at gates a3, b1, b2, c1 & c2 ➔ An inverter drain can prevent this.

Design Solution to Discharge Issue

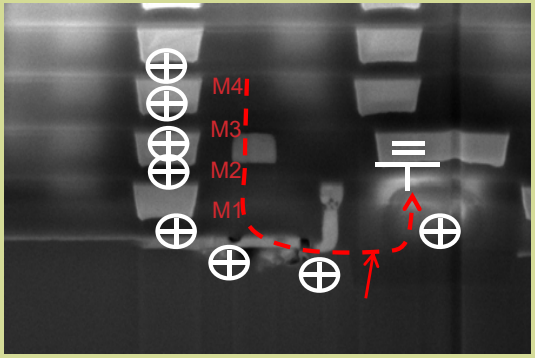
- Standard built in Antenna Diode can't prevent the damage.
- Charge built up on Dummy Fill in several metals
- Charge is too high to be stopped by small antenna diode.
- Design solution modified to include an "Inverter Drain".
- The new design solution is able to prevent the damage.

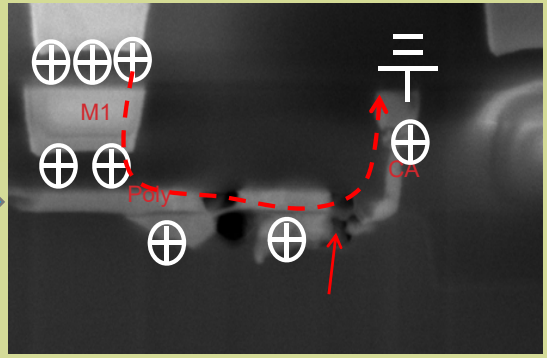
Problem Characteristics – For Process Solution

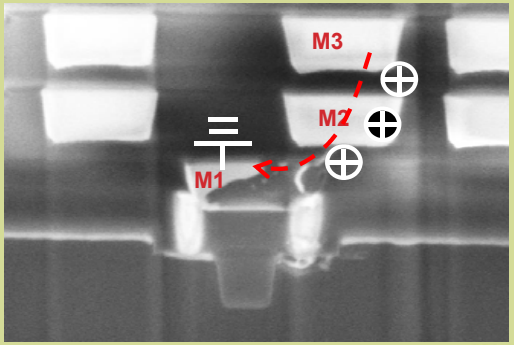
- Static charge accumulation on dummy fill patterns:
  - During CMP, deposition or scrubber clean steps.

CMP: Chemical Mechanical Polishing

- Damage always at regions below dummy metals:
- Highly desirable to prevent built up of charges;
  - During the process - Quality & Reliability perspective.







Process Solution for ESD/EOS Issue

Method of removing charge from dummy fill, instantaneously:

- To maintain wafer at “charge neutral condition” at all process steps.

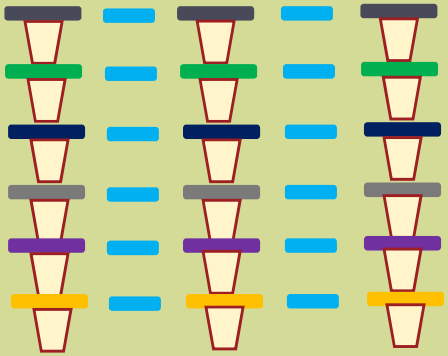
The above can be achieved by:

- Connecting dummy fill to ground bus, at each layer as processed.
- As ground bus is connected through substrate to a grounded Chuck.
- Charge will be continuously removed at all process steps.

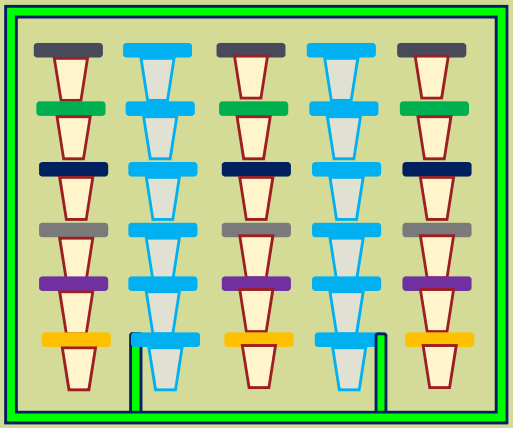
- Solution applicable to any wafer process for any tech. node.
  - Also for post fab processing steps: Bumping, sort & Assembly.
  - As wafer/die backside will be grounded to Frame/substrate.

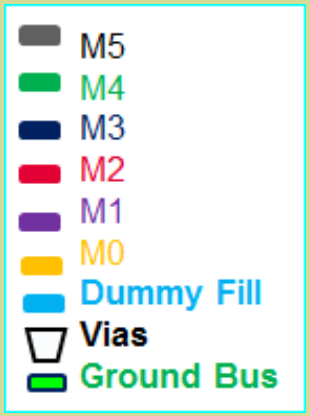
Proposed Process Solution

Conventional Method:
Floating Dummy Fill



Solution: Dummy Fill
Connected to Ground Bus





Conclusion

- Screens are very important tools at all levels.
  - Wafer/module, Card/PCB or System Level.
- Fail types & modes to be characterized
- To find root cause & fix: Corrective/Preventive Actions
- Fixes on design, process & assembly – mandatory.
  - Else reliability quals. will not pass to proceed.
- Fails not fixed, appear later & more difficult to fix.