
TWENTIETH ANNUAL
TestConX™
March 3 - 6, 2019
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive

COPYRIGHT NOTICE

www.testconx.org

Bridging the Gap Between SLT and ATE

Yi Zhang
Teradyne Corp

TestConX™

2000 - 2019 20 YEARS ANNIVERSARY

TERADYNE

Mesa, Arizona ● March 3 - 6, 2019

Use of SLT Is Getting More Attention

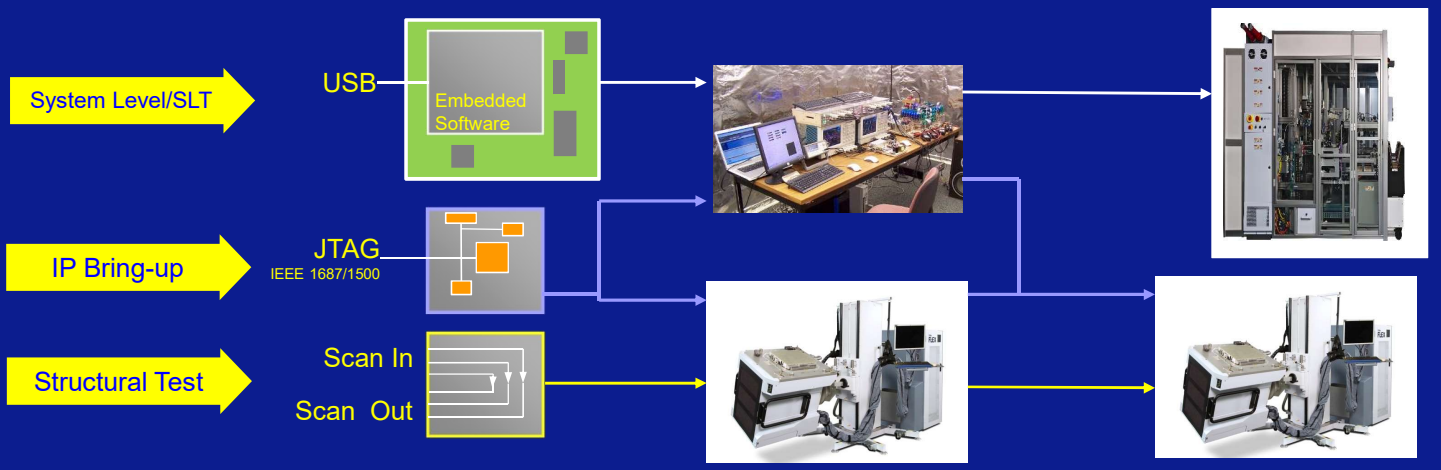
- More complex devices
- High Quality Standards
- …everything else you've heard today
- Teradyne makes both ATE and SLT systems
- But SLT does not exist in a vacuum

Titan SLT System

UltraFLEX ATE

Typical Device Bring Up Cycle

- Several Parallel Paths
  - Functional bring-up/debug in the lab and eventual SLT test insertion
  - Silicon IP Debug
  - ATE development of structural and parametric tests
- But: New Tools are bringing more functional test capability to ATE



TestConX™

Bridging the Gap Between SLT and ATE

3

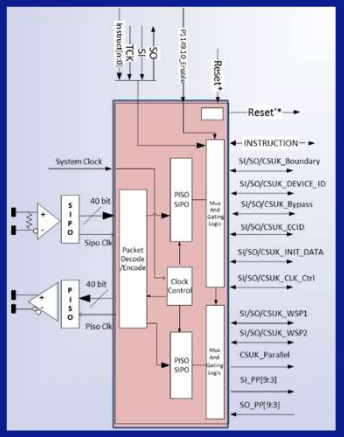
Titan SLT - Tester Information

- Supports up to 320 sites per system
- Supports PoP, PGA, BGA, LGA, etc.
- Test sites are fully asynchronous (load and test)
- DUT Interfaces Per Site:
  - 1Gbps Ethernet port per test computer
  - 10 Gbps high speed port per DUT
  - 1 Serial port per DUT
  - 1 JTAG enabled port to each DUT
  - 1 SPI interface to each Test Board
  - Voltage: 3.4-10V
  - Power control/measurement
- System can be serviced while running for ~100% OEE

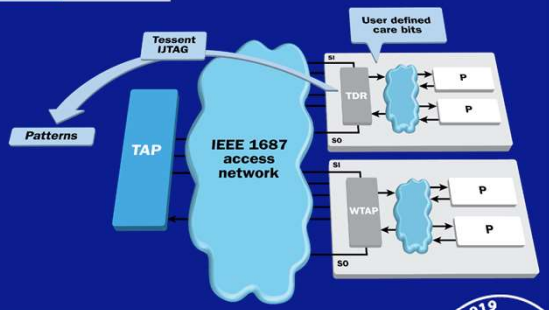
TestConX™

Interesting Trends in Standards

- IEEE 1149.10
  - Scan test over high speed Interface (like USB)
- IEEE1687/1500
  - Allows IP vendors to offer standardized access to Silicon IP for test
- Accellera "Portable Stimulus Group" (IEEE 1800.2-2017)
  - system-level design, modeling, and verification standards

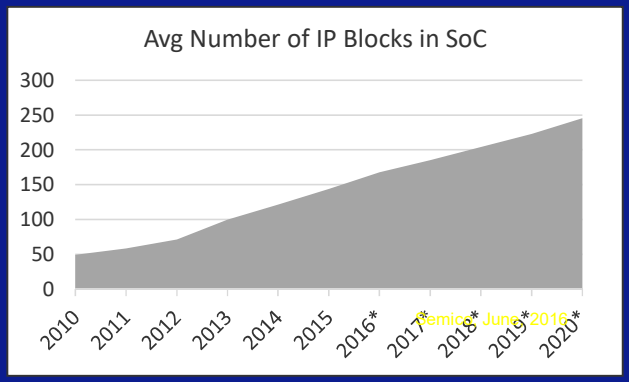


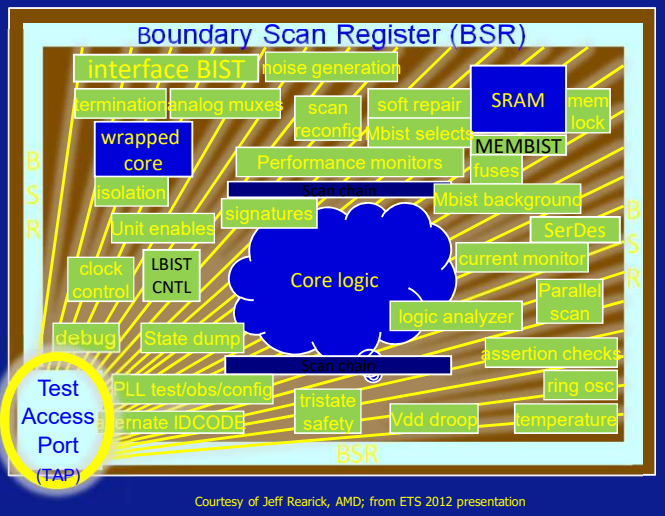
Source: IEEE High Speed JTAG P1149.10 Working Group



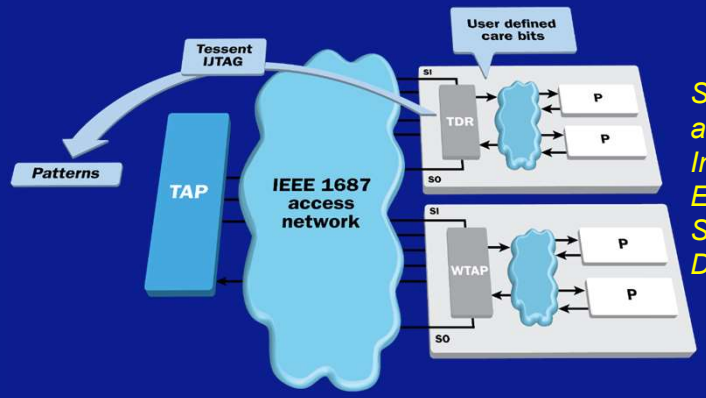
New Standards Can Help

- IEEE 1687 (IJTAG)
  - Standardized way to talk to device cores





Courtesy of Jeff Rearick, AMD; from ETS 2012 presentation

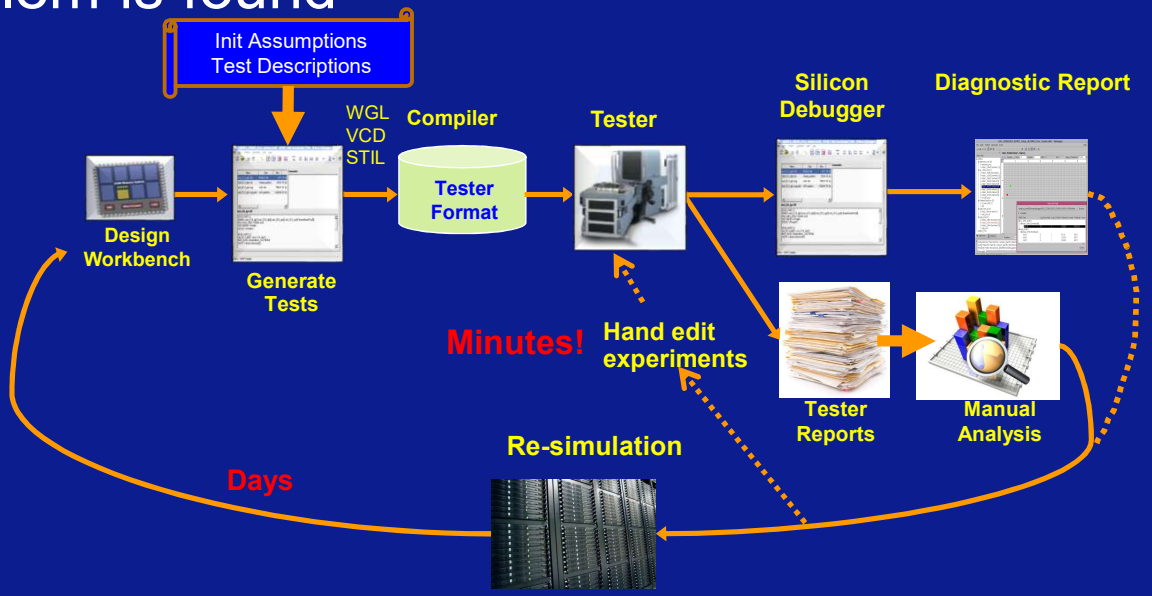


Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device


Challenge: Handling IP Diversity
こんにちは
Guten Tag
Hello
Hola
안녕하세요
Ciao
Bonjour
你好
Hello
Hello
Hello
안녕하세요
Hola
Hello
Ciao
Hello
Hello
Guten Tag
Bonjour
Hello
Hello
你好
IJTAG
(IEEE 1687)
Test Tools
Test Tools
Standardized communication interfaces enable faster integration, test and debug
M. Knowles, M. Hutner, ATE-Connect, ASM Webinar
TestConX™
Bridging the Gap Between SLT and ATE
7
2000 - 2019
20 YEARS
ANNIVERSARY

The Long Road Between Design and Test

- The device bring-up process can have long delays if a problem is found



Teradyne/Mentor Announcement at International Test Conference

- Mentor introduces ATE-Connect™ test technology with Teradyne, dramatically speeding silicon debug and bring-up

Mentor
A Siemens Business

Press

Wilsonville, OR, October 24, 2018

Mentor introduces ATE-Connect test technology with Teradyne, dramatically speeding silicon debug and bring-up

- **Industry-first ATE-Connect technology in Tessent SiliconInsight introduces direct communication between Tessent DFT software and Teradyne testers, accelerating silicon bring-up from weeks to days**
- **Teradyne's UltraFLEX ATE fully supports the interface to Tessent SiliconInsight with ATE-Connect technology**

Mentor, a Siemens business, today announced the availability of the ATE-Connect™ technology in its Tessent® SiliconInsight® product for IC debug and bring up. The ATE-Connect technology creates an industry-standard interface to eliminate communication barriers between proprietary, tester-specific software and design-for-test (DFT) platforms. The new technology accelerates debug of IJTAG devices, helps speed up product ramps, and reduces time-to-market for products in 5G wireless communications, autonomous driving, and artificial intelligence. Mentor has also announced that Teradyne's UltraFLEX test solution fully supports the new Mentor interface through its Portbridge technology.

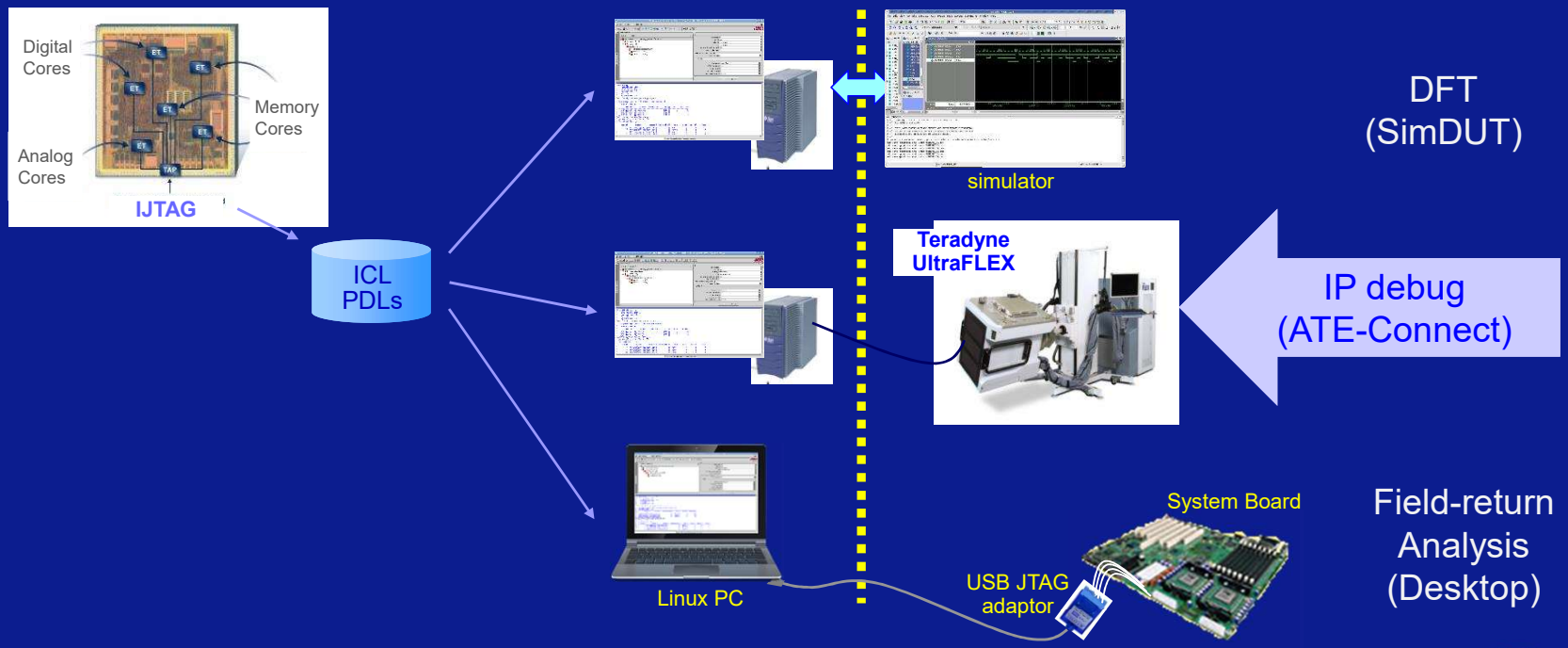
Despite broad industry adoption of the IJTAG (IEEE 1687) test architecture for chip-level testing, many companies maintain very different approaches for converting chip-level test patterns into tester formats, as well as for debugging tests on automatic test equipment (ATE). Consequently each specific chip must have test patterns written by DFT engineers and then translated by test engineers to debug each scenario on each tester type. Test engineers typically work at a low, detailed level with clock cycles, while DFT engineers work at a higher level using IJTAG. The differences in tools and techniques between the two can lead to confusion on how to most efficiently debug chips, resulting in long delays in the IC product lifecycle.

Using the TCP/IP network protocol, the Mentor ATE-Connect technology provides IJTAG commands to the device under test and receives data from the device on the ATE – all while keeping the sensitive design information in the realm of Tessent SiliconInsight and only providing the required stimulus to the device under test on the ATE. With this standard network communication, customers can leverage their existing secure networks to enable seamless interaction with testers around the globe.

8005 S.W. Boeckman Road · Wilsonville, OR 97070-7777 · 503-685-7000 · www.mentor.com

TestConX™

Tessent SiliconInsight: Consistent Debug Environment



SiliconInsightSetupSpecification

TestConX 2019

The Difficult Way to debug a functional or BIST test

- Auto-Generated Patterns

TSet	Command	Label	Vector/Cycle	(EECS,EEDI,EESK,SPISCK,SPICSB,LED3,LED2,LED1,LED0) (DSSC-Capture)	RSET	LANWAKEB	PERSTB	EEDO	ISOLAT TTC ECLT BSKD	CKTAL1	CKTAL2	SPISO	EECS	EEDI	EESK	SPICSB	SPISCK	LED3	LED2	LED1	LED0
GphyAdc1			0		X	X	0	0	1000	X	X	11	H	L	H	L	L	H	L	L	H
GphyAdc1			1		X	X	0	0	1000	X	X	11	H	L	L	L	L	H	X	X	X
GphyAdc1			2		X	X	0	0	1000	X	X	11	X	X	X	L	H	L	H	L	L
GphyAdc1			3		X	X	0	0	1000	X	X	11	H	L	H	L	L	H	L	L	H
GphyAdc1			4		X	X	0	0	1000	X	X	11	L	L	L	L	H	L	H	L	H
GphyAdc1			5		X	X	0	0	1000	X	X	11	H	L	L	H	L	L	L	L	L
GphyAdc1			6		X	X	0	0	1000	X	X	11	H	L	L	L	L	H	L	L	H
GphyAdc1			7		X	X	0	0	1000	X	X	11	L	H	L	H	L	L	L	L	H
GphyAdc1			8		X	X	0	0	1000	X	X	11	L	H	L	L	X	X	X	X	X
GphyAdc1			9		X	X	0	0	1000	X	X	11	X	X	X	L	H	L	H	L	L
GphyAdc1			10		X	X	0	0	1000	X	X	11	H	L	H	L	L	H	L	L	H
GphyAdc1			11		X	X	0	0	1000	X	X	11	L	L	L	L	H	L	H	L	H
GphyAdc1			12		X	X	0	0	1000	X	X	11	L	L	L	L	L	L	H	L	H

TestConX™

Bridging the Gap Between SLT and ATE

11

2000-2019 20 YEARS ANNIVERSARY

The Easy Way

Parallel ports

Register control

Enumerated values

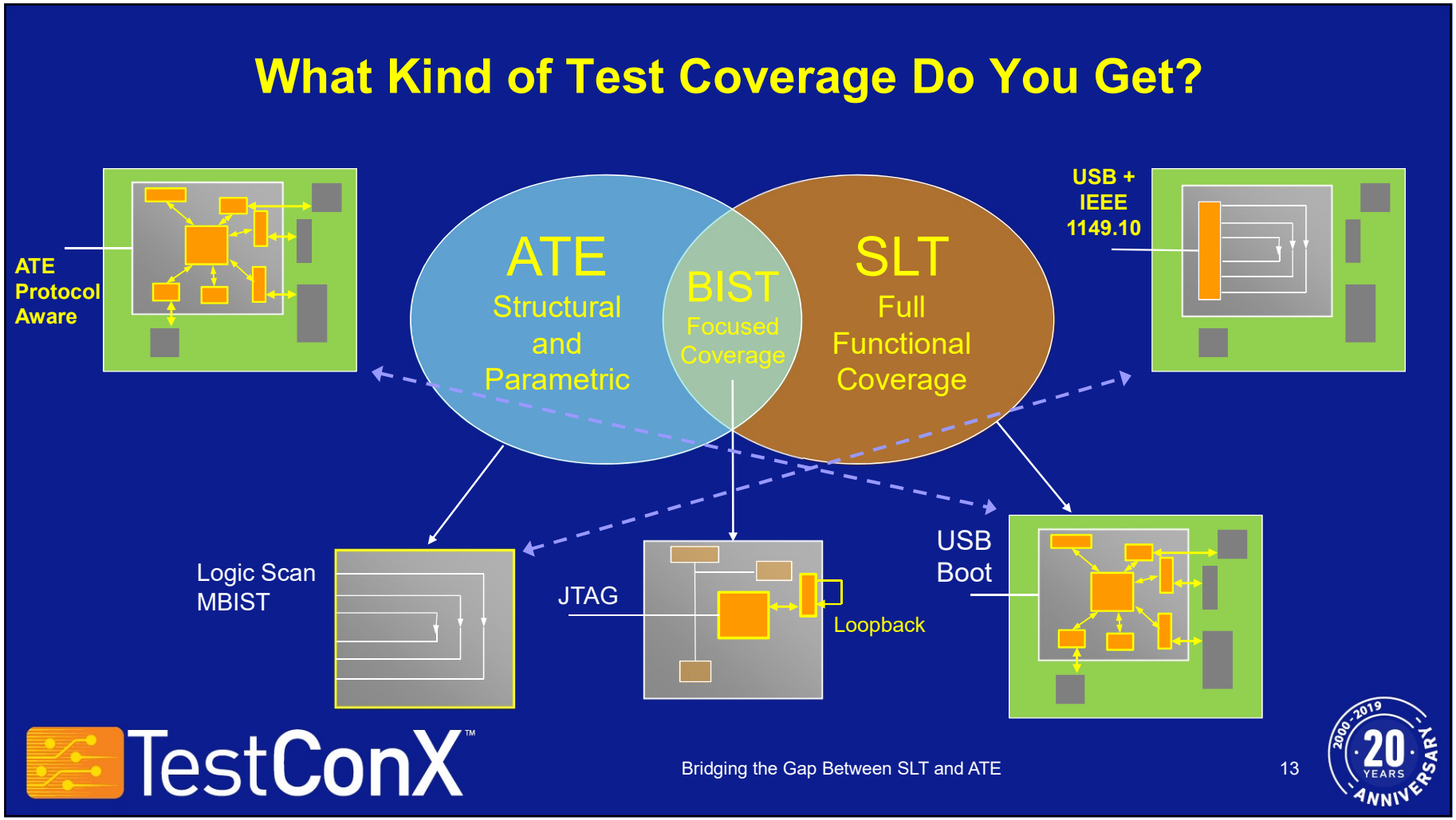
```
Module adc_ltc2308 {

  TCKPort clk;
  DataInPort  measure_ch[2:0]        { Attribute connection_rule_option =
"allowed_tied"; }
  DataInPort  measure_start          { RefEnum init_conv; }
  DataOutPort measure_done           { RefEnum conv_status; }
  DataOutPort measure_dataread[11:0] { Source dataread[11:0]; }

  DataRegister dataread[11:0] {
    ResetValue 12'b0;
  }

  Enum init_conv {
    Convert = 1'b1;
    Idle    = 1'b0;
  }
  Enum conv_status {
    Sampling = 1'b0;
    Done     = 1'b1;
  }
}
```

Read routine

Wait time + de-assert measurement start

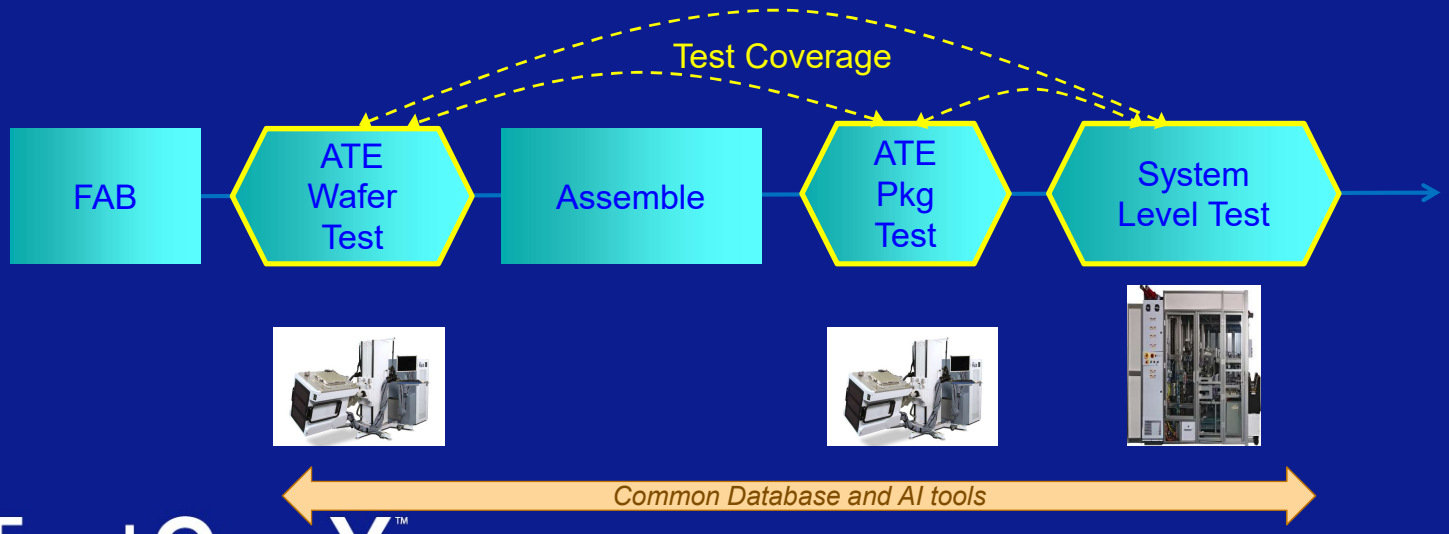
Measurement shift-out

```
# The read_adc procedure requires a channel # (from 0 to 7).
#   The ADC then converts voltage on this channel to a 12-bit unsigned
binary value.
#   This value is then compared against an all-zero value.

iProc read_adc { ch wait } {
    iNote "Starting measurements on channel $ch"
    iWrite measure_ch $ch
    iWrite measure_start Convert
    iApply

    iNote "Waiting for $wait TCK cycles before moving on..."
    iRunLoop $wait -tck
iWrite measure_start Idle
    iApply

    iNote "Checking that measure_done = 1 and extracting results"
    iRead measure_done Done
    iRead measure_dataread 0b000000000000
    iApply
    iNote "Done."
}
```


What Kind of Test Coverage Do You Get?
ATE
Protocol
Aware
ATE
Structural
and
Parametric
BIST
Focused
Coverage
SLT
Full
Functional
Coverage
USB +
IEEE
1149.10
Logic Scan
MBIST
JTAG
Loopback
USB
Boot
TestConX™
Bridging the Gap Between SLT and ATE
13
2000 - 2019
20
YEARS
ANNIVERSARY

What Does This Let Us Do?

- Balance Test Coverage Between Test Insertions for the best mix of cost, quality and yield
- Use Common Data Analysis and AI tools across the entire flow



TestConX™

Bridging the Gap Between SLT and ATE

14

SLT is Great…a Lot of The Time

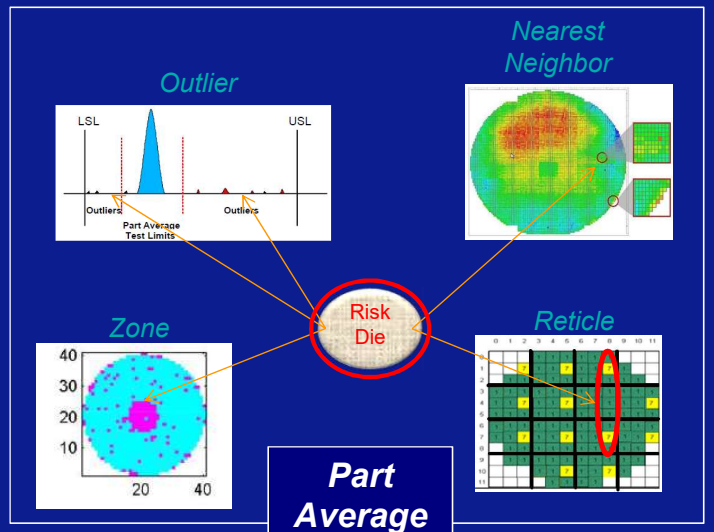
- When is SLT not the best option?
  - Not cost-efficient because of test time or device volume
  - Not cost-efficient because a device has higher allowable defect rates
  - Lower Complexity or narrow range of functionality (ASIC) can be covered on ATE
  - Readily available probing and handling equipment for high- and low-temperature testing
- What is done instead?
  - Find ways to screen for observed system-level problems
    - Example: Mediatek ITC paper about stress-testing during scan
  - Do some sort of BIST or functional test on ATE
    - Just needs to be time-efficient
    - Multisite to lower costs

Emerging Markets

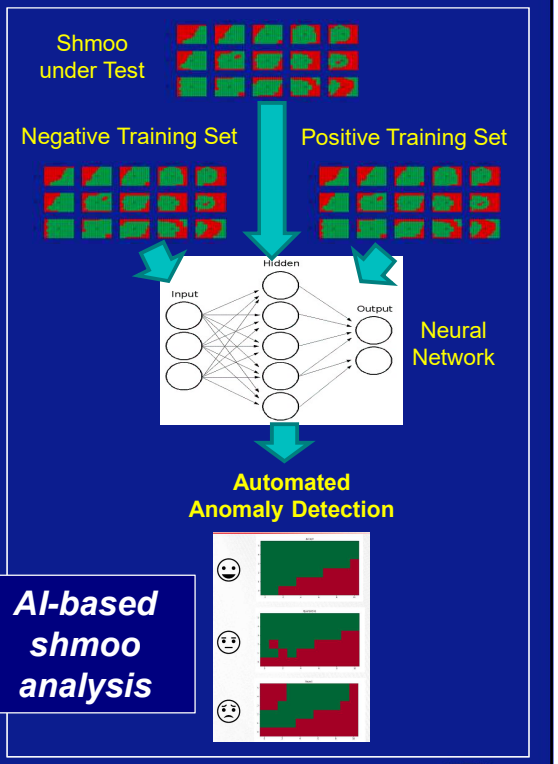
- AI
  - There are two pieces to AI: Infrastructure and Edge
    - Infrastructure will always use SLT for the usual reasons
  - What About Edge devices?
    - Now it's about volume, cost and reliability
    - More like applications processors we do today that have a wide range of test strategies
- ADAS
  - Automotive IC manufacturers seem to know how to make complex devices without using SLT
  - What about Level 3 / 4 ADAS?
  - What about the higher volume devices (e.g. MCUs)?

Opportunity Today: AI In the Test Flow

- Lots of tools to use the data collected in Test
  - Test List Optimization
  - Offline Parametric and Shmoo Analysis
  - Part Average Test
  - Test Cell Heath
  - Traceability tools



Part Average Testing



AI-based shmoo analysis

TestConX™

Bridging the Gap Between SLT and ATE

2000 - 2019 20 YEARS ANNIVERSARY

Can We Build a Bridge?

- Unify ATE and functional/SLT programming environments for more efficient test deployment, code portability, better failure analysis
- Balance test coverage over time on the most efficient equipment?
  - Let economics make the decision
- Apply AI techniques to optimize it all?
  - Outlier detection, etc.