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Holistic approach to test coverage across Final Test, Burn In, and System Level Test

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Agenda

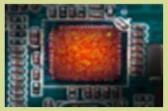
- Overall Test Flow at package level
- Test Content / Objectives Perspective
  - Burn in / SLT / ATE test objectives, coverage
  - Holistic approach / tradeoffs / discussion of insertion mergers
- Handler / Test Equipment and test time considerations
  - Burn in / SLT / ATE Tradeoffs
  - Holistic approach / equipment re-use and debug convergence

Test Flow: Traditional


Wafer Sort T1


Dice and Assembly


Final Test T2


Burn-in (Optional)


Final Test T3


System Level Test (Optional)

Multi-temperature Structural/Functional ATE tests - Screen structural defects and parametric deviations

Screen Early Life Failures

Screen mission mode failures and HW/SW interaction failures

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Goals for Post-Assembly tests: Traditional

Final Test on ATE

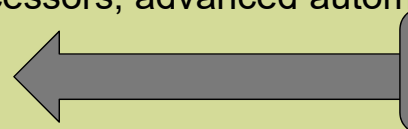
- Assembly, structural and functional defect screening
- Absolutely Necessary across all devices– Minimize test time and temperature insertions
- Performance binning / parametric screening

Burn In

- Necessary only for subset of devices (Automotive, military, new technology etc)
- Attempt to reduce/eliminate burn in if possible
- Goal is to stress devices and screen for infant mortality

SLT

- Necessary only for subset of devices (High end processors, advanced automotive, servers, etc)
- Attempt to reduce/eliminate SLT if possible
- Goal is to eliminate mission mode defects not captured by ATE/Burn in insertions



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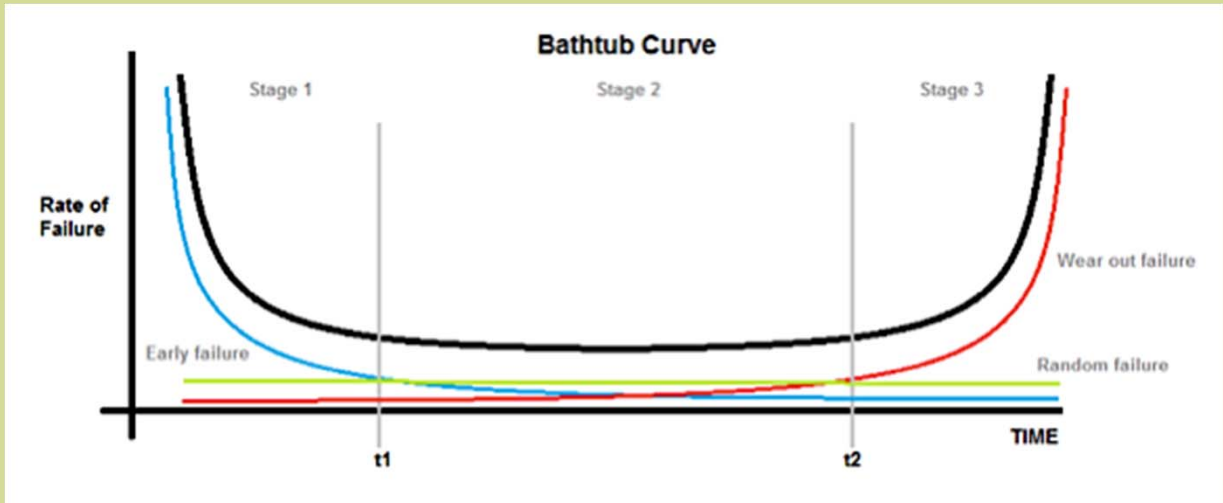
Burn In Goals & the Bath Tub Curve

Burn in Goal:

Accelerate defects and move from stage 1 to stage 2 by stressing device via extreme conditions (voltage / temperature/frequency)



Source : EDN

System-Level Test: Reduces outgoing DPPM and Screens Mission Mode Faults

6B untested at 5 nm!

Technology Node	Transistor Count / SOC (billions)	Transistors missing coverage with 99.5% static ATPG (millions)	Transistors missing speed coverage with 85% at speed ATPG (millions)
22 nm	2.5	12.5	375
14 nm	5.0	25.0	750
10 nm	10.0	50.0	1,500
7 nm	20.0	100.0	3,000
5 nm	40.0	200.0	6,000

Dramatic higher number of untested transistors @ lower technology nodes

Technology Node (nm)	Vdd (V)	100 mV Guardband as a % of Vdd	CMOS Threshold (V)	Headroom Vdd- Threshold (V)	100mV Guardband as % of headroom
90	1.4	7.1%	0.5	0.9	11.1%
65	1.2	8.3%	0.5	0.7	14.3%
45	1.1	9.1%	0.5	0.6	16.7%
28	**1**	**10.0%**	**0.5**	**0.5**	**20.0%**
20	0.9	11.1%	0.45	0.45	22.2%
14	**0.8**	**12.5%**	**0.4**	**0.4**	**25.0%**
10	**0.7**	**14.3%**	**0.4**	**0.3**	**33.3%**

Guardband Stack kills yield at lower nodes

Mobile Consumer DUT Scenario

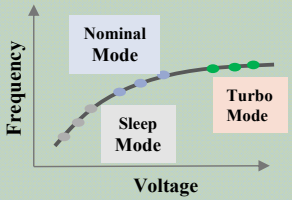
- A video game is playing
- An app is downloading
- Skype is running in the background
- Timer is running

Then - an incoming phone call arrives…

ATE Vector for scenario : Months

SLT Test for scenario : Minutes

SLT enables test coverage for real world scenarios



Source: Mentor

ATE: Insufficient time to run patterns at all corners

SLT: Boots and runs DUT @ different voltages

PVT corner explosion and DVFS

Additional SLT drivers : Inter-IP block coverage, 3D effects (fin-cracks), ATE turn around times

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ATE: Goals

Automated Test Equipment (ATE) is any apparatus that performs tests on a device, known as the Device Under Test (DUT), using automation to quickly perform measurements and evaluate the test results

A typical sequence includes:

- Continuity / Opens & Shorts
- DC Pin parametrics
- Test Logic verification
- DC Stuck-at
- DC Logic Retention
- AC Frequency Assessment
- AC Logic Delay
- AC Pin Specification
- Memory Testing
- Memory Retention
- IDD and IDDQ
- Special vectors

Test Insertion Advantages / Drawbacks

Stage	Temperature	Tradeoff analysis		Screening
		Pro's	Con's	
WAFER SORT	COLD	Low static consumption	Low parallel scalability	**Effective for memories and logic** Not effective for H/S and I/F
	ROOM	Less demanding industrial setup	Low parallel scalability Not WC condition for majority of known failure modes	Not effective for H/S and I/F
	HOT		Low parallel scalability Probe limitation High static consumption	Effective for memories and logic Not effective for H/S and I/F
FINAL TEST	COLD		High parallelism might be not affordable Low efficiency High costs	Effective for memories and logic Not effective for H/S and I/F
	ROOM	Less demanding industrial setup	**High parallelism might be not affordable** Not WC condition for majority of known failure modes	Effective for memories and logic **Effective for parametric & assembly** **Not effective for H/S and I/F**
	HOT	Best case for activation of package/assembly defects	High parallelism might be not affordable	Effective for memories and logic Effective for parametric
BURN-IN	COLD → HOT	Low cost for <5W device	Cost not scalable for >5W device Very long duration (> hours)	Effective for memories and logic Not effective for parametric Not effective for H/S and I/F
SLT	MULTI-TEMP	Exercise device in true functional condition	Analytical coverage estimation, Difficult to map failure to root cause Long duration (> mins)	Effective for memories and logic Effective for parametric **Effective for H/S and I/F**

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SLT / ATE / Burn in content tradeoffs

SLT / ATE Tradeoffs

- Longer duration tests involving low pin count – Cheaper on SLT
- Continuity/ Parametric tests / High pin count structural tests – Easier on ATE

SLT / Burn in Tradeoffs

- Low speed JTAG, ATPG – Burn in focused
- Mission mode, at speed SW execution – SLT
- SLT often requires active thermal control as device gets hot running at-speed

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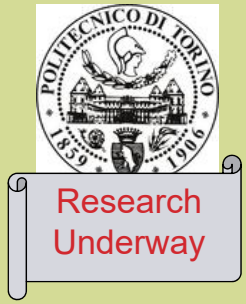
So what's going to change?

If SLT must be run on 100% of devices, then what insertions can be merged to lower overall costs?

- ATE / SLT:
  - Since SLT runs for multiple minutes, could you design your DFT to run slower/skinny scan? What is the cost of 30 seconds of SLT vs 3 sec of ATE time?
  - If SLT coverage includes all the high speed interface, is all the AC Scan still necessary at Final Test?
  - Can BIST be launched at SLT?
- SLT / Burn in:
  - Can the infant mortalities of burn-in be induced with high performance SLT with controlled thermal stress?

Alternatives being considered …



How can simple patterns be run at SLT?

- ATE / SLT:
  - Insert a functional program in flash using JTAG
  - Stimulate DUT emulating the environment with patterns from ATE
  - Sample DUT response
- SLT / Burn in:
  - Insert a functional program in flash using JTAG
  - Stimulate DUT emulating with environment patterns from application board
  - Store DUT response in memory and download the memory content

Why consolidate SLT/Burn-in solution?

- Modular solution
- Multi-temperature experiments
- Long test (SLT that has a typical duration of minutes) in a long test phase (Burn-in that has a typical duration of hours)
- High parallelism reduces cost and time

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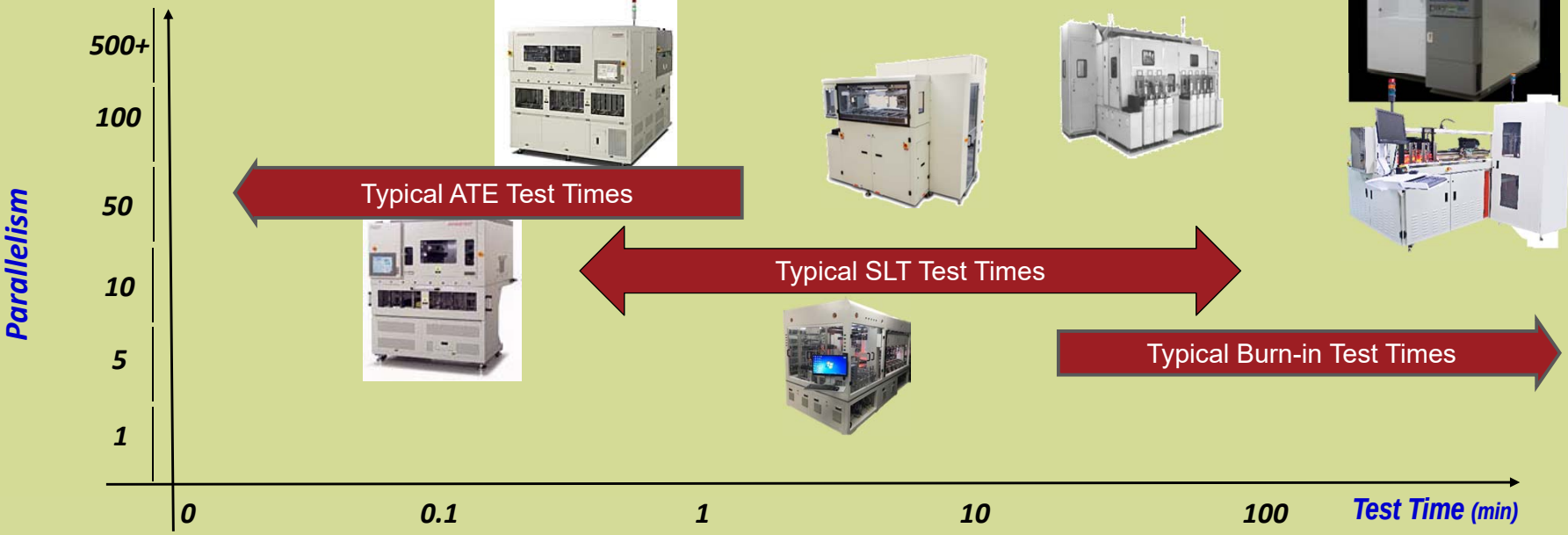
Pictures courtesy of Advantest & Astronics Test Systems

Handler / Test Time tradeoffs



From a handling/test time perspective

- SLT overlaps with ATE with test times from 30 secs – several mins
- SLT overlaps with burn in for 15 mins / longer test times
- SLT requires more pitch between sites to accommodate circuitry close to the DUT

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Conclusions

- For devices with longer time to market some SLT screened defects can be incorporated into ATE vectors eliminating/reducing the need for an SLT insertion
- With a massively parallel SLT architecture with thermal control, some of the infant mortalities found at burn-in could be screened at SLT.
- High speed interfaces screened at SLT could reduce need for at-speed scan test at Final Test
- SLT could run some slower patterns through a small number of pins more cost effectively.
- Long duration 'slow burn in' with some modifications could be altered to be similar to SLT with native speeds

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