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SLT Test Fundamentals & Challenges

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AMD

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- General Purpose of SLT
- SLT Challenges
  - Customization vs Standardization
  - Next generation features
- Conclusion

SLT Test Fundamentals & Challenges

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Purpose of SLT

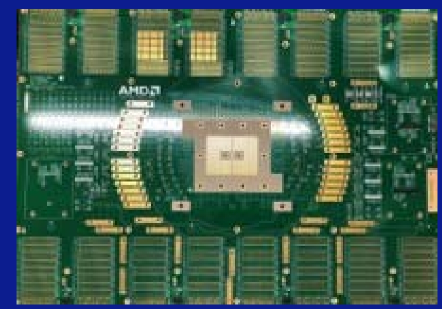
1. Fills the ATE coverage gap
2. Easier to match end-user experience
3. Lower Test costs

Baseline Test Insertions

ATE Wafer Sort	Burn-in Wafer/Package	ATE Package Test	SLT Package Test
		Yield > 98%	Yield > 99.xx%
▪ Coarse Performance Bucketing ▪ Stuck-at-Faults	▪ Accelerate Reliability Defects	▪ Finer Performance Binning ▪ Assembly defects ▪ Additional faults (temp or voltage related)	▪ Verify Performance Bin ▪ dPPM faults

Which of these matches better with End-User hardware & software ?

ATE



SLT

End-User

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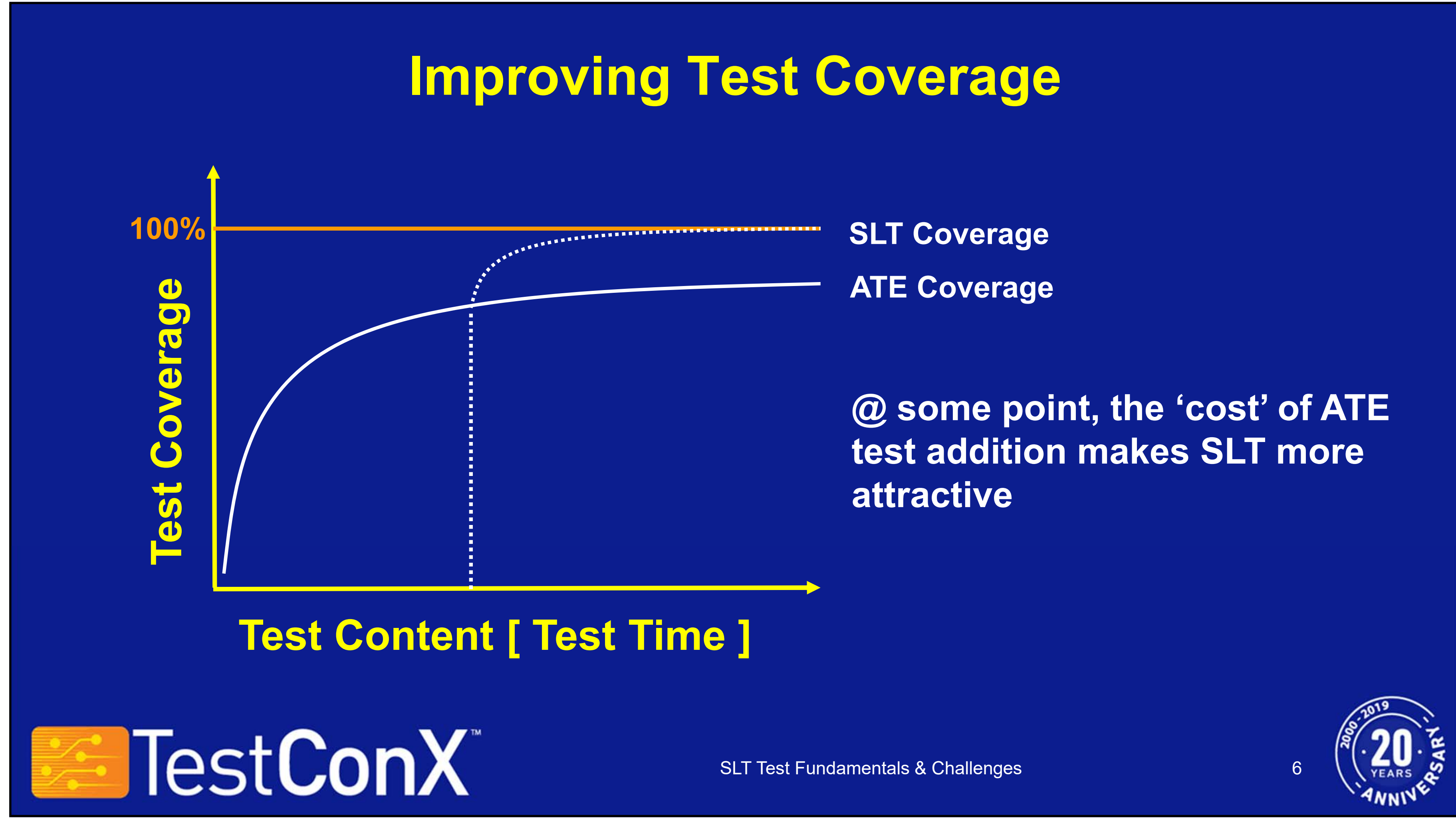
Improving Test Coverage
100%
Test Coverage
SLT Coverage
ATE Coverage
@ some point, the 'cost' of ATE test addition makes SLT more attractive
Test Content [Test Time]
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2000-2019
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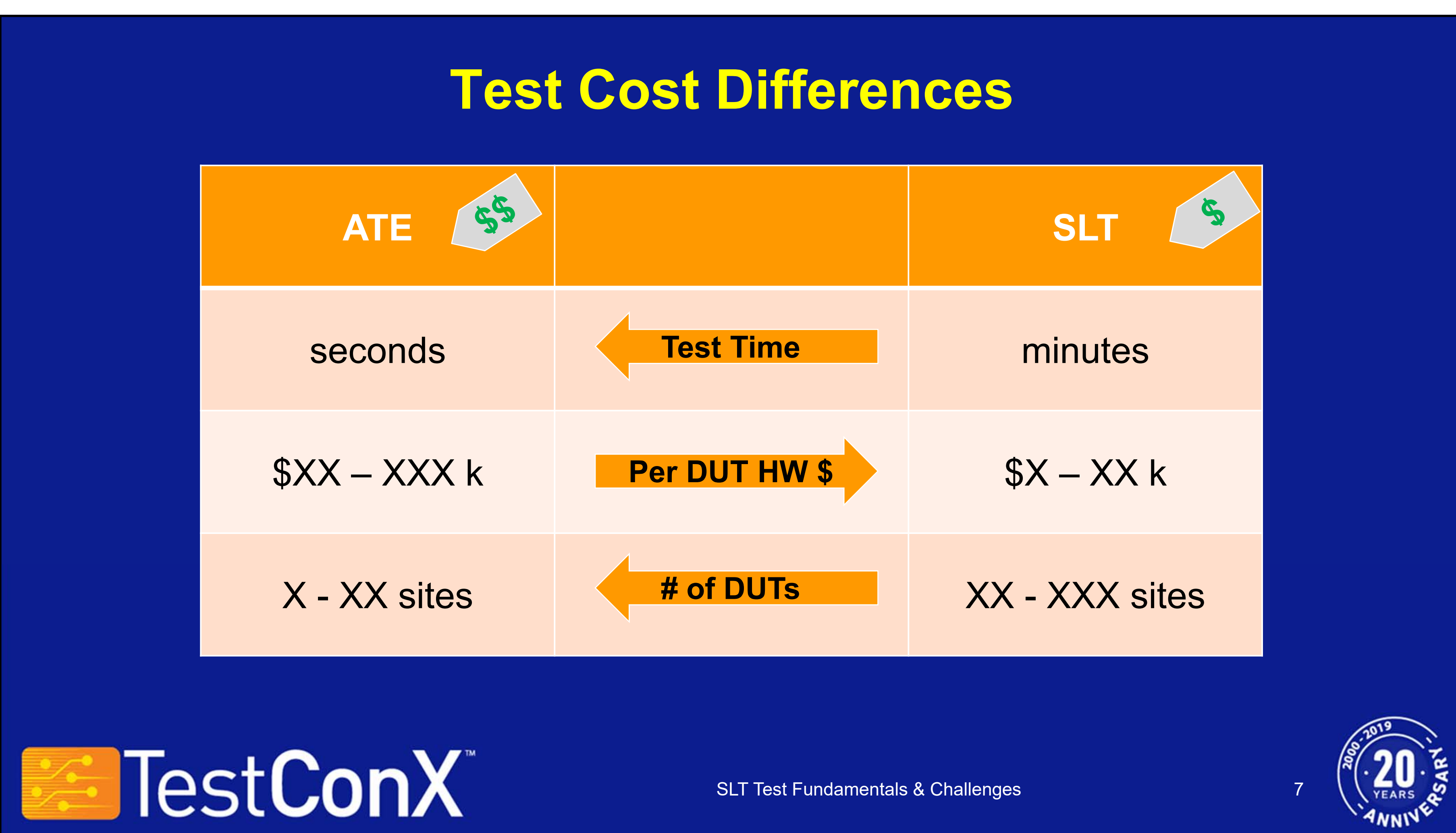
Test Cost Differences
ATE
$$
SLT
$
seconds
Test Time
minutes
$XX – XXX k
Per DUT HW $
$X – XX k
X - XX sites
# of DUTs
XX - XXX sites
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SLT Challenges

1. **Customization vs Standardization**
   - End-user modifications for SLT
   - Leverage ATE or Burn-in for SLT

2. **Next Generation Features → Higher Test Costs**
   - Power management
   - I/O Protocols & Speed
   - More features → Longer test times → More Capacity

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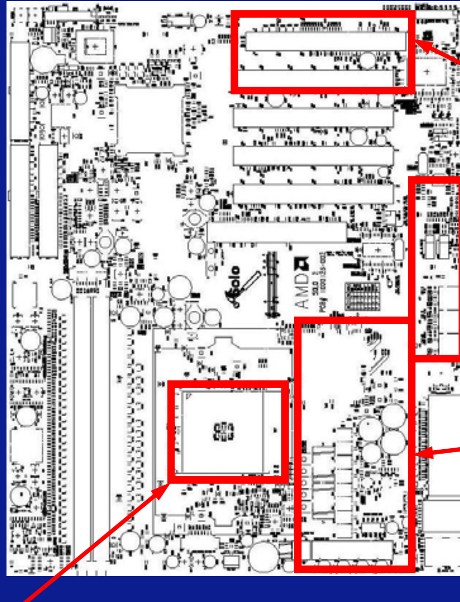
SLT Customization

Baseline : Reference Motherboard



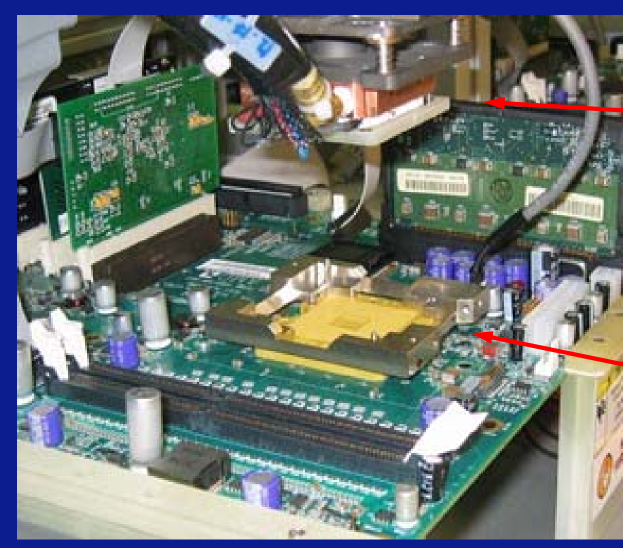
DUT Board
- Voltage Regulation
- Test control signals

Software
- Automated control
- Fail/Pass messaging

Thermal
- Active vs Passive
- High-Insertion

Sockets
- High-Insertion
- Handler compatible

SLT Customization



DUT Board
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Sockets
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ATE or Burn-in SLT Integration

Integrate SLT functions into ATE or Burn-in Infrastructure

[Accurate, Stable, Repeatable, Debuggable, Scalable]

ATE limitations

- SLT Test Time constraints
- ATE Instrumentation constraints
- SLT Component reliability

Burn-in limitations

- SLT Test Time constraints
- Burn-in Board space constraints

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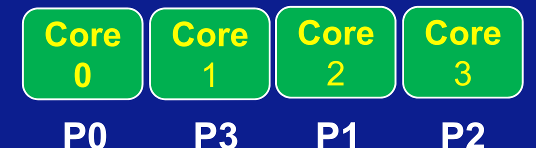
Next Gen Features - Power Management

Single P-State	Multiple P-States Single power plane	Multiple Finer P-States Independent power planes

P0

P0 P0



P0 P3 P1 P2

Px – Power State (Voltage, Frequency)

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Next Gen Features - I/O Protocols

[Multiple connectors | Faster bit-rates | Advanced Power Management]

Display

DP 1.0 → 1.1 → 1.2 → 1.3 → 1.4

HDMI 1.0 → 1.1 → 1.2 → 1.3 --> 1.4 → 2.0 → 2.1

USB

USB Type A/B/C

USB 1.0 → 2.0 → 3.0 → 3.1 → 3.2

PCIe

PCIe 1.0 → 2.0 → 3.0 → 4.0 → 5.0

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Concluding Remarks

- New Product features will continue to move faster than ATE or Burn-in capabilities… increasing the test cost burden into SLT.
- SLT in many ways is a mitigation to cover the coverage gap to guarantee end-user expectations.
- SLT Standardization (or integration into other test equipment) is starting to expand in both hardware and software environments allowing for better test support and scalability.

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