TWENTIETHANNUAI

estConX

March 3 - 6, 2019

Hilton Phoenix / Mesa Hotel Mesa, Arizona

Archive

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Session 2B Presentation 4

TestConX 2019

On the Bus - Advanced bus protocols for validation

A Scalable High Performance Mid-Bus Probing Solution for PCIe 4.0, 5.0, and Beyond

Xiao-Ming Gao Intel Corporation





TestConX Workshop

www.testconx.org

March 3-6, 2019

On the Bus - Advanced bus protocols for validation

Agenda

- Challenges of high speed I/O probing
- Pros and cons of existing probing solutions
- A new repeater based scalable mid-bus solution
- Case studies and simulation results
- Summary





On the Bus - Advanced bus protocols for validation



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Pros and Cons of Probing Solutions

Probing interposer

- Expensive and requires design of new board
- Probing channel interconnect may add extra distortion

Mid-bus solutions

- Easy to implement by adding bifurcation resistor/capacitors
- Probing channel interconnect has lower distortion



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PCB Board Stackups



Stackup 1: Dielectric: FR4

Stackup 2: Dielectric: Megtron 6

Common topologies:

Through hole and blind viasMain channel on layer 16Probing channel on layer 20Main channel:8.8"Probing channel:3"

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Channel Performance of Megtron 6 Board



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FR4 Board PCIe Gen 4 Simulation Data



Repeater input



Repeater recovered data



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FR4 Board PCIe Gen 5 Simulation Data



Repeater input



Repeater recovered data



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Megtron 6 Board PCIe Gen 4 Simulation Data



Repeater input



Repeater recovered data



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Megtron 6 Board PCIe Gen 5 Simulation Data





Repeater recovered data

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Megtron 6 Board PCIe Gen 5 Simulation Data



Repeater Tx output



Protocol analyzer received data

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Summary

- PCIe Gen 4 and 5 probing demands high performance platform
- Current probing solutions introduce extra distortions and have bandwidth limitation
- A repeater based probing architecture provides superior performance
- New design also scales well with future higher speed I/O



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Acknowledgements

The author would like to thank Naveid Rahmatullah for his inputs and Ayman Abdo for the review.



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