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Environmental Stresses Failures and Case Studies

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Abstract

Environmental stresses are critical tests to assess:

(a) Moisture sensitivity levels (MSL)
(b) Chip to packaging interactions (CPI)

Generally done during:

I. New Process or product's bringing up.
II. Assembly or package Qualification.

Critical to identify which process causing fails & to fix.

- ➢ To understand fail types and modes.

Environmental stress fail case studies presented.

Introduction: Environmental Stress Tests

Environmental tests done at package level:

1) Pre-Conditioning Stress Test **(PCT)** – includes MSL
2) Temperature Cycling Stress Test **(TCT)**
3) Highly Accelerated Humidity Stress Test **(HAST)**
4) High Temperature Storage Life Test **(HTSL)**

Others include:

- Autoclave Test **(ACT):** 100% moisture.
- Temperature Humidity Bias **(THB)**:
  - Slow temp. gradient version of HAST.
  - HAST & THB considered complementary.

Pre-Conditioning Test: Significance

Test for reliability of packages on to PCB

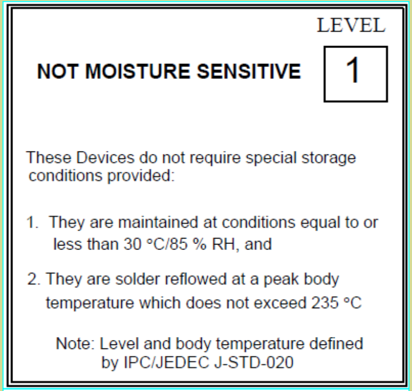
- Uses soak/moisture & Reflow.

Also tests for storage, cycling after packaging.

- Done before Environmental tests - except HTSL.
- Identifies Moisture Sensitivity Level (MSL).
- Assesses Chip to Package Interaction (CPI)
- Fails can be from Process, bumping or Assembly.
- Also done at wafer level as quick test.

Moisture Sensitivity Levels

- Plastic packages gets damage due to moisture
  - During high temp. surface mounting process.
- Appropriate precautions to follow [3]
  - Wrong moisture level cause fails.
- Different MSLs by JEDEC:
  - Level 1: 85°C, 85% RH, 168 hrs
  - Level 2: 85°C, 60% RH, 168 hrs
  - Level 3: 30°C, 60% RH, 192 hrs
  - Level 4: 30°C, 60% RH, 96 hrs
  - Level 5: 30°C, 60% RH, 48 / 72 hrs
  - Level 6: 30°C, 60% RH, 6 hrs



LEVEL

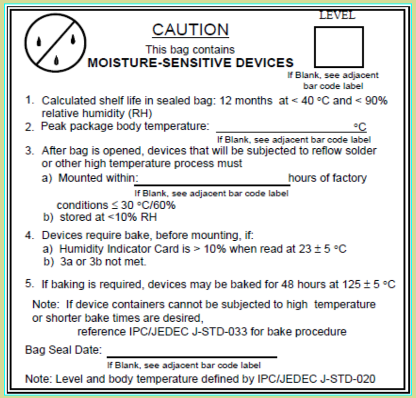
NOT MOISTURE SENSITIVE 1

These Devices do not require special storage conditions provided:

1. They are maintained at conditions equal to or less than 30 °C/85 % RH, and
2. They are solder reflowed at a peak body temperature which does not exceed 235 °C

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Levels: 2 to 5



CAUTION

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
If Blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at < 40 °C and < 90% relative humidity (RH)
2. Peak package body temperature: ____________ °C
   If Blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: ____________ hours of factory
   If Blank, see adjacent bar code label
   conditions ≤ 30 °C/60%
   b) stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23 ± 5 °C
   b) 3a or 3b not met.
5. If baking is required, devices may be baked for 48 hours at 125 ± 5 °C

Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: ____________
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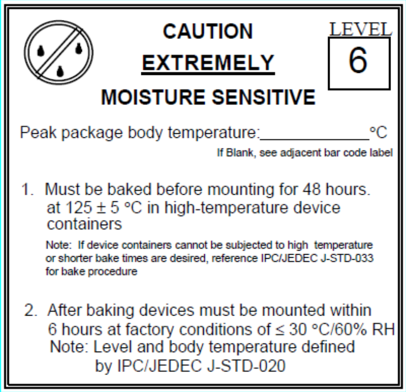
Note: Level and body temperature defined by IPC/JEDEC J-STD-020



CAUTION
EXTREMELY
MOISTURE SENSITIVE

LEVEL 6

Peak package body temperature: ____________ °C
If Blank, see adjacent bar code label

1. Must be baked before mounting for 48 hours. at 125 ± 5 °C in high-temperature device containers
   Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure
2. After baking devices must be mounted within 6 hours at factory conditions of ≤ 30 °C/60% RH
   Note: Level and body temperature defined by IPC/JEDEC J-STD-020

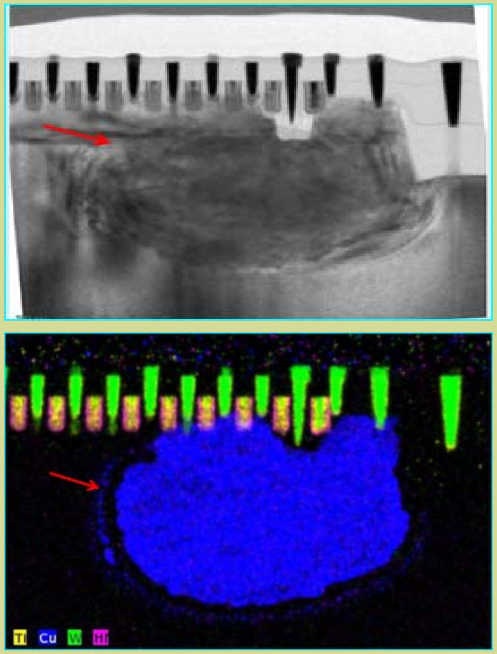
PCT Fails: Case Study - 1

Background: Functional fails after Packaging on new product.

- Electrical Test, sort & yield on other products: OK ➔ not Fab.
- **FA:** Showed Cu migration from wafer backside.
- Fails on 1 of 2 assembly, using wet backgrind (BG).
  - BG/wafer thinning done at Assembly to 150mil.
- **Hypothesis:** Cu particles from wet BG gets attached to wafer back and slowly diffuse through Si causing fails.
- **Screen:** PCT used to separate good vs. bad lots.

Cu Migration after PCT & FA Findings

- Wafers have 30-70nm protection layer.
- Fails on assembly using Cu slurry.
- Customer's 2nd assembly - No fails.
  - Uses dry polish BG – No "Cu" slurry.
- To prove "Cu" is not from Fab.
- 10xPCT to separate which area.
- Fails appear on lots with wet BG.
- CA/PA: BG process changed to dry.
  No more fails observed.



Temperature Cycling Test (TCT) - Significance

TCT is Package reliability test for:

TCE – Thermal Coefficient of Expansion

- TCE mismatches & Thermo-mechanical strength.
- Adhesion between process layers & materials
- Checks for rated Temp. Operating range.
- Also between chip and package materials.
- Coffin Mansion: $AF_{,TC} = [(T\max, c - T\min, c) / (T\max, o - T\min, o)]^{m}$
- Fail Rate: $FR = [Pn(1\text{-}CL, 2f+2) \times \#\ \text{of use temp cycles per hour} \times 10^{9}] / [N \times Tc \times AF, (FIT)$

Different Types of TC Tests

TC Type	Air to Air	Liquid to Liquid	Power Cycling
Test Name	Temp. Cycling	Thermal Shock	Power & Temp Cycling
JEDEC	JEDEC22-A104	JEDEC22-A106	JEDEC22-A105
MIL-Std-883	Method: 1010.7	Method: 1011.9	Power: 5mins on & off
# of Chambers	1/2/3 Chamber	3 Zones: LT, RT, HT	Single Chamber
Temp. Range	- 65°C ~ +150°C	- 65°C to +150°C	- 40°C to +150°C
Soak/Dwell	1 to 15 minutes	1 to 15 minutes	10 minutes
Transfer Time	< 1 minute	1 to 5 minutes	20-30mins
Duration	1000 cycles	300 cycles	1000 cycles

- **Wafer Level Thermal Cycling: Device/test structures.**

TCT Test Fails: Study - 2

Background: Module level fails after TCT.

- 1/77 fail at 500cy, Bin5 continuity, Pin A6 Open.

- **EFA**: I-V curve trace confirm Pin A6 fail - “Open”
  - ✓ CSAM shows ➔ no de-lamination.
  - ✓ Optical inspection ➔ no anomaly at fail pin.

CSAM – Confocal Scanning Acoustic Microscopy

E/PFA: Electrical/Physical Failure Analysis

- **PFA**: Layer by layer de-processing & inspection.
  - No anomaly at M6,V5 but abnormality at Via 4.
  - PVC at fail pin showed some contrast Via-4.

PVC: Passive Voltage Contrast

TCT Fail FA & Findings

- **TEM** ➔ dark contrast & abnormal via-4.

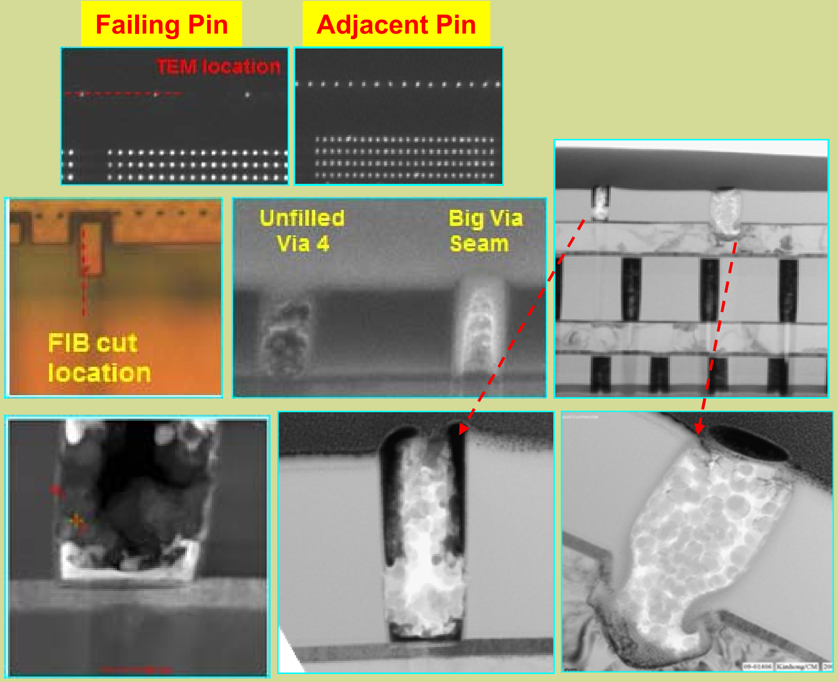
  TEM: Transmission Electron Microscopy

- **FIB** ➔ Partially filled via-4.
  - Big via seam on adjacent via.

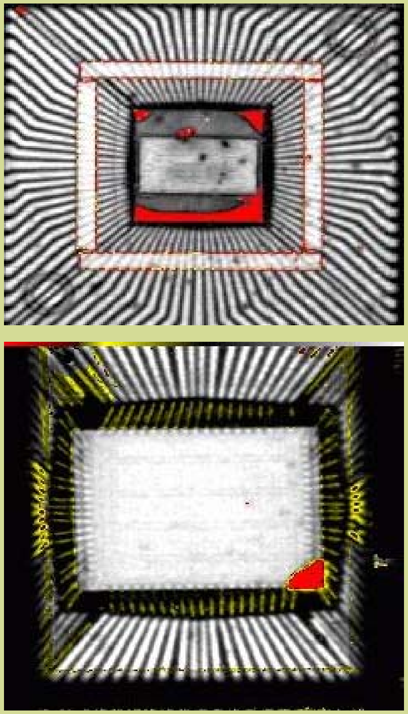
  FIB: Focused Ion Beam

- **EDX** ➔ Missing TiN at via sidewall

  EDX: Energy Dispersive X-ray Spectroscopy

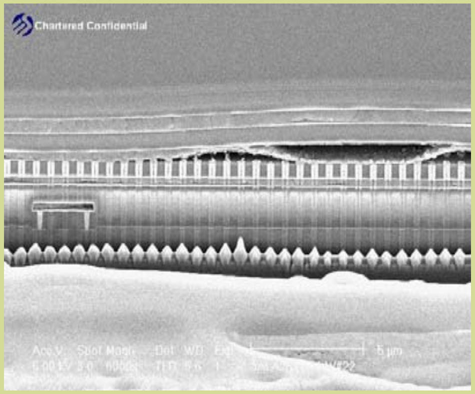


Other TCT Fails - Examples

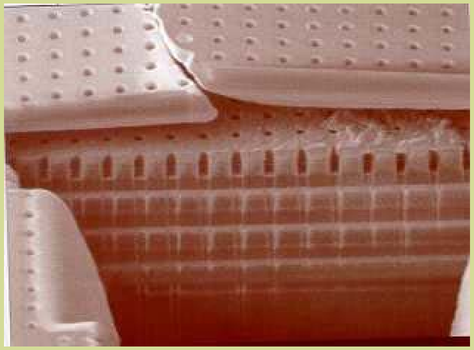


Mold compound De-laminations

Process Layer De-laminations



ILD/IMD Crack



IMD/ILD: Intra Metal or Layer Dielectric.

Highly Accelerated Humidity Stress Test

HAST test is done to ensure:

- Robust enclosure of package type
- Under High temp., Pressure & Moisture.
- Modes: DC/static Bias [6] or un-biased [7].
- Alternate pin bias: minimum dissipation.
- 96hrs – Biased & 232hrs - un-biased.

HAST test brings out:

- Weakness in the packaging materials
- Against moisture seepage.

HAST Fails: Study - 3

Background: Customer reported modules fails after HAST.

Failure Analysis: Fails show passivation crack.
- PIT: Passivation Integrity Test show cracks on fails.

Checks: Initial on process & assembly ➔ No abnormality.
- Crack stop, Guard Ring, MOB ➔ OK. Cracks on die.
- Other Qual on assembly ➔ No fails on TC/THB/HAST.
- Epoxy from renowned, long term supplier.

MOB: Moisture Obstruction Barrier

Hypothesis: Once passivation cracks happen, HAST infusing moisture into device to cause fails.

HAST Fails & Findings

Epoxy form & mold cure temp. checks:

- Triangular/cylindrical & bigger/smaller.

Compared with other assembly on epoxy:

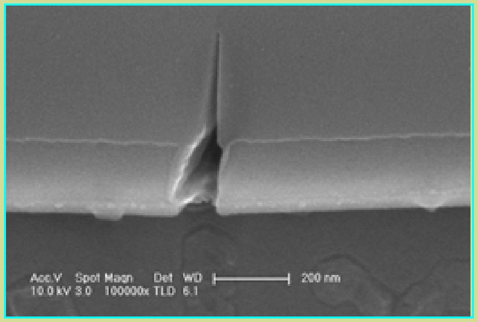
- Failing assembly uses triangular granules
- Mold cure temp. & duration - different

Proposed to change fillers to cylindrical &

- Increase mold cure temp to correct 4.5hrs.

CA/PA: After granules & mold temp. changes:

- Subsequent lots show ➔ No cracks.
- PIT & HAST tests passed on 3 lots.
- Customer agreed on Assembly issue & released line.



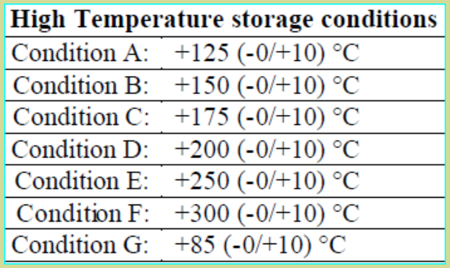
Passivation crack

CA/PA: Corrective & Preventive Action

High Temperature Storage Life Test

To assess storage life thro’ supply chain to user.

- Product still functions without any deviations.
- Tests on effect of temp. & storage time for fails.
  - Storage at Warehouse, Distributor & shelves.
  - Storage after Chips mounted onto PCB or Cards.
- Mechanisms that effect electrical parameters:
  - Oxide growth, Degassing, Tin whiskers/Dendrites & migrations.
- HTSL Depends on storage conditions: Temp & duration
  - Seven levels are defined by JEDEC.
  - Done to 1000hrs with 250hr, 500hr readouts.



High Temperature storage conditions	
Condition A:	+125 (-0/+10) °C
Condition B:	+150 (-0/+10) °C
Condition C:	+175 (-0/+10) °C
Condition D:	+200 (-0/+10) °C
Condition E:	+250 (-0/+10) °C
Condition F:	+300 (-0/+10) °C
Condition G:	+85 (-0/+10) °C

HTSL Stress Significance

- Critical Environmental tests & brings up:
  - Voids in Vias, incomplete nucleation of metals
  - Partial /un-landed /misalignment on Vias/Contacts.
  - Degassing, Anneal, Nucleation on process/materials.
  - Parametric shifts & current/leakage issues.
- Important for eFuses, O/MTPMs, NVMs on:
  - Data Retention & Endurance Cycling
  - Post Program & Pre-cycling screens.

O/MTPM: One/Multi Time Programmable Memory
NVM: Non-Volatile Memory

HTSL Test Fails: Study - 4

Background: Yield drop & fails after HTSL package test.

- Fails from 0.35um Fab transfer process with Al BEOL.
- Bad wafers show “Wafer Right side fail” pattern.

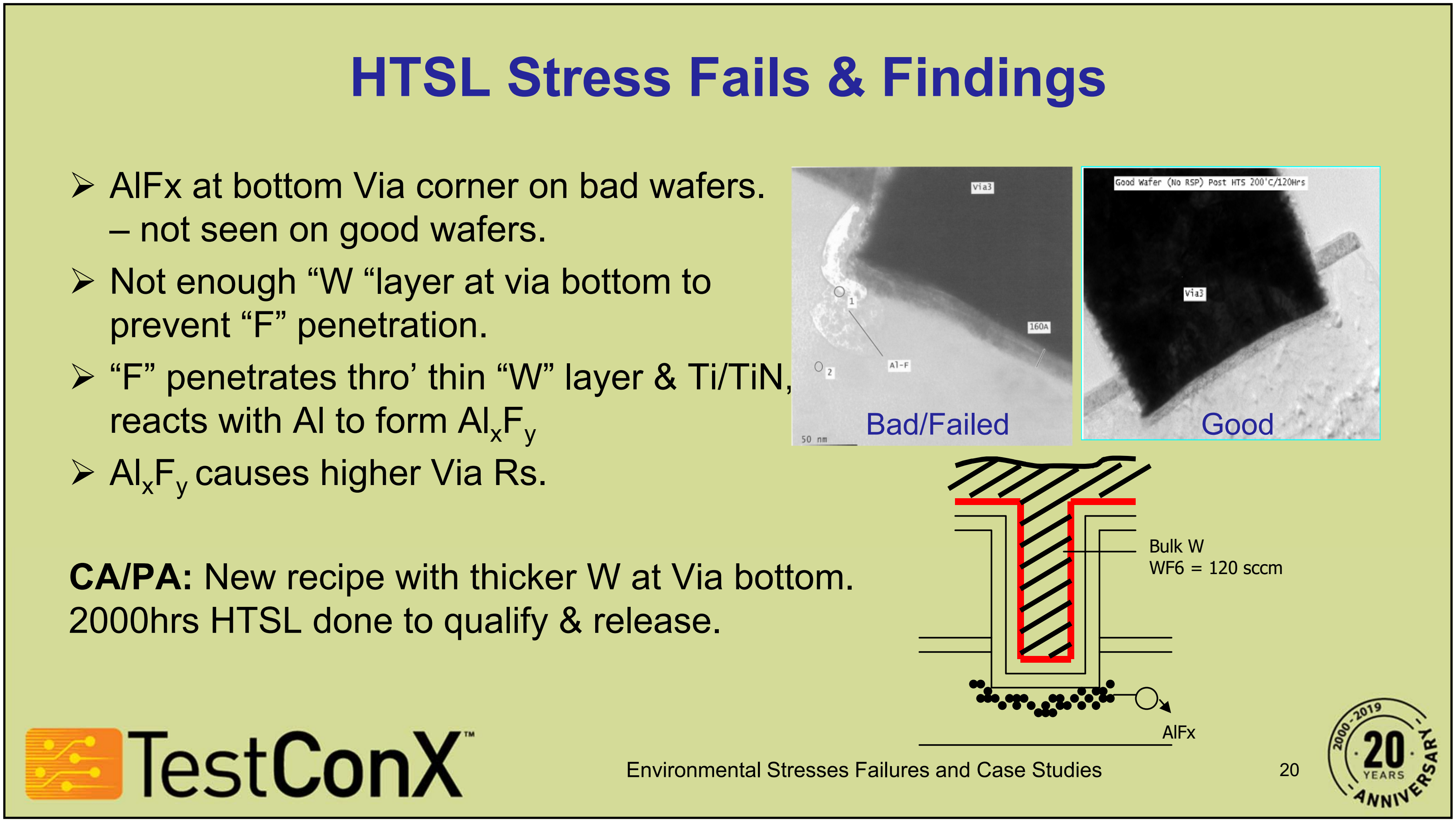
FA: Analysis shows anomaly at Via-3 – confirmed.

Fail Signature: Via resistance (Rs) increase causing fails.

Hypothesis: Fluorine from WF6 pre-W Dep. step go through nucleation layer, Ti/TiN barrier & react with Al to form AlxFy.

Correlation: AlxFy results in high Via resistance detected by HTSL.

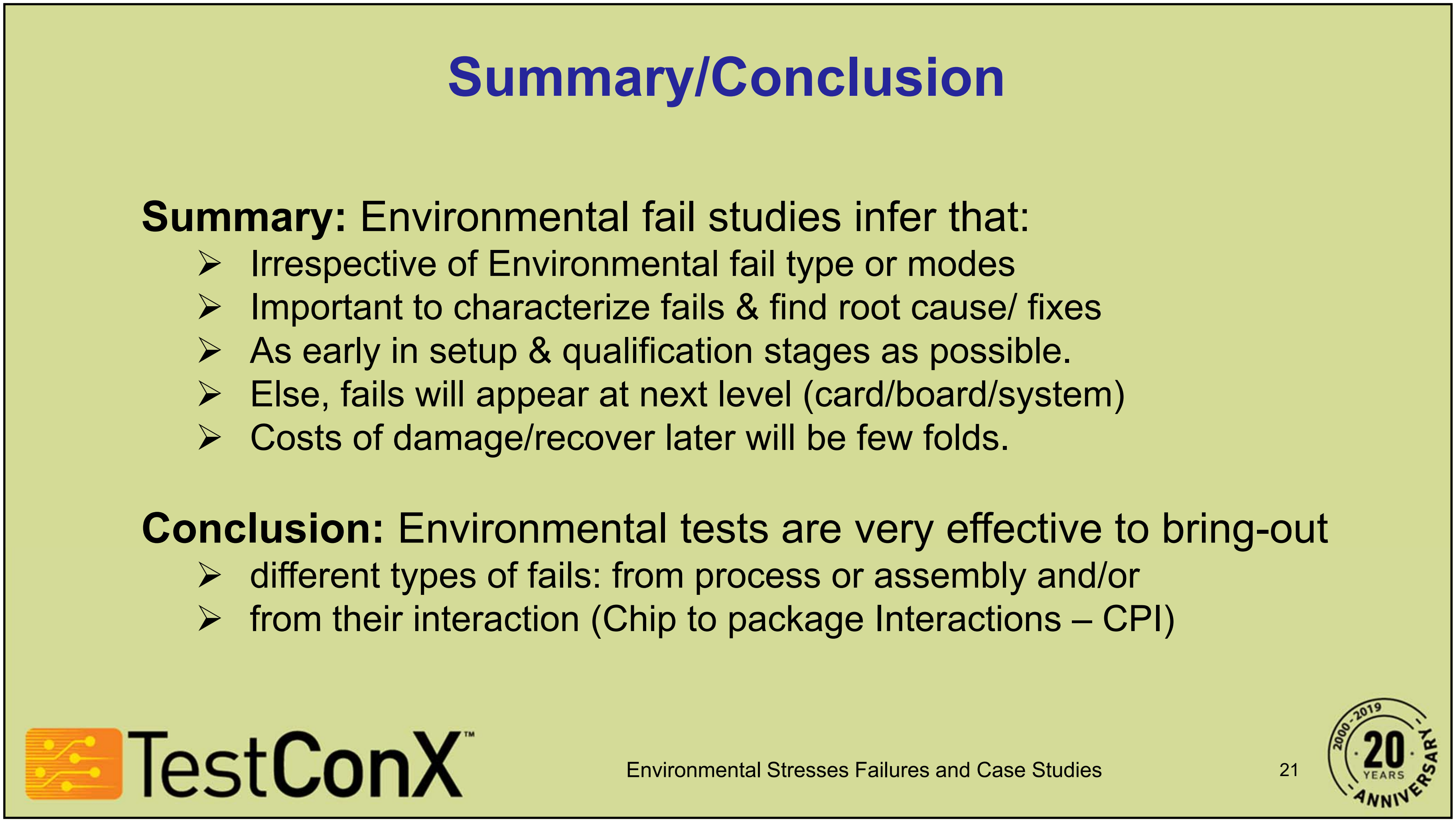
AlxFy: Aluminum Fluoride, can be Al_2F_3 or Al_4F_6



HTSL Stress Fails & Findings

- AlFx at bottom Via corner on bad wafers. – not seen on good wafers.
- Not enough “W “layer at via bottom to prevent “F” penetration.
- “F” penetrates thro’ thin “W” layer & Ti/TiN, reacts with Al to form Al_xF_y
- Al_xF_y causes higher Via Rs.

CA/PA: New recipe with thicker W at Via bottom. 2000hrs HTSL done to qualify & release.



Summary/Conclusion

Summary: Environmental fail studies infer that:

- Irrespective of Environmental fail type or modes
- Important to characterize fails & find root cause/ fixes
- As early in setup & qualification stages as possible.
- Else, fails will appear at next level (card/board/system)
- Costs of damage/recover later will be few folds.

Conclusion: Environmental tests are very effective to bring-out

- different types of fails: from process or assembly and/or
- from their interaction (Chip to package Interactions – CPI)

References

1] J-STD-20: Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices.
2] JEP-113: Symbol and Labels for Moisture Sensitive Devices
3] J-STD-033: Handling And Shipping Of Moisture Sensitive Surface Mount Devices
4] JESD22-A113: Preconditioning of Non-hermetic Surface Mount Devices Prior to Reliability Testing
5] JESD22-A104: Temperature Cycling Test
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7] JESD22-A118: Accelerated Moisture Resistance - Unbiased HAST
8] JESD22-A101: Steady State Temperature Humidity Bias Life Test
9] JESD22-A103: High Temperature Storage Life Test.
10] JEP-156: Chip-Package Interaction Understanding, Identification & Evaluation.