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Validating LPDDR4x memory in a Package-on-Package (PoP) architecture using a ball grid array (BGA) interposer

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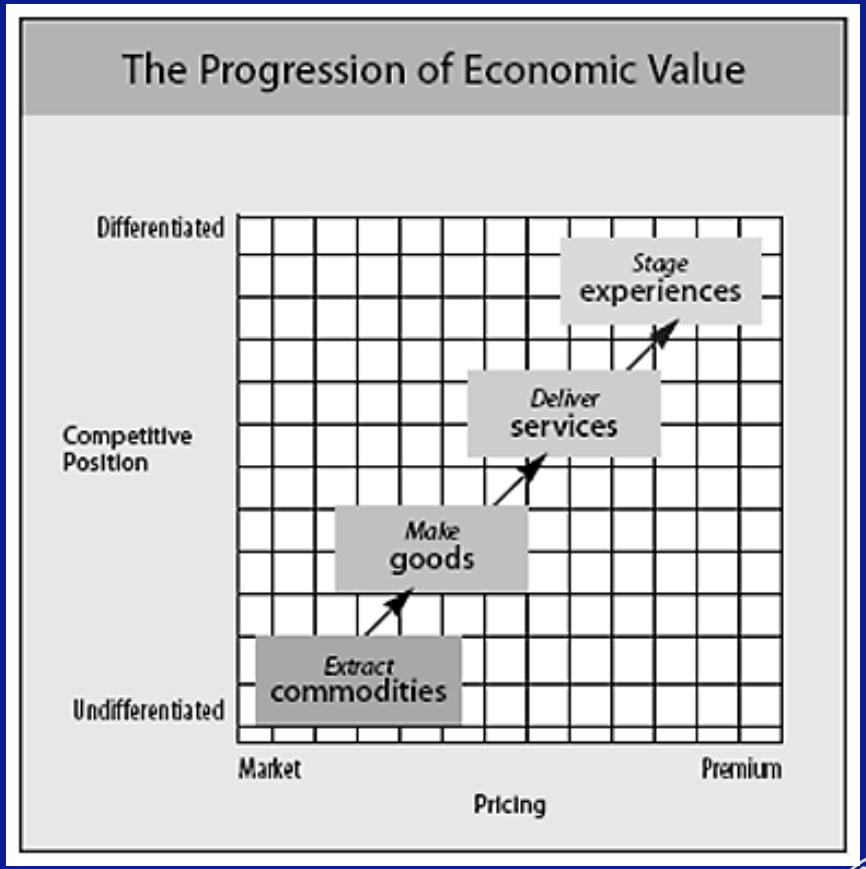
Experience economy

- Semiconductor engineers now deliver experiences

- https://hbr.org/1998/07/welcome-to-the-experience-economy



Novel validation solutions

- We need to look at our business as more than simply the building and selling of personal computers. Our business is the delivery of information and lifelike interactive experiences. – Andy Grove
- An experience occurs when a company intentionally uses services as the stage, and goods as props, to engage individual customers in a way that creates a memorable event.
- Validating our products has reached a new scale.
  - Not only the transistor, but the experience as a whole such as protocols, HW architectures

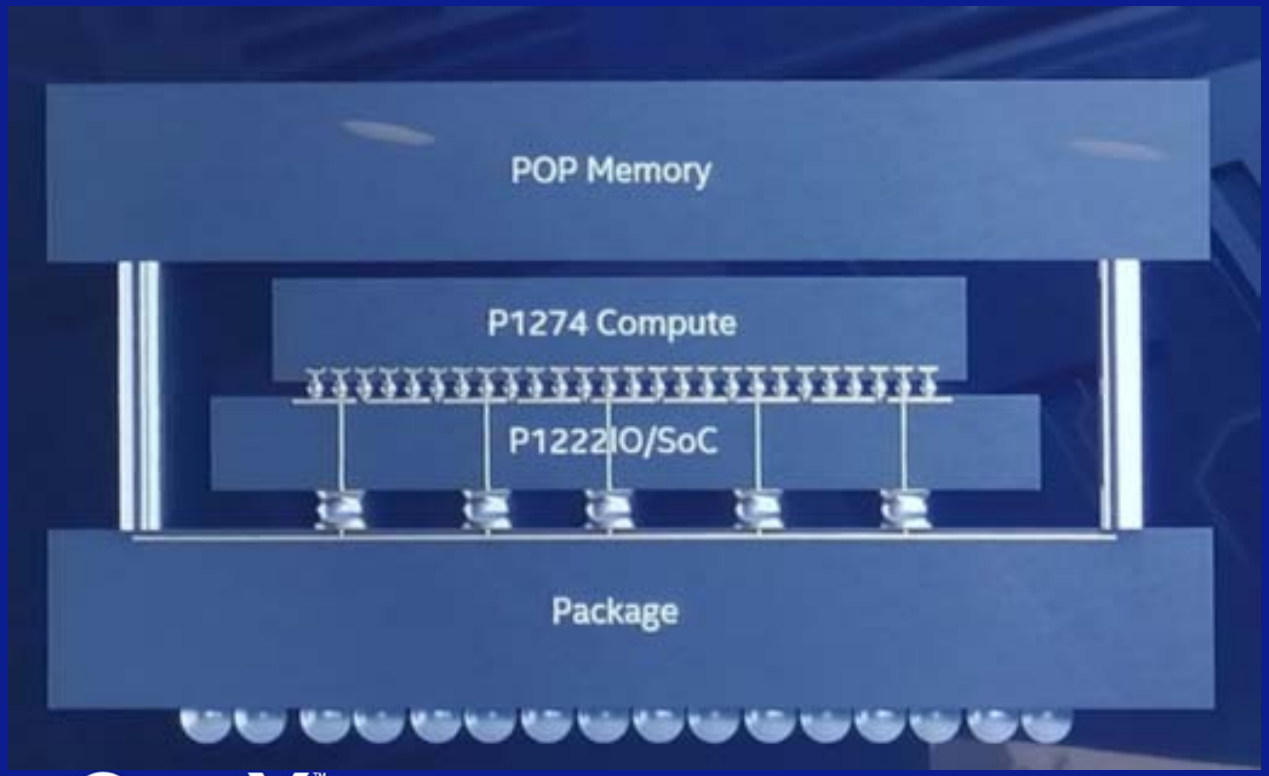
Contents

- Probing card for a Package-on-Package (PoP) Configuration
- Challenges: Signal integrity
  - Loss of amplitude of signal; maintain physical characteristics
  - The people debugging have to see the exact same thing that the SoC does.
- Challenges: Power integrity
  - Prototyping, consider all situations
- Challenges: Mechanical stack
- Challenges: LPDDR4x technology
- Validation results (Speed, Voltages)

Why do we need this solution?

- Validated HW improves customer experience
- New, more complex, more efficient memory
  - Power per bit of data transferred keeps going down
- Interposers allow to reduce complexity of motherboard and aiding OEM adoption of the part.
- New ways to validate Package–on-package architectures

Why do we need this solution?



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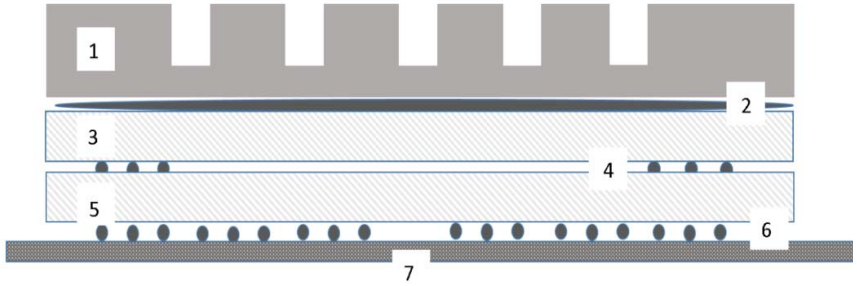
Validating LPDDR4x memory in a Package-on-Package (PoP) architecture using a ball grid array (BGA) interposer

Electrical and functional validation

- HW validation solution for the memory interface inside the package-on-package stack.
- Simulations of a myriad electrical structures to carry 2.1GHz signals.
- A ball grid array (BGA) interposer featuring 12L and 70um laser via technology
- Simulation driven layout of a fly-by routing topology.
- Ability to run with the latest logic analyzer cards from a single vendor
    - Keysight (U4164A), allows to run the analyzer engine using the system clock, or what they call “State mode”.

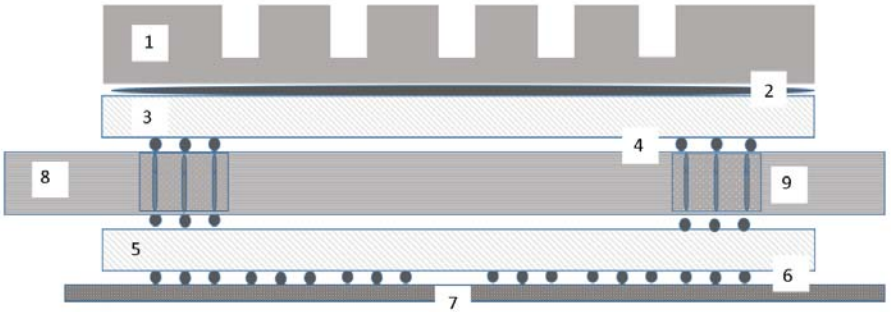
Package on Package probing card

Platform package assembly



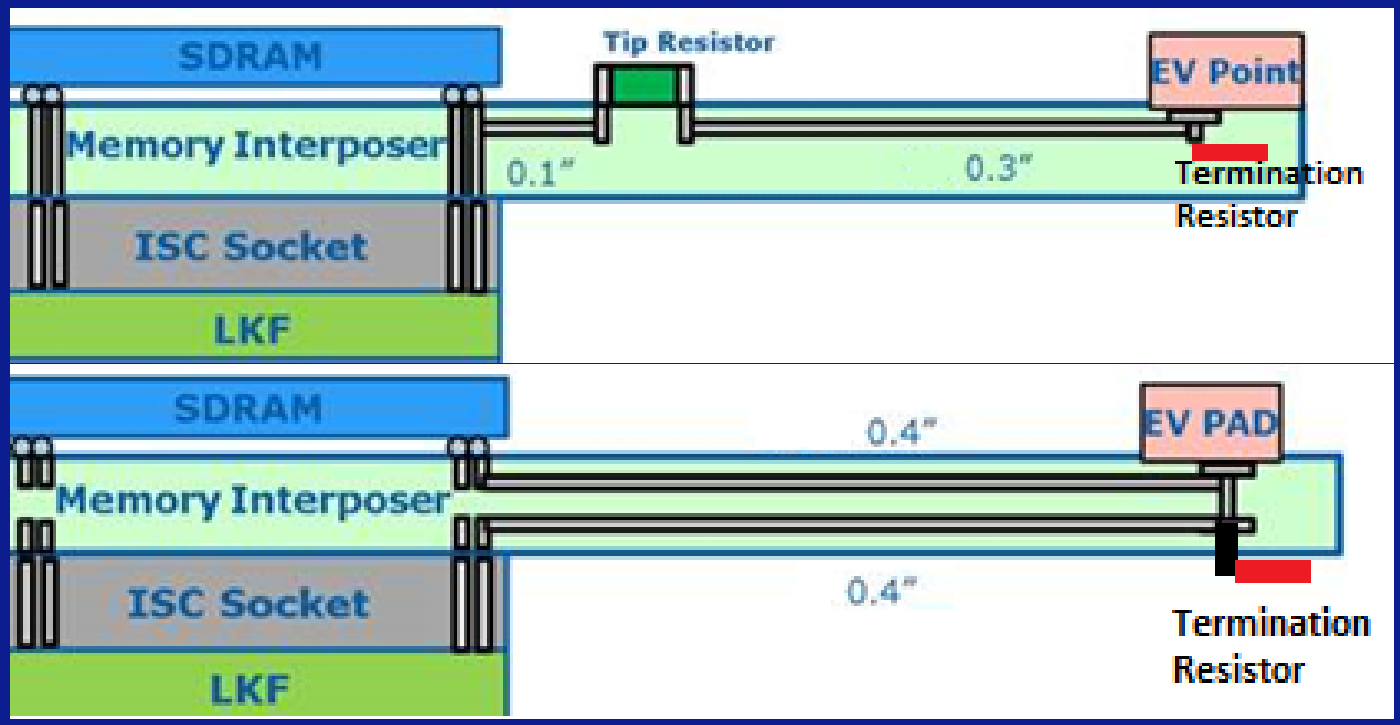
1 Heat Sink
2 Thermal adhesive
3 TOP die (usually memory package)
4 Solder ball array to connect TOP and BOTTOM die (additional filler material not shown)
5 BOTTOM die (usually CPU die)
6 Solder ball array to connect BOTTOM die and motherboard(additional filler material not shown)
7 Motherboard

Probing package assembly



1 Heat Sink
2 Thermal adhesive
3 TOP die (usually memory package)
4 Solder ball array to connect TOP and thermal interposer (additional filler material not shown)
5 BOTTOM die (usually CPU die)
6 Solder ball array to connect BOTTOM die and motherboard(additional filler material not shown)
7 Motherboard
8 Heat dissipating structure (heat conduction with solid copper, forced air heat exchanger or heat pipe)
9 Fiberglass with microvia pattern (plated through via or laser via)

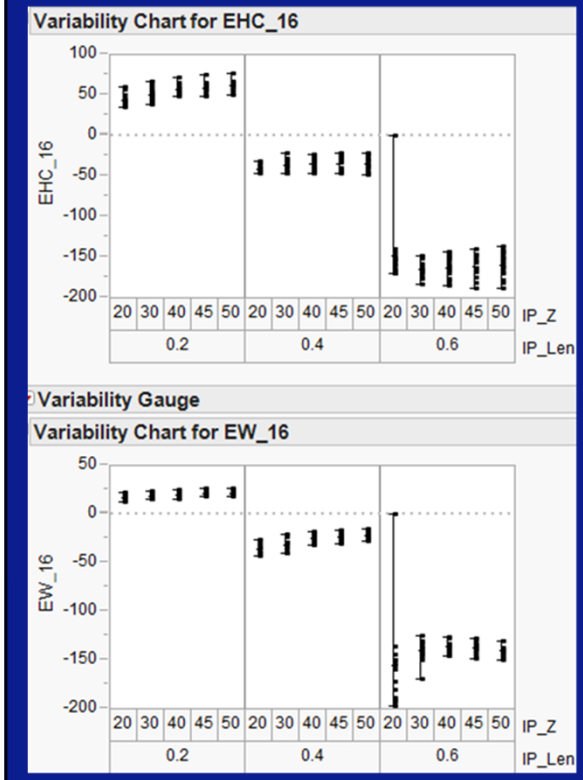
Probing methodology: Fly By vs. T topology

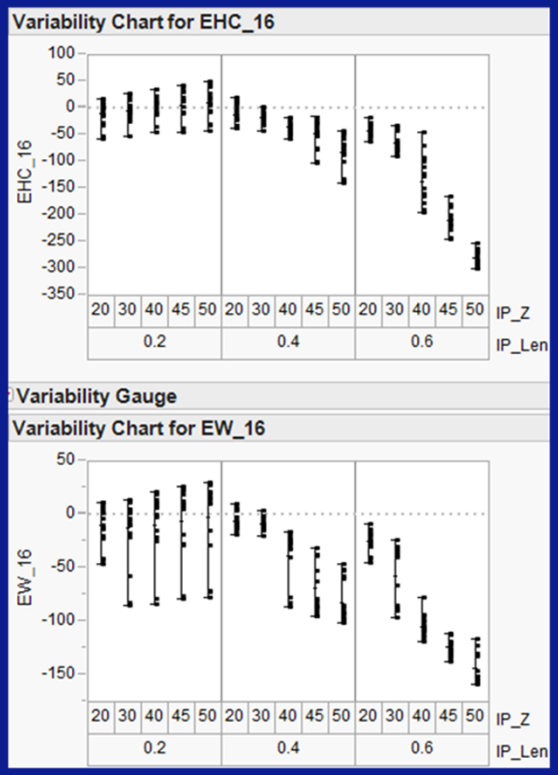


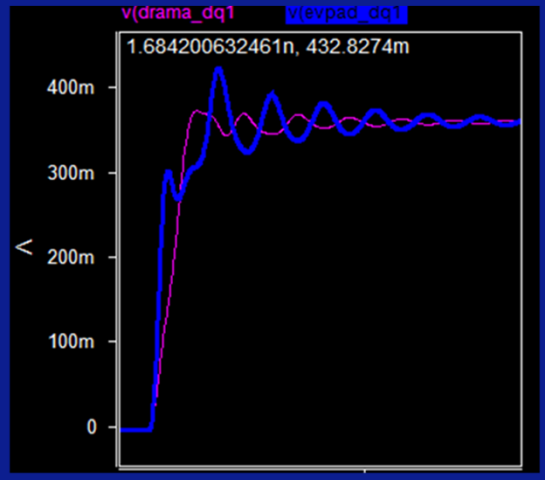
T topology

Fly By

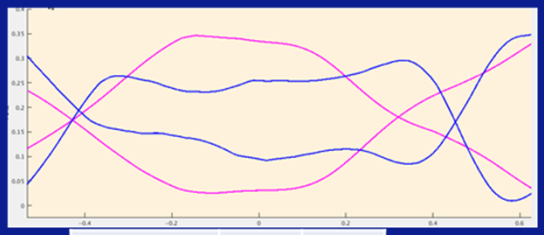
Simulation results







Electrical Simulations



Load	EW_16	EHC_16
dramA_dq1	15.96	48.06
EVpad_dq1	-14.91	-10.95

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LKF EV/SV Mem interposer: SI

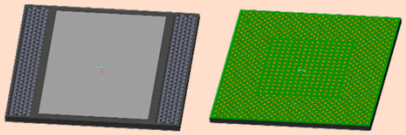
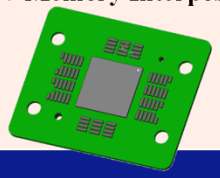
- DQ/DQS group tight matching to 5mils including package trace lengths.
- Stacked via design due to 0.35mm ball pitch.
- Due to the small pitches, stacked micro-vias were used.
- An innovative core-less micro-via 14 layer stack-up to optimize for signal integrity.

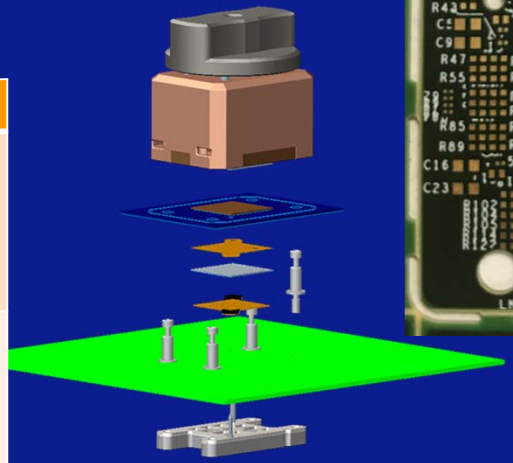
Power delivery

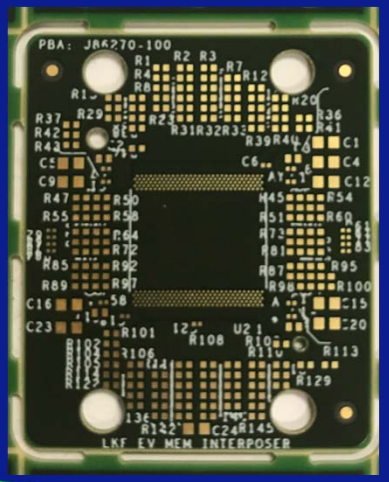
- Probing interposer adds a inductance to the power delivery network (PDN) for the memory chip
- Caps placed on the interposer to try to compensate for extra inductance
- A low pass filter in frequency domain is what the interposer is doing
- Interposer designed to max. current supported by memory part, this is not what the normal operation of the memory consumes
- Current consumption measurements not supported by interposer

Solving the mechanical architecture challenge or how to hold everything together

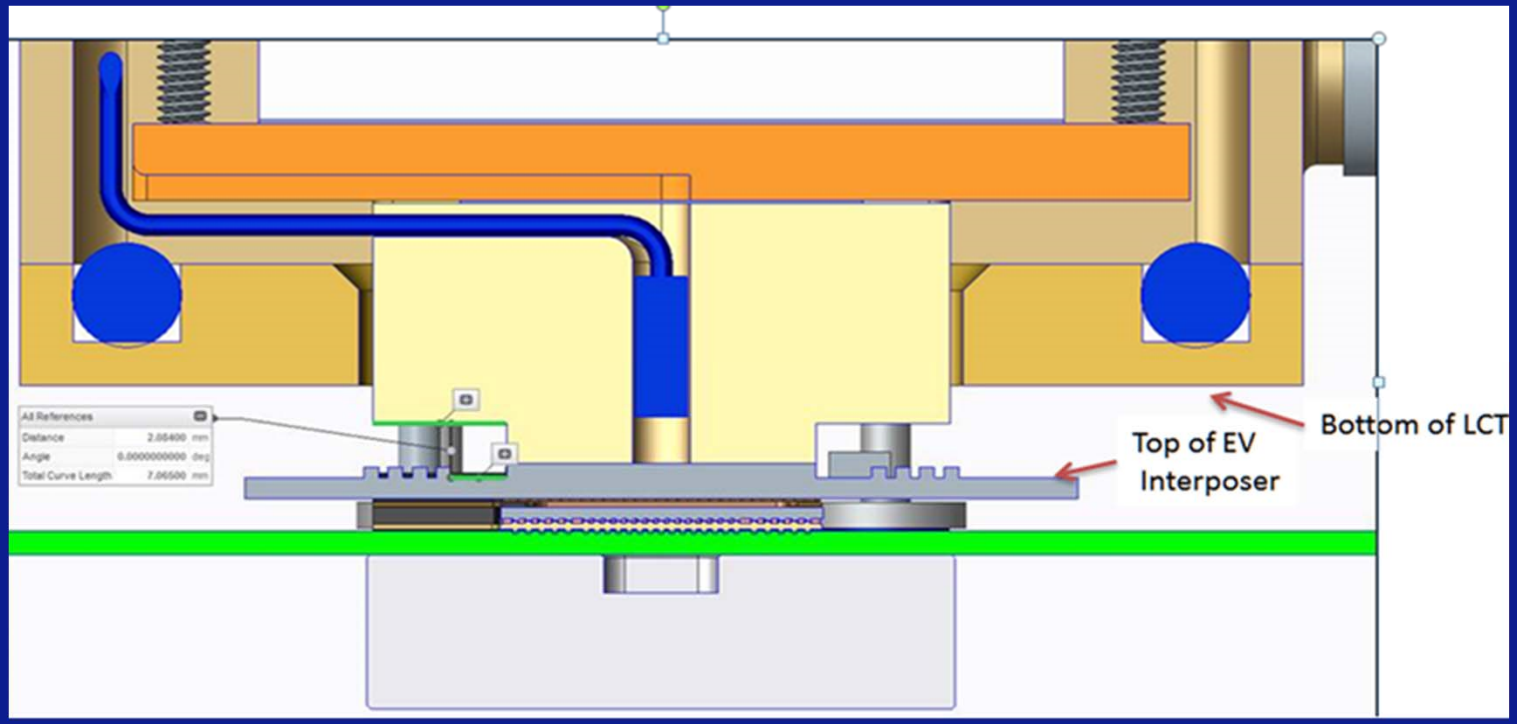
- Agilent N5381A Probe
- Discrete LKF SoC has LGA pads on the bottom
- Full frame LGA SoC socket
- Memory Interposer LGA socket

Packages	Sockets
LKF SOC (Discrete) 	ISC LGA SoC Socket 
LKF EV Memory Interposer 	ISC LGA Mem. Interposer Skt. 

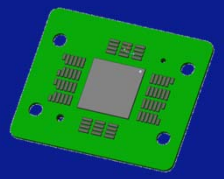




Mechanical architecture: cooling mechanism

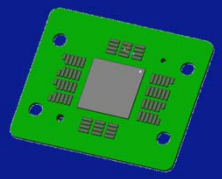


Validation results



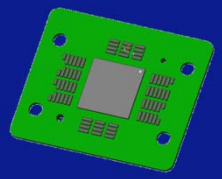
- Functional and electrical verification completed successfully
- One system configuration bug identified with the aid of this interposer
- Power delivery network
  - Voffset@2133Mhz => 200mV
  - Voffset@4166Mhz => 150mV

Conclusions



- Probing BGA interposers, a cost effective solution to validate complex memory protocols
- Package-on-package architecture requires custom mechanical solution for validation
- Simulation driven PCB design is no longer a choice but a requirement
- Customer experience focus, delivering validated solutions

Acknowledgements



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