
TWENTIETH ANNUAL
TestConX™
March 3 - 6, 2019
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive

COPYRIGHT NOTICE

www.testconx.org

Reliability Testing of Panels and Strips

Carl Kasinski
Aehr Test Systems

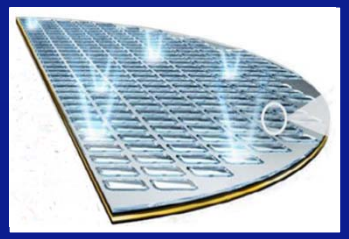
TestConX™
Mesa, Arizona • March 3 - 6, 2019

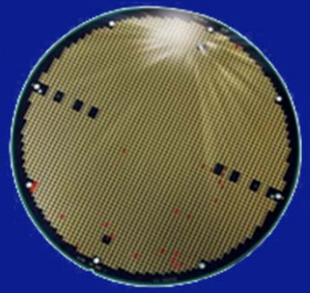
2000 - 2019 20 YEARS ANNIVERSARY

AEHR TEST SYSTEMS

New Packaging Technologies

- New packaging trends for smartphones, communication and automobiles
- Single, stacked die or multi-chip packages integrated into panels or strips for high volume production
- Share common substrate yet require individual resources for parallel test and burn-in



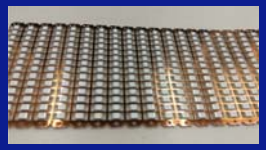


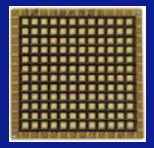
What is a Panel or Strip of Devices

- 100's –1,000's of devices on single substrate
- Panel/strip packaging advantages:
  - Lowers test cost
  - Increases production throughput
  - Simplifies handling

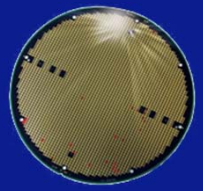
Early strip designs

QFN / uBGA panels



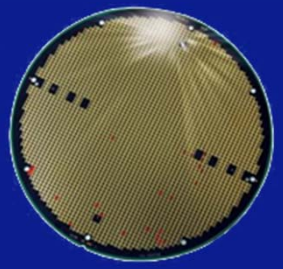


Wafer level panels

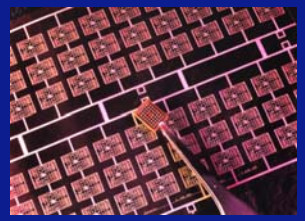


Examples of Panel/Strip Substrates

- Devices assembled onto a substrate and handled/tested in a wafer or tray format
- Advantages:
  High density handling/test using wafer or tray handling equipment
- Challenges:
  Substrate planarity in Z-axis, CTE effects and optical alignment requirements



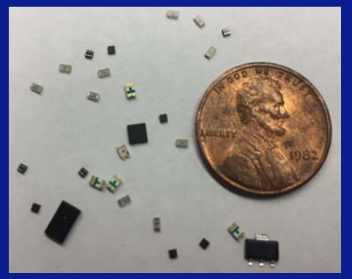
Wafer Format Panel



Tray Format Strip

The Evolution of Panel/Strip Test

- Parallelism increases over last 10-15 years
- Lower ASPs driving higher parallel test
- Increased reliability requirement
  - ADAS, self-driving cars, mobile & security
- Optical test challenges
- Packages are getting smaller



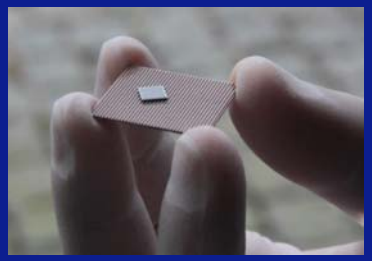
Chip Scale Packages (CSPs)

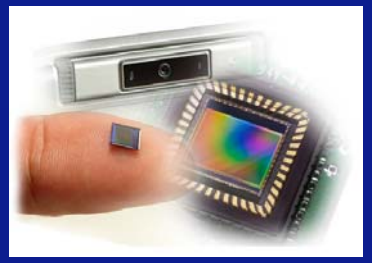
Device Shrink Handling Challenges

uCs - 1985

uCs - 2005

uCs – CSP Format

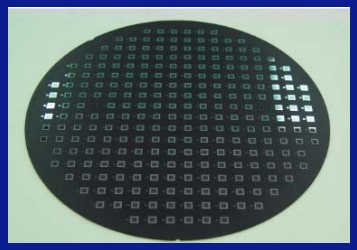




Packaging evolution for microcontrollers

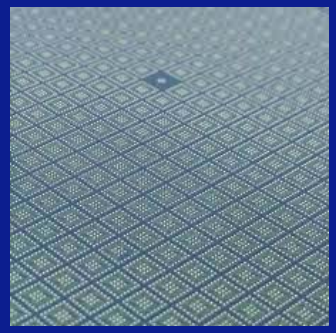
Reported Benefits of Panel/Strip Testing

- Reduced cost of test
- Reduced cycle time
- Consistently higher yields and quality
- Faster time for test development
- High strip density
- Reduced floor space and improved equipment utilization
- Immediate feedback and part traceability



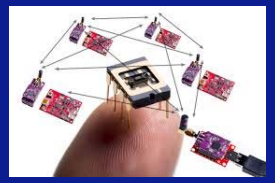
Reported Challenges Encountered

- Implementation of new required equipment
- Very precise alignment contactor capabilities
- High mechanical force challenges connecting 1,000s of pins
- Effective temperature soaking systems
- Device Power and thermal management for 100 - 1,000 devices



Products Driving Panel/Strip Test

- Smartphones/iPads/Laptops
- IoT Devices
- Wearable Sensors
- Microcontrollers
- Automotive Safety / Sensors
- Integrated Data Communication
- Higher Density IC Designs

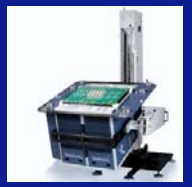


TestConX™

Reliability Testing of Panels and Strips

What Type of Testing is Required?

- ATE solutions for 100-200 simultaneous devices:
  - Simple parametric testing
  - Functional pattern stimulus and capture
  - Analog devices requiring Mixed Signal test
- Solutions for testing 500 – 1,000 devices in parallel
- Devices requiring burn-in, aging and reliability stabilization
  - Automotive products
  - Optical components in handhelds and displays
  - DRAM & Flash (cycling)



TestConX™

Reliability Testing of Panels and Strips

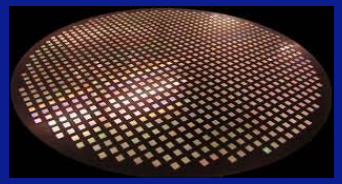
10

Unique Resource Requirements

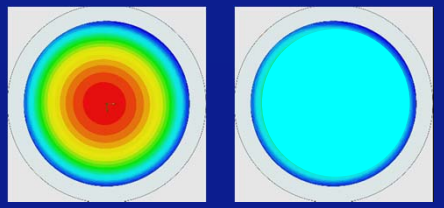
- Modules often contain multiple die technologies
  - Digital logic requires individual DPS and pattern stimulus/capture
  - VCSELs – constant current supplies and optical test
  - Sensors may require special test resources
- Flexibility of universal channel resources
  - S/W programmable as DPS, Functional I/Os, PMUs or Clocks
- High power panels/strips may require up to 2-3 kW

Reliability Stabilization Challenges

- High Number of Resources Required
  - Power supplies (FV & FI) – 100s to 1,000
  - Digital resources - 100s to 1,000+



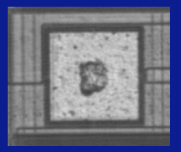
- 1,000s of Precise Probes Required
  - Address alignment and mechanical force requirements
- Power and Thermal Management
  - Supply 100 - 3,000 watts per panel/strip
  - Thermally managing resulting heat energy



Unmanaged Managed

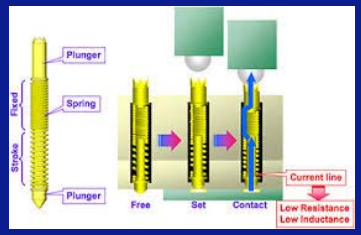
Contactor to Pad Issues

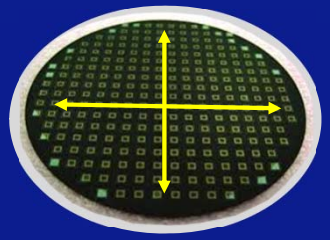
- Package pad size challenges
  - Pad sizes can be < 100 um^2
  - Leverage wafer level contacting techniques
  - May require very small pitch between pads
- CTE effects at stabilization temperature
  - Maintain contact to pads while elevating temperature to >125°C



100 µm pad

Probe mark in 30 µm window

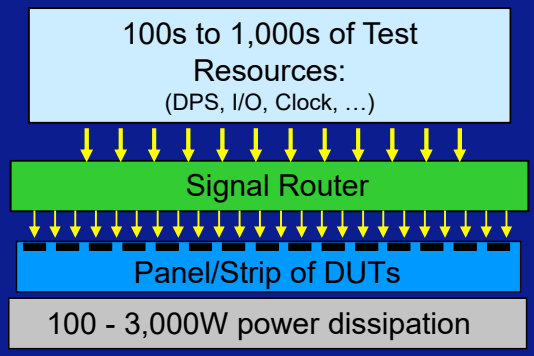


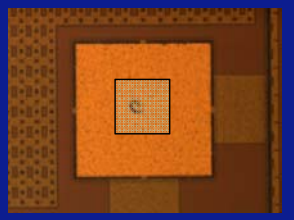


Additional Contacting Issues

Requires these mechanical capabilities:

- Supply contact force to 100s – 1,000s of pads on panel/strip
- Handle various substrate materials and very high compliance requirements (panel bow in mms)
- Maintain contact alignment through temperature cycling (25°C → 125°C → 25°C)
- Accommodate varying sizes of substrates

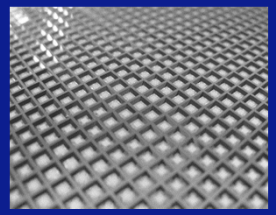


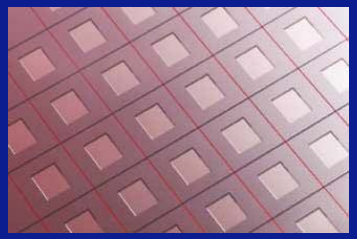


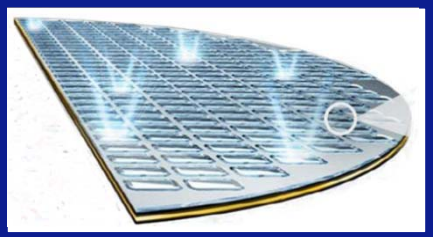
Substrate Challenges

Substrate will typically have an irregular surface:

- Probes must compensate with longer contact pin stroke
- Heating/cooling uniformity across irregular surface
- Substrate may exhibit warpage through temperature steps



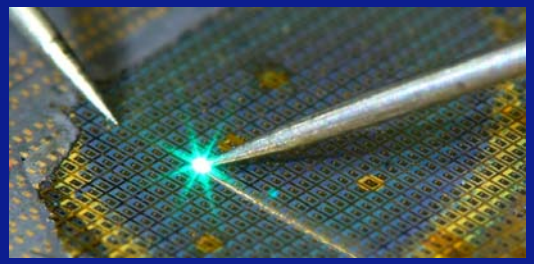


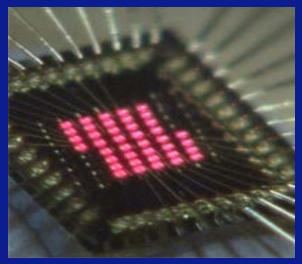


Optical Reliability Stabilization Requirements

Device performance shifts cannot be isolated using traditional electrical testing

- Screen out “infant mortalities”
- Color and power level stabilization – age device to desired performance
- Dark-line defect identification – minimize LED optical variances





TestConX™

Reliability Testing of Panels and Strips

16

So … Is Panel/Strip Reliability Testing Viable?

THE ANSWER IS: YES

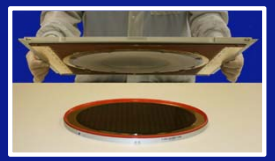
With the following system capabilities:

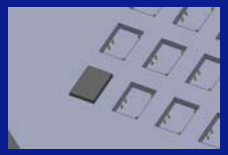
- 1,000s of configurable resources (DPS, Functional I/Os, PMUs & Clocks)
- 1,000s of precise probes to connect to the DUT pads
- Total power available capable of supplying up to 3 kW (if required)
- Ability to manage the resulting heat energy to maintain thermal stability

Panel/Strip Reliability Test Examples

Reusable StripPak™ Contactor

- Supports up to 2,048 Universal Resources per Panel/Strip
- Wafer test technology micro pogo pin contactors – 1,000s per StripPak
- Aehr Test ThinChuck™ thermal chuck (up to 3.5 kW per Panel/Strip)
- Configurable for multiple Panel/Strip types





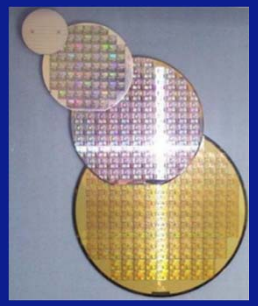
TestConX™

Optical Device Testing at Wafer and Package Level

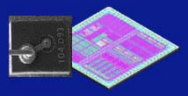
18

2000-2019 20 YEARS ANNIVERSARY

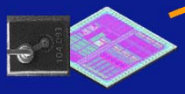
Production Reliability Test Options



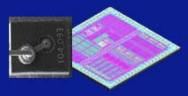
Wafer



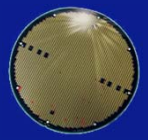
Singulated Die



Singulated Die



Singulated Die

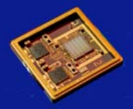


Module "Panel"

Module "Strip"

Single Die Package

Singulated Module



System in Package

System /Product/PCB