# TWENTIETHANNUAI

estConX

#### March 3 - 6, 2019

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Archive

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Session 1B Presentation 3

#### TestConX 2019

On the Bus - Advanced bus protocols for validation



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On the Bus - Advanced bus protocols for validation



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On the Bus - Advanced bus protocols for validation



- An typical I3C network consists of one master and one or more slaves
- SCL I3C Clock
  - Always driven by master
  - Always in push-pull mode
- SDA I3C Data
  - Driven by both master and slave
  - Sometimes open drain, sometimes push-pull

Test**ConX** 





I3C Timing					
SDA		A3 / A2	A1 / A0	RNW	D7 D6
SCL	C1 C2	C3 C4 C5	C6 C7	C8 C9	C <sub>pp</sub> 1
Phase	BUS IDLE START	ADDR==7'b0000101		RNW==0 ACK==0	DATA
Drive		Master		Slave	Master
Туре		Open Drain		/	Push Pull
•	<ul> <li>Each clock phase consists of two e</li> <li>Negedge SCL: Drive SDA</li> <li>Posedge SCL: Sample SDA</li> <li>During the slave driven phases:</li> <li>Master drives SCL</li> <li>Slave drives SDA on negedge SCL_delay</li> <li>Master samples SDA_delay on posedge SCL</li> </ul>	events: SCL C8 SCL C8 SDA SDA SDA SDA SDA	Round trip timing		2019
	Test <b>ConX</b> ®	Coping with I	Drive Sample		5 Revealed to the second







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