# TWENTIETHANNUAI

estConX

#### March 3 - 6, 2019

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Archive

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#### TestConX 2019

On the Bus - Advanced bus protocols for validation

# MIPI Tiny SneakPeek: An Optimized Debug Protocol for efficient Platform Debug

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MIPI Tiny SneakPeek: An Optimized Debug Protocol for efficient Platform Debug



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#### Agenda

- What is MIPI<sup>®</sup> Sneak Peek Protocol (SPP<sup>™</sup>)
- Usage model of MIPI<sup>®</sup> SPP™
- Conclusions and call to action



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#### SneakPeek Protocol: A "Container"



Source: Wikipedia.de Containertransport; CC BY-SA 3.0



Source: Wikimedia 40 foot container double semi truck; CC BY 3.0

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Source: Wikipedia Containerization; CC BY 2.0

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#### SneakPeek Protocol (SPP™) Overview

• Packet based protocol

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- Simple enough to be implemented in dedicated HW modules
- Command/ Response protocol driven by the debug tooling (DTS)
- Focus on system and debug peripheral memory access
- Network latency tolerant for higher throughput while maintaining error feedback through command/ response





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#### **MIPI<sup>®</sup>: SneakPeek**

- No dedicated port needed
- Stability depends on network/ PHY
- Debug solution might be impacted by power states

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#### SPP Command/ Response Opcodes

Commands

(issued by the DTS):

- Pad
- Nop
- InitializeSPEngine
- UnblockSPEngine
- ReadSPConfig
- WriteSPConfig
- ReadSystem
- WriteSystem
- WriteReadSystem
- LoopTrigSystem

Responses (sent by the TS):

- Pad
- Nop
- AckInitalizeSPEngine
- AckUnblockSPEngine
- ReadSPConfigData
- WriteSPConfigResult
- ReadSystemData
- WriteSystemResult
- WriteReadSystemData
- LoopTrigSystemResult











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#### **SneakPeek Protocol (SPP)**

- Pairing Command/Response
- FullSPP can bundle several command/responses into a single SP Transfer Block (SPTB)
  - Optimized for high bandwidth interfaces
- TS does not generate spontaneous traffic

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#### One Size fits all?

- Depending on application, the SPP overhead is significant
  - Minimal header size is 16 Bytes
- The TinySPP flavor was introduced to better cope with low bandwidth I/Fs
  - Minimal header size is 4 Bytes
  - Short addressing capabilities
  - Introduction of actions in commands and events in responses



Source: Wikipedia.de Containertransport; Public Domain





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#### **SneakPeek Protocol Flavors**

Feature	TinySPP	FullSPP		
# of Access Spaces	8 (3-bit field)	32 (5-bit field)		
Sequence Number	<ul> <li>N/A. Additional requirements to network:</li> <li>Messages stay in order</li> <li>Guaranteed Delivery</li> <li>DTS/TS has to do book-keeping</li> </ul>	Present		
Standard Size Field	Chosen by TS	Different option		
Size of Transaction Byte Count (TBC) Field	7 bits	16 bits		
Short Addressing	6-bit address replacement supported. Short addressing is required in TinySPP	N/A		
Packet Alignment	Byte aligned	16-Byte aligned		
Shortest Packet Length	4 Bytes	16 Bytes		
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# TinySPP

- Optimized for low bandwidth interfaces. Primary target is MIPI I3C
- Focus on 32-bit systems
  - Use SP register to go beyond 32-bit
- "Short addressing" to optimize local accesses
- Use:
  - Action and event to reduce latency

Event	Action				
No Event to Report	No Action to be Performed				
Execution State Changed to Start	Change Execution State to Start				
Execution State Changed to Stop	Change Execution State to Stop				
Trace Activity Changed (Start/ Stop)	Change Trace Activity (Start/ Stop)				
Reset Occurred	Reset				
Trigger	Trigger				
Trace Attention Needed	Reserved				
Communication (RX) Data Ready	Communication (TX) Data Ready				
Vendor defined Event 1	Vendor defined Action 1				
Vendor defined Event 2	Vendor defined Action 2				

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	E	xample: SPP	Data For	mat			
	TinySPP           31         30         29         28           Addr[7:2] o         0	27     26     25     24     23     22     21     20     19     18     17     16       r Res     SPCONF_ADDR S     Transaction Byte Count or Reserved     Transaction Byte Count or Reserved	15         14         13         12         11         10         9         8         7           Action         LCP         SRI         COF         AccessSpace or Rsvd         or Rsvd	7 6 5 4 Opcode	3 2 1 0 Version		
	LCP I SRI S COF ( S I FullSPP	ast Command Packet Send Response Immediately Continue on Fault Jse Short Address	ý Sizo or Bayd Associacione or Bayd	Oracda	Varias		
	LCP SRI COF Ac	tion Reserved	Transaction Byte Cou	int or Reserved	d		
AddressLow or SignatureLow or Reserved AddressHigh or SignatureHigh or Reserved							
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#### Conclusions

- MIPI Sneak Peek Protocol provides a scalable debug/ test solution
  - Meets the high and low bandwidth link requirements
  - Can be implemented in Software or Hardware
  - Reusable solution across different product segments





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#### **Call to Action**

- Adopt and implement the flexible MIPI Debug Solution
- Join the MIPI Debug WG
  - Currently participants are SoC, IP, Tools vendors
  - Requires MIPI Contributor membership
  - Telcos every other Tuesday at 9am pacific time
    - 90-120 minutes depending on the agenda
  - Three F2F sessions with all MIPI WGs
    - Generally meet for 4 days



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#### **Further Information**

- MIPI Debug WG Public Page
- MIPI Architecture Overview for Debug
- MIPI Debug on Wikipedia



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