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Advanced Packaging Innovation Challenges

- Super-thin Optical SiP & CIS

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A-Kelon (Huizhou) Optronics

Suzhou ▪ October 23, 2018

Contents

- Main Trend of IC Packaging Innovation
- Development on Super-thin Optical SiP (SOSiP)
- Development on Super-thin CSP (SCSP)

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Main Trend of IC Packaging Innovation

Driving Force for IC Packaging Innovation

NEXT-GENERATION SEMICONDUCTOR FABRICATION TECHNOLOGIES

45nm 2007
32nm 2009
22nm 2011
14nm 2013
10nm 2015
7nm 2017
Beyond 2020

MANUFACTURING
DEVELOPMENT
RESEARCH

Carbon Nanotube ~1nm diameter
QW III-V Device
Nanowire 10 atoms across
Graphene 1 atom thick
Not to scale

Source: Intel

Driving Force for IC Packaging Innovation (Cont'd)

Performance

Wafer Technology

Fine pitch Solution

Thin Package

10/7nm Tech.

14 nm Tech.

16 nm Tech.

20 nm Tech.

Fine Cu Pillar/ Plated SnCu

Sn Cu

Cu Pillar, Sn/Ag/Cu, Sn/Ag, EU

0.8/0.65 mm

0.6 mm

0.5 mm

0.45 mm

Solder Bump 150 um

Cu Pillar A:110um P:60um

Solder bump 130 um

Cu Pillar 65um w/1 line 80um w/ 2line

Cu Pillar 55-60um W/ 2 line escape

Production

Available

2016~2018

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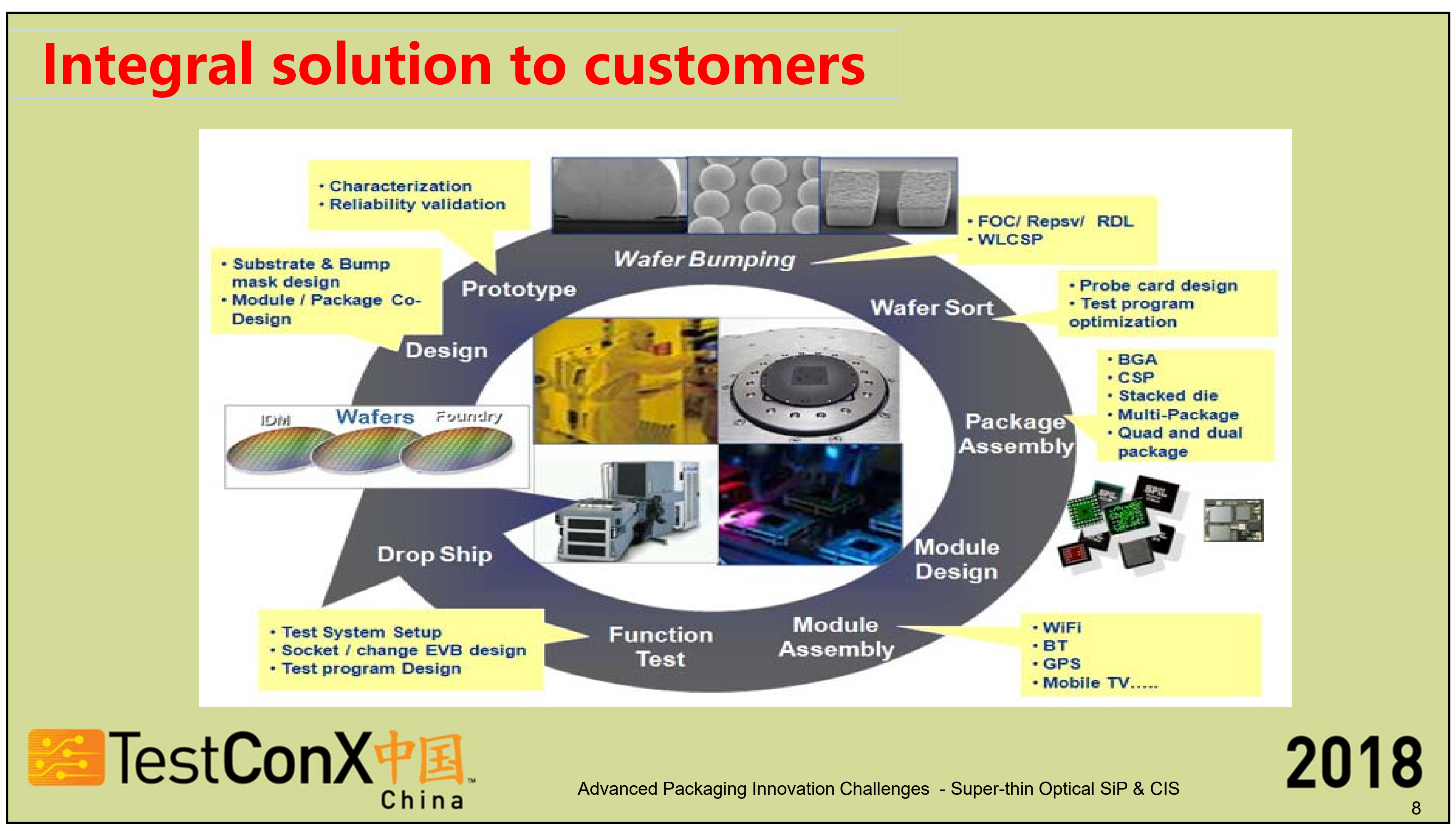
Integral solution to customers
• Characterization
• Reliability validation
• Substrate & Bump mask design
• Module / Package Co-Design
Prototype
Design
Wafer Bumping
• FOC/ Repsv/ RDL
• WLCSP
Wafer Sort
• Probe card design
• Test program optimization
Package Assembly
• BGA
• CSP
• Stacked die
• Multi-Package
• Quad and dual package
Wafers
IDM
Foundry
Module Design
Drop Ship
Function Test
Module Assembly
• Test System Setup
• Socket / change EVB design
• Test program Design
• WiFi
• BT
• GPS
• Mobile TV.....
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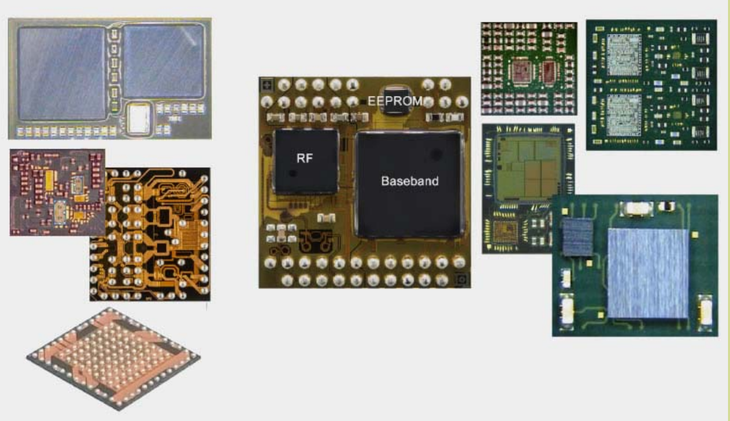
Main Trend of Advanced IC Packaging

- SiP (System in Packaging)
- FOWLP (Fan-out Wafer-level Packaging)
- FOPLP (Fan-out Panel-level Packaging)

What is SiP?



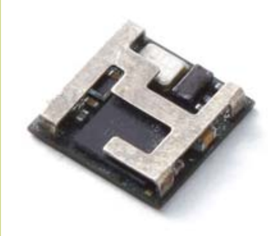
A combination of one or more IC devices plus optionally passive components that define a certain functional block within a quasi-package mounted onto PCB.

Advantages:

- Thinner / smaller form factor than individually packaged components
- Increased performance and functional integration
- Design flexibilities
- Better electromagnetic interference (EMI) isolation
- Reduced system board space and complexity
- Improved power management and more room for battery
- Simplified SMT assembly process
- Cost effective “plug-and-play” solutions
- Faster time-to-market (TTM)
- One stop turnkey solution - Wafer to fully tested SiP modules

Example of SiP Module from ASE

Antenna on Package (AoP)



To minimize the antenna size at the package level offering the smallest antenna & highly integrated RF SiP module.

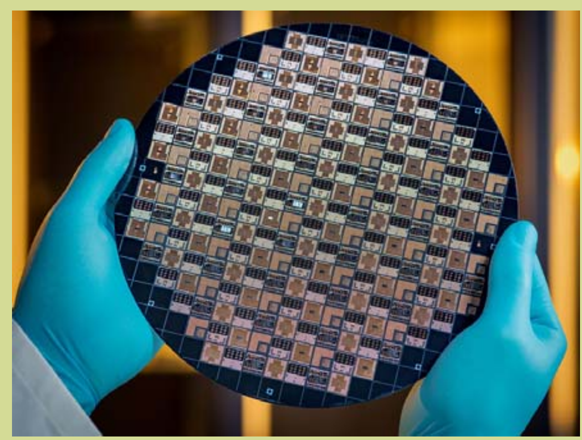
Feature:

Good radiation performance with the low insertion loss and good impedance matching between the RF SiP and the antenna.

Capabilities:

- Min. package size: 4.9mm x 3.3mm (achieved at 2.4GHz)
- Film step coverage: >30%
- Min. line/space on top: 250µm
- Dimension tolerance on side wall: within +/-35um

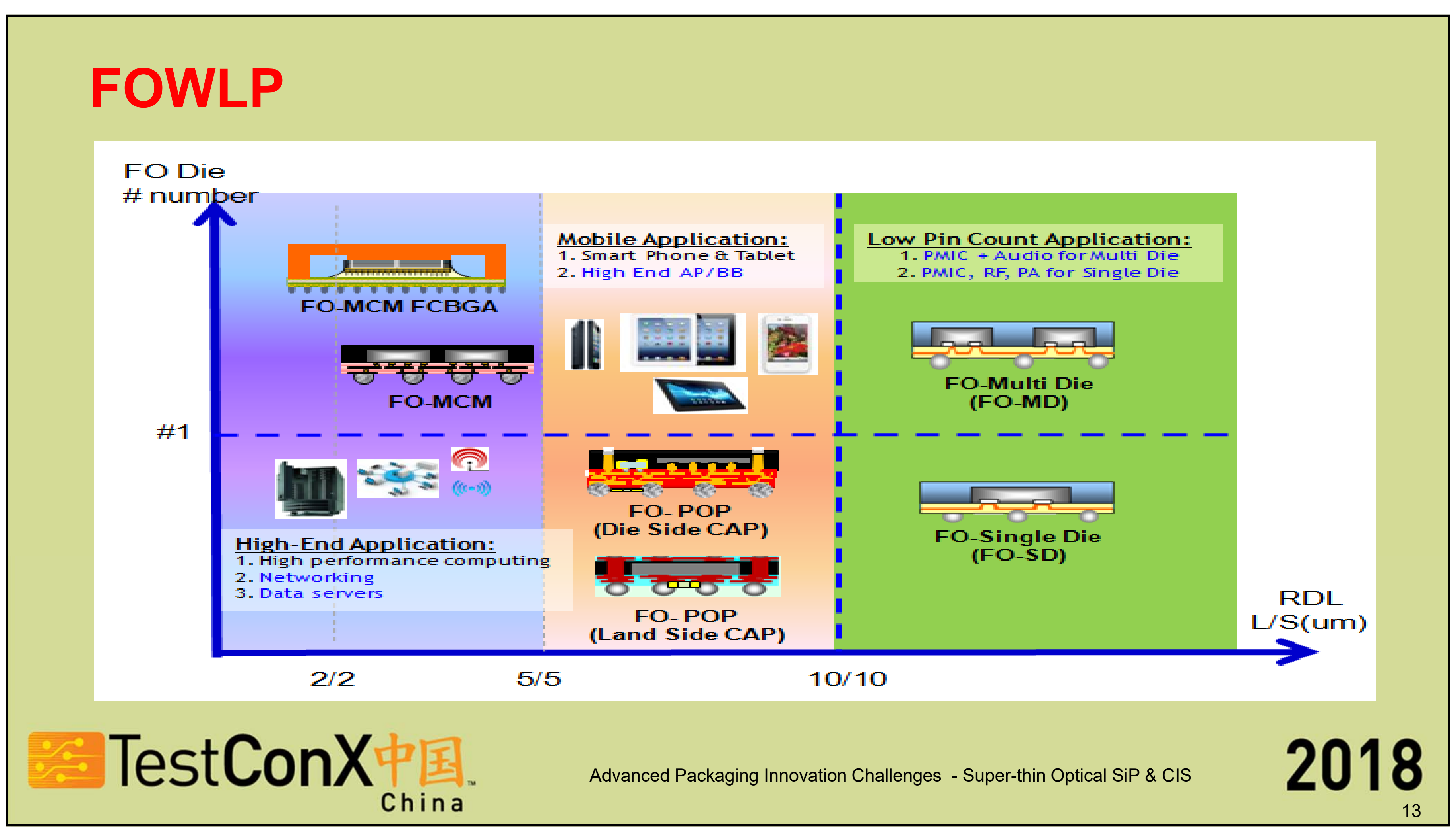
What is FOWLP?



Reconfigured molded wafer combined with a thin film redistribution layer to yield an SMD-compatible package.

Advantages:

- Substrate-less package
- Low thermal resistance
- Improved RF performance due to shorter interconnects together with direct IC connection by thin film metallization
- Embedded passives (R, L, C) as well as antenna structures using a multi-layer structure.
- Lower cost larger mold embedding form factors


FOWLP
FO Die
number
#1
FO-MCM FCBGA
FO-MCM
High-End Application:
1. High performance computing
2. Networking
3. Data servers
Mobile Application:
1. Smart Phone & Tablet
2. High End AP/BB
FO- POP
(Die Side CAP)
FO- POP
(Land Side CAP)
Low Pin Count Application:
1. PMIC + Audio for Multi Die
2. PMIC, RF, PA for Single Die
FO-Multi Die
(FO-MD)
FO-Single Die
(FO-SD)
RDL
L/S(um)
2/2
5/5
10/10
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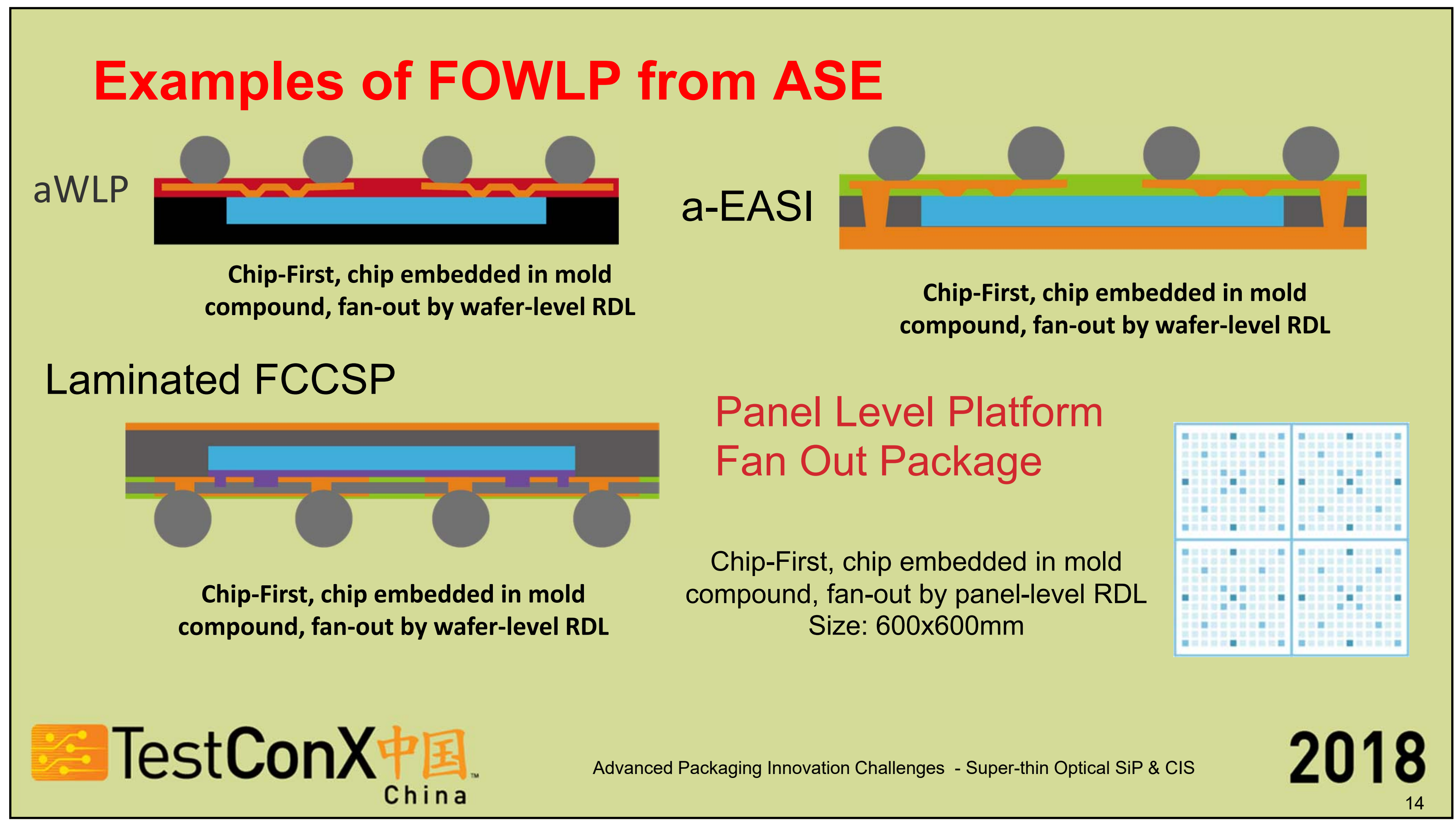
Examples of FOWLP from ASE
aWLP
Chip-First, chip embedded in mold compound, fan-out by wafer-level RDL
a-EASI
Chip-First, chip embedded in mold compound, fan-out by wafer-level RDL
Laminated FCCSP
Chip-First, chip embedded in mold compound, fan-out by wafer-level RDL
Panel Level Platform
Fan Out Package
Chip-First, chip embedded in mold compound, fan-out by panel-level RDL
Size: 600x600mm
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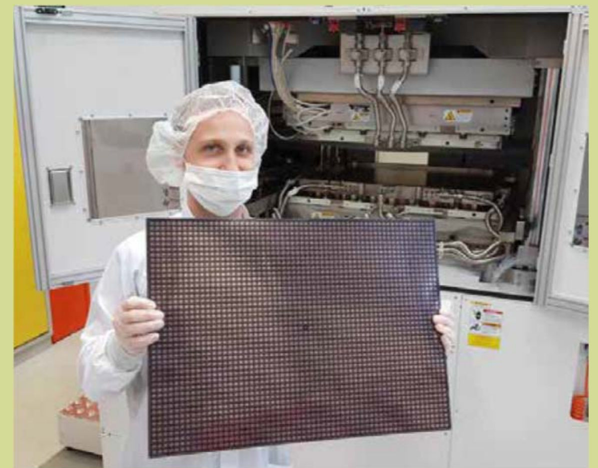
What is FOPLP?



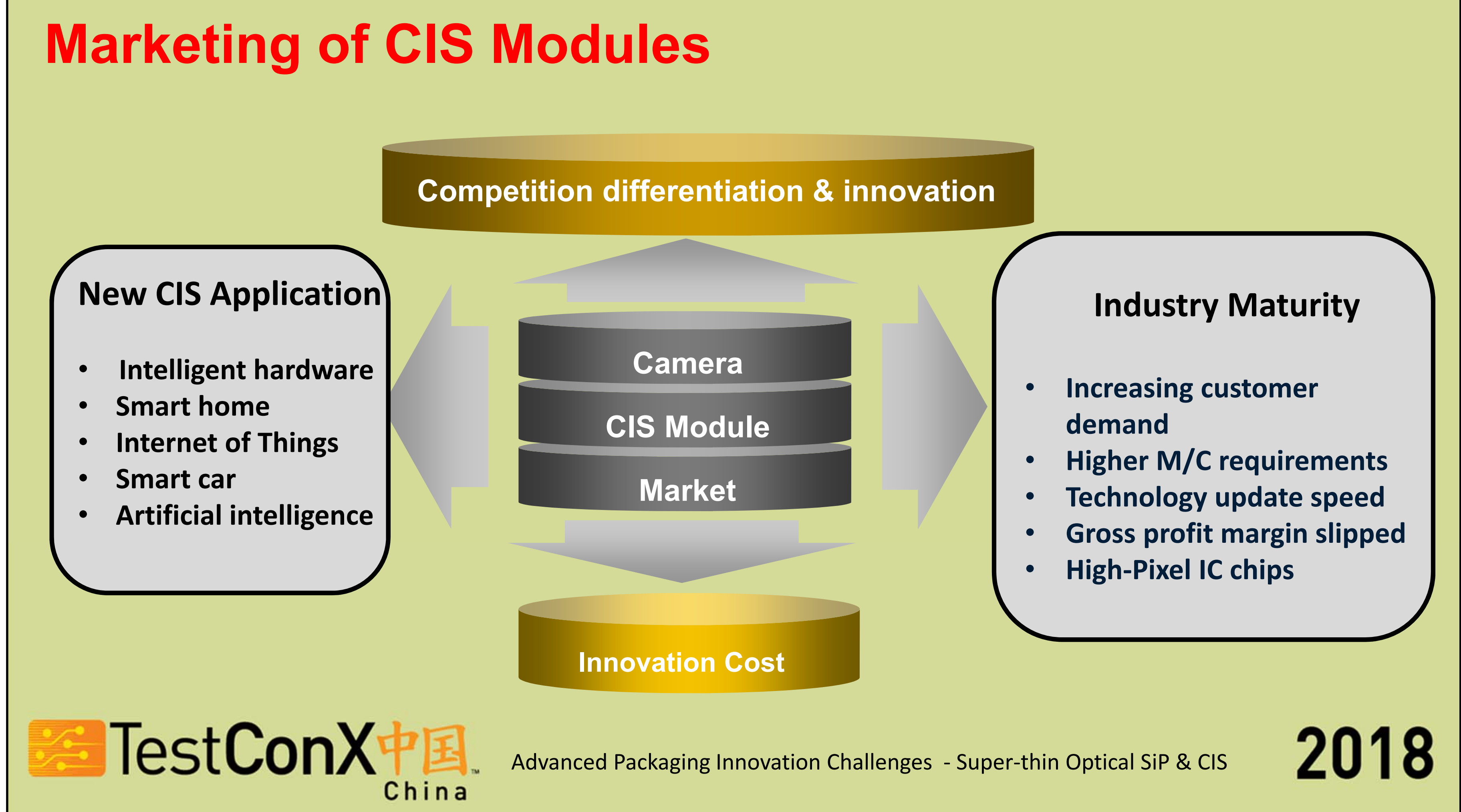
Large area mold embedding technologies and embedding of active components into printed circuit boards (Chip-in-Polymer)

Advantages:

- ❑ Electrical Performance
- ❑ Improved wiring and I / O
- ❑ Standardization for embedding die package
- ❑ Definition of supply chain
- ❑ Thermo-mechanical reliability
- ❑ Lower Cost due to large panel size
- ❑ High throughput
- ❑ High volume production

Development on

Super-thin Optical SiP (SOSiP)


Marketing of CIS Modules
Competition differentiation & innovation
New CIS Application
• Intelligent hardware
• Smart home
• Internet of Things
• Smart car
• Artificial intelligence
Camera
CIS Module
Market
Innovation Cost
Industry Maturity
• Increasing customer demand
• Higher M/C requirements
• Technology update speed
• Gross profit margin slipped
• High-Pixel IC chips
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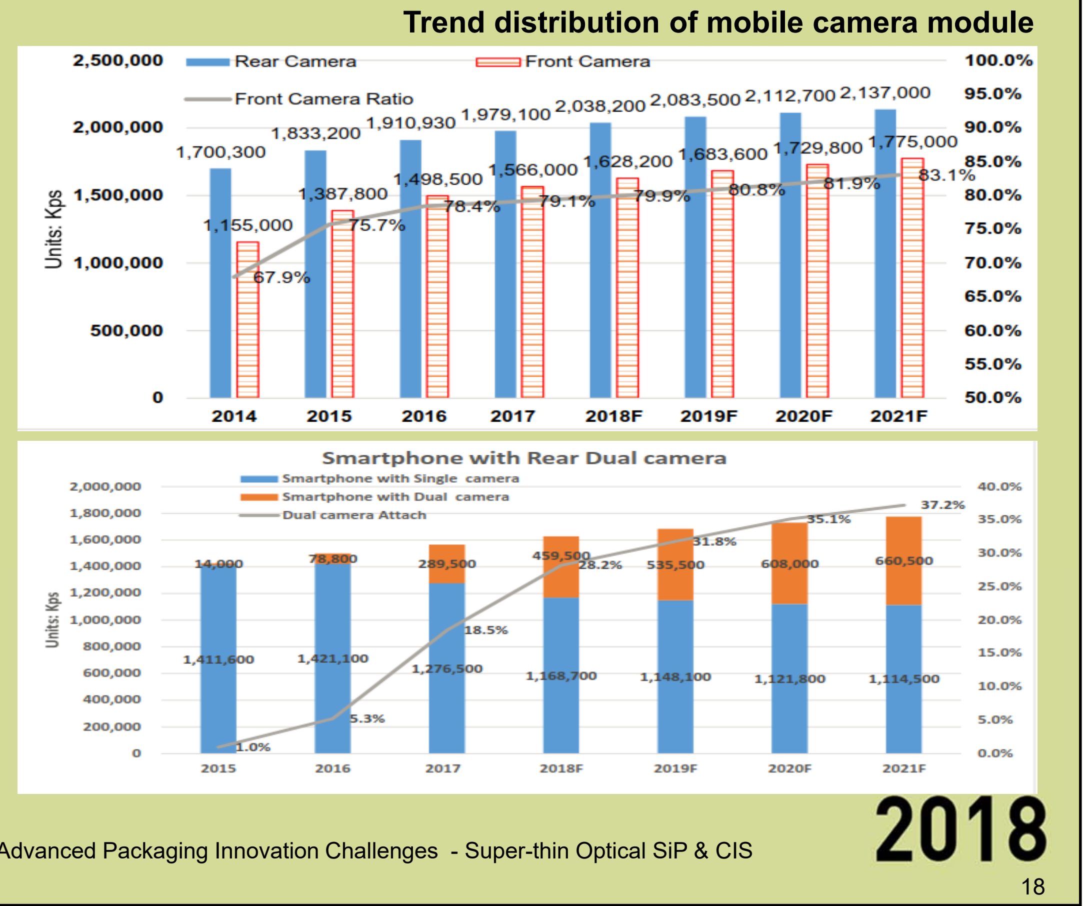
Marketing of CIS Modules (Cont’d)

CIS module market prospects in China

- 2017 market size reached 3.545 billion.
- 2018-2020, smartphones and tablet cameras will grow steadily, while applications such as in-vehicle cameras, smart homes and wearable devices will become new growth points.
- The smart device camera module market will maintain rapid growth, and shipments are expected to reach 4 billion in 2021.

Trend distribution of mobile camera module



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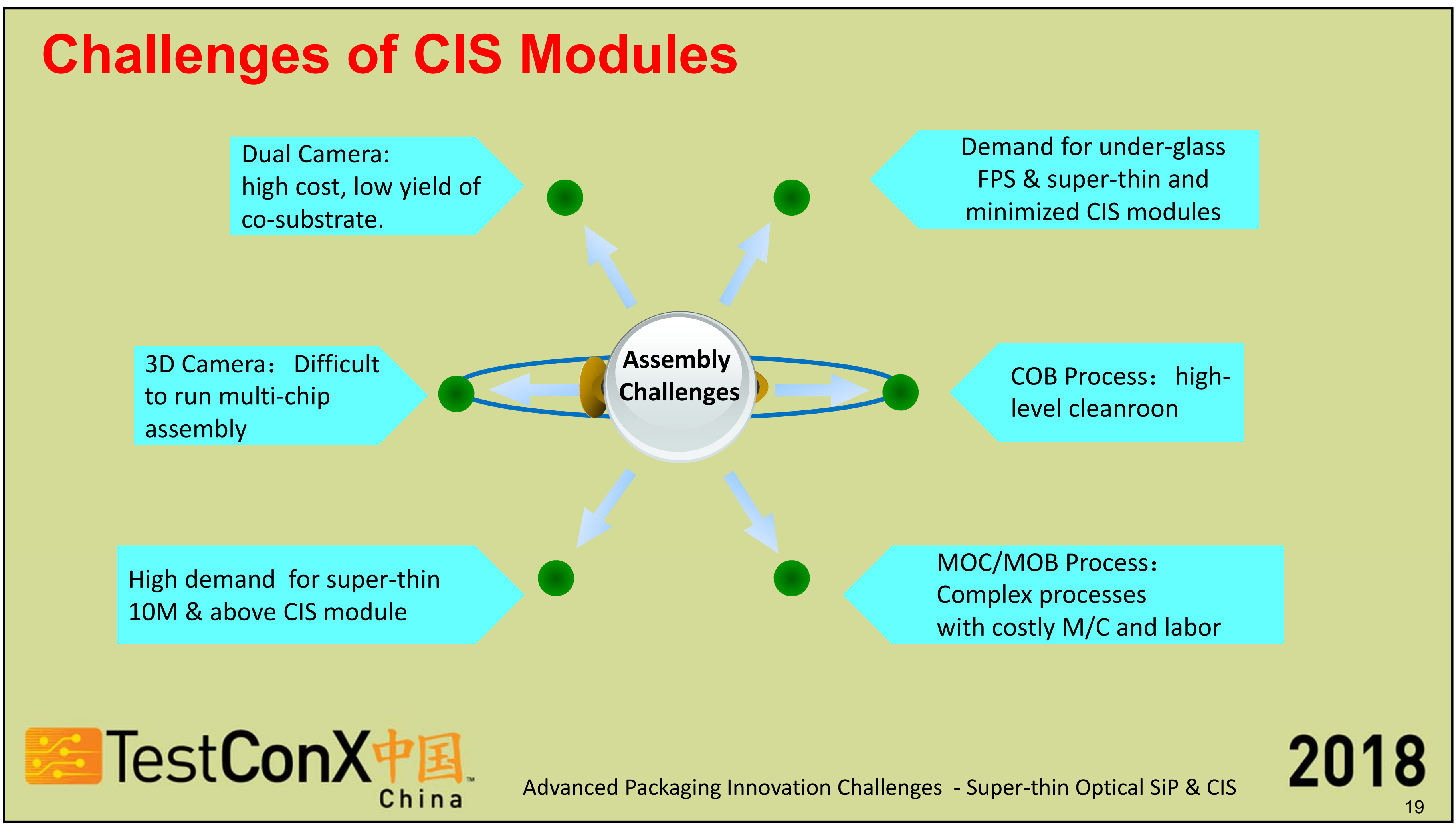
Challenges of CIS Modules
Dual Camera:
high cost, low yield of
co-substrate.
Demand for under-glass
FPS & super-thin and
minimized CIS modules
3D Camera： Difficult
to run multi-chip
assembly
Assembly
Challenges
COB Process： high-
level cleanroon
High demand for super-thin
10M & above CIS module
MOC/MOB Process：
Complex processes
with costly M/C and labor
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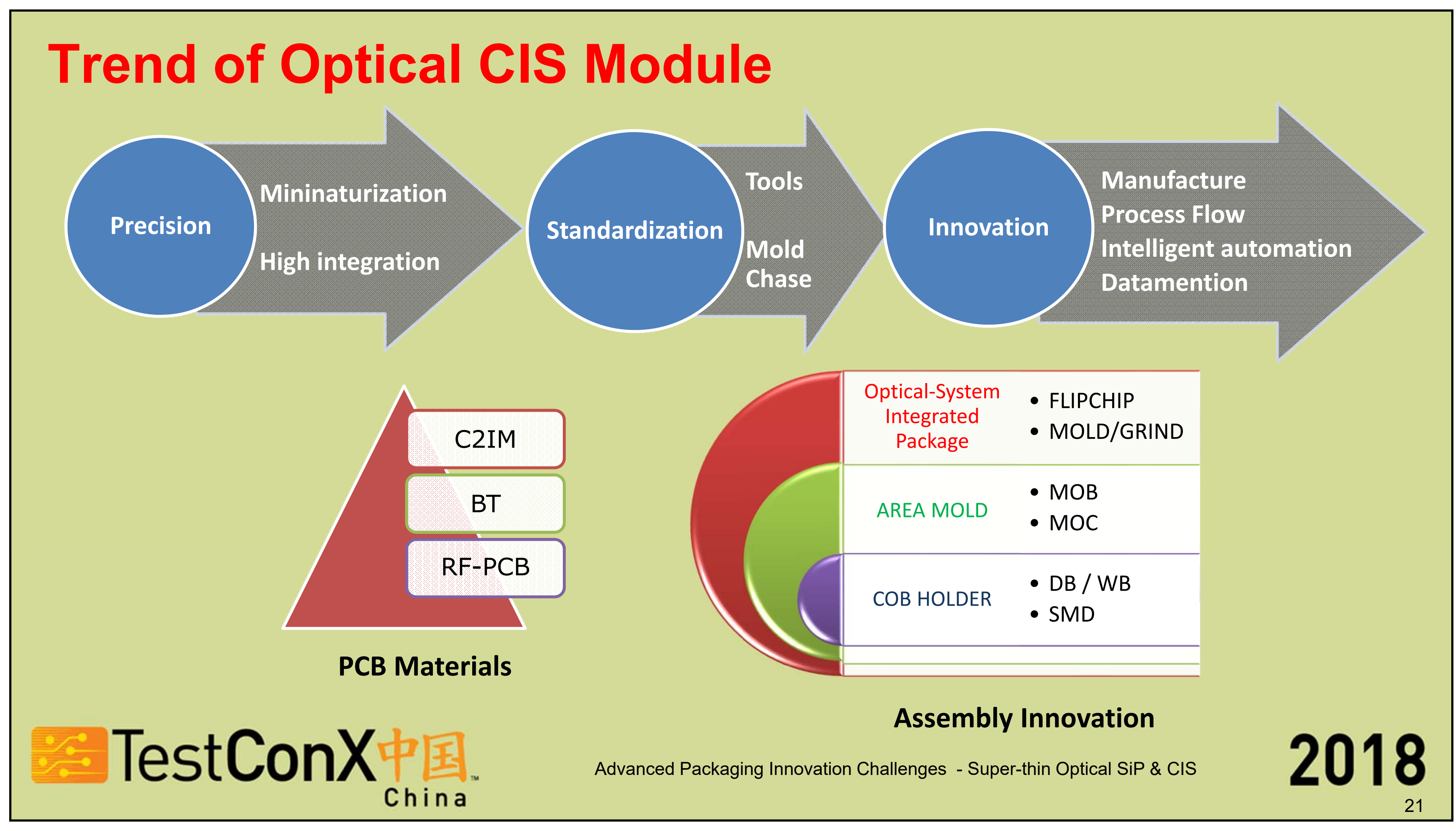
Applications of CIS Modules

Smart home area

Intelligent vehicle field


Trend of Optical CIS Module
Precision
Mininaturization
High integration
Standardization
Tools
Mold Chase
Innovation
Manufacture
Process Flow
Intelligent automation
Datamention
C2IM
BT
RF-PCB
PCB Materials
Optical-System Integrated Package
• FLIPCHIP
• MOLD/GRIND
AREA MOLD
• MOB
• MOC
COB HOLDER
• DB / WB
• SMD
Assembly Innovation
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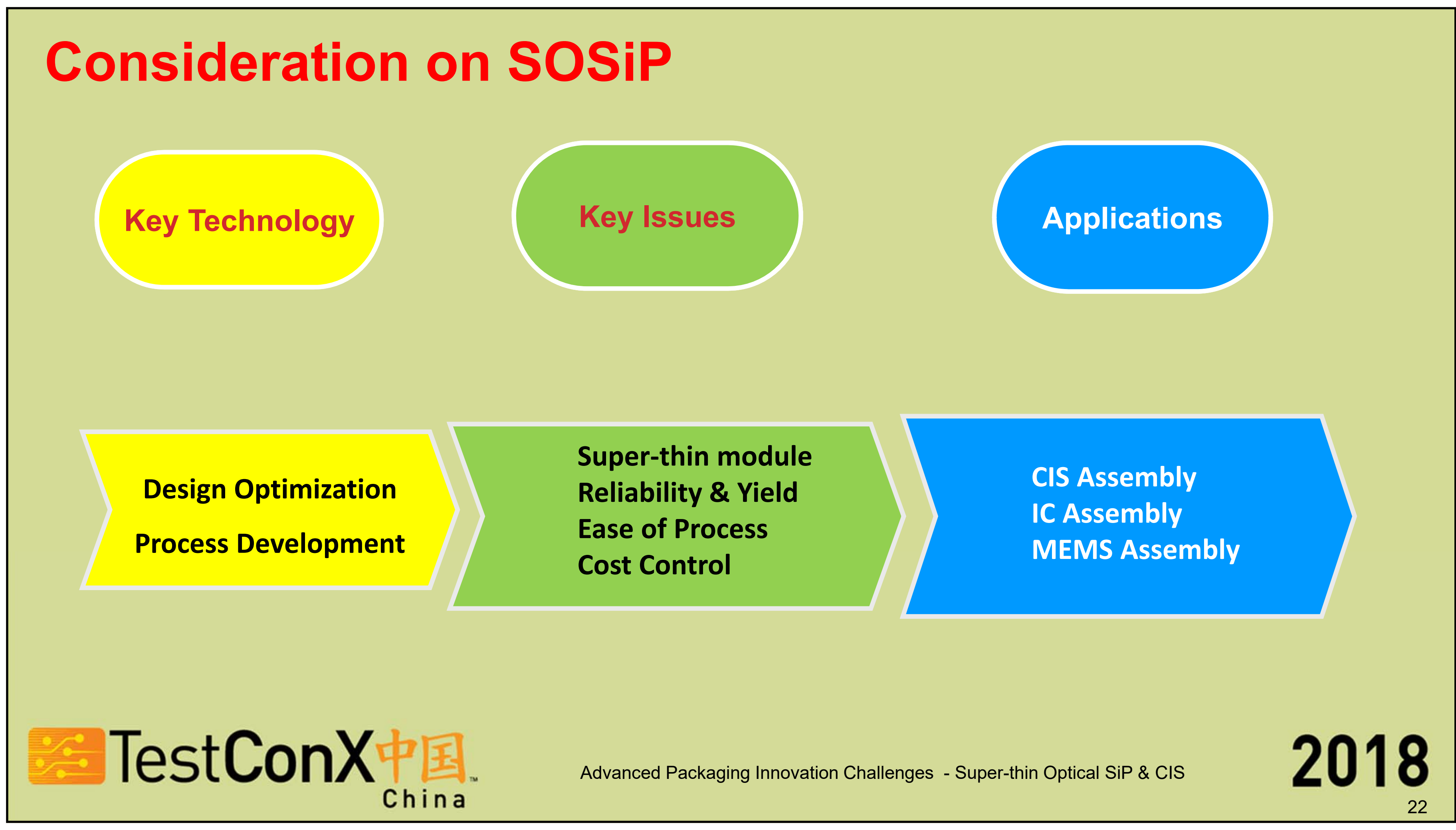
Consideration on SOSiP
Key Technology
Key Issues
Applications
Design Optimization
Process Development
Super-thin module
Reliability & Yield
Ease of Process
Cost Control
CIS Assembly
IC Assembly
MEMS Assembly
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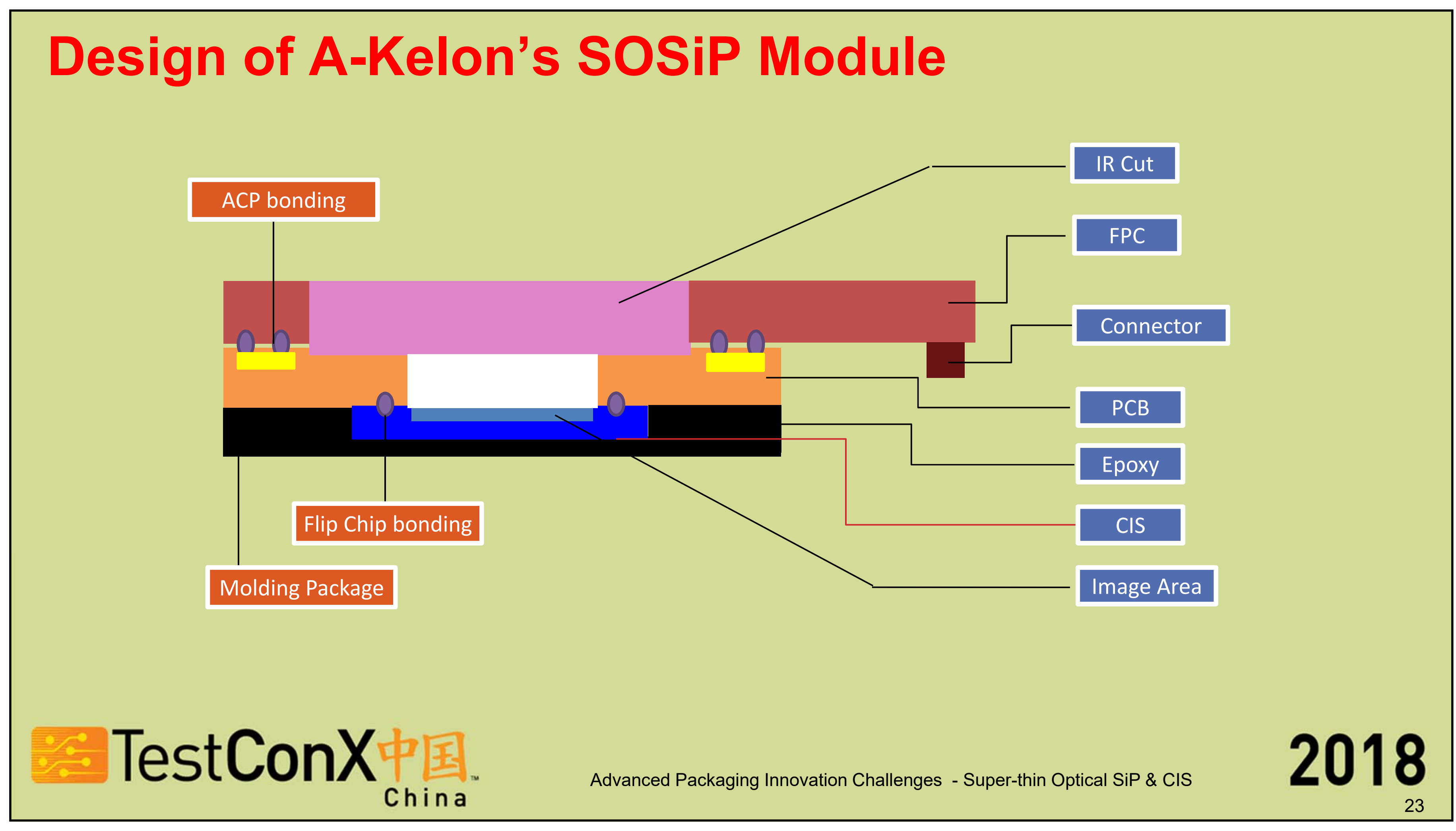
Design of A-Kelon's SOSiP Module
ACP bonding
IR Cut
FPC
Connector
PCB
Epoxy
CIS
Image Area
Flip Chip bonding
Molding Package
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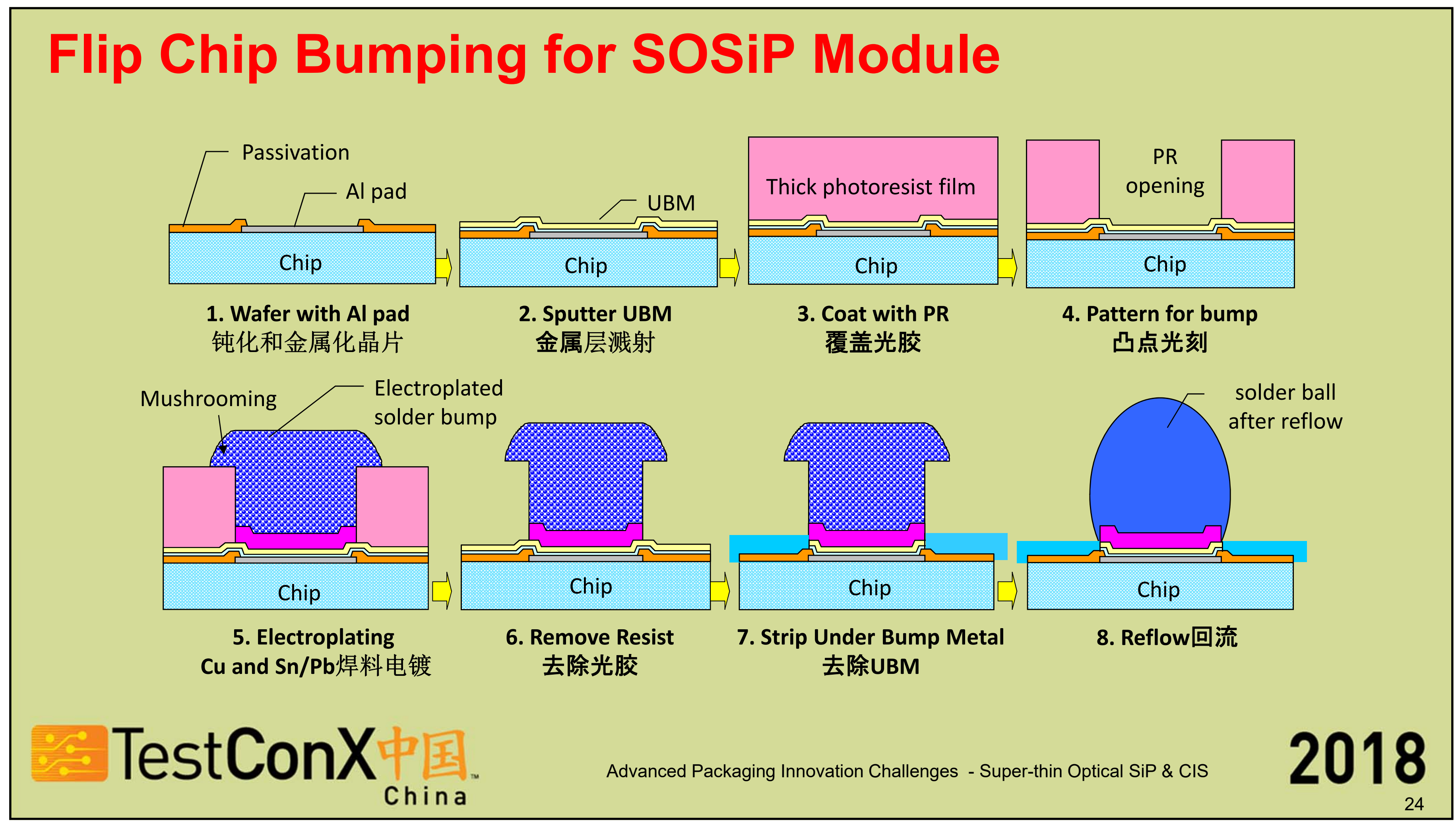
Flip Chip Bumping for SOSiP Module
Passivation
Al pad
Chip
UBM
Chip
Thick photoresist film
Chip
PR opening
Chip
1. Wafer with Al pad
钝化和金属化晶片
2. Sputter UBM
金属层溅射
3. Coat with PR
覆盖光胶
4. Pattern for bump
凸点光刻
Mushrooming
Electroplated solder bump
solder ball after reflow
Chip
Chip
Chip
Chip
5. Electroplating
Cu and Sn/Pb焊料电镀
6. Remove Resist
去除光胶
7. Strip Under Bump Metal
去除UBM
8. Reflow回流
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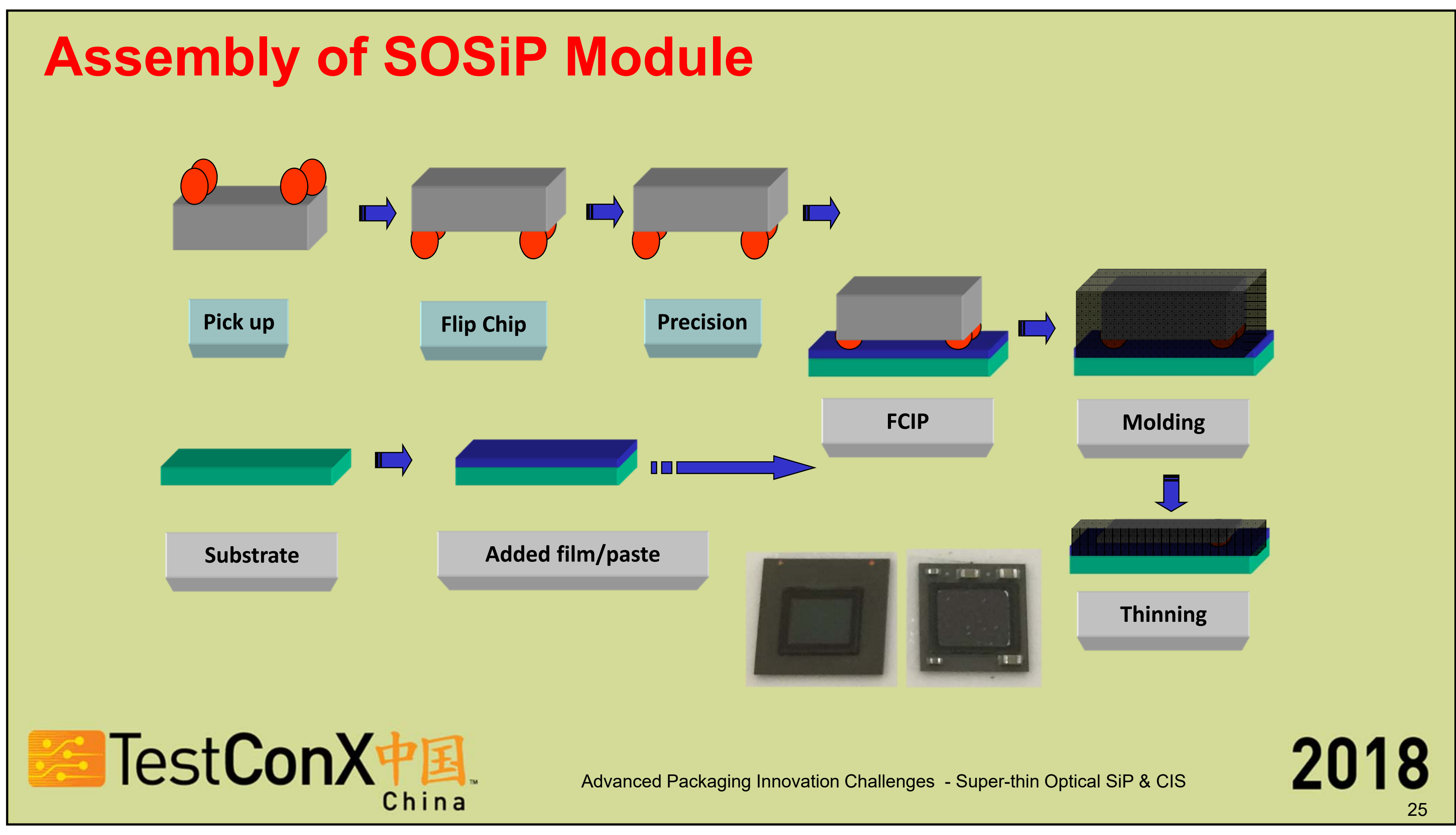
Assembly of SOSiP Module
Pick up
Flip Chip
Precision
FCIP
Molding
Substrate
Added film/paste
Thinning
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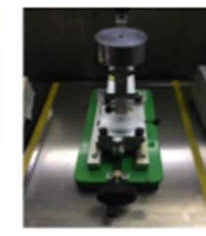
Reliability Tester

- 可靠性检测设备

2次元测试仪

耐摩擦测试 铅笔硬度测试 按压测试



落球冲击 盐雾测试 RCA纸带耐磨测试 水滴角测试 FPC软性弯折测试 水煮测试

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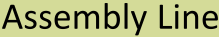
Assembly Equipment

Overview of Cleanroom

Curing System

Bonder


Assembly Line

Cleaning System

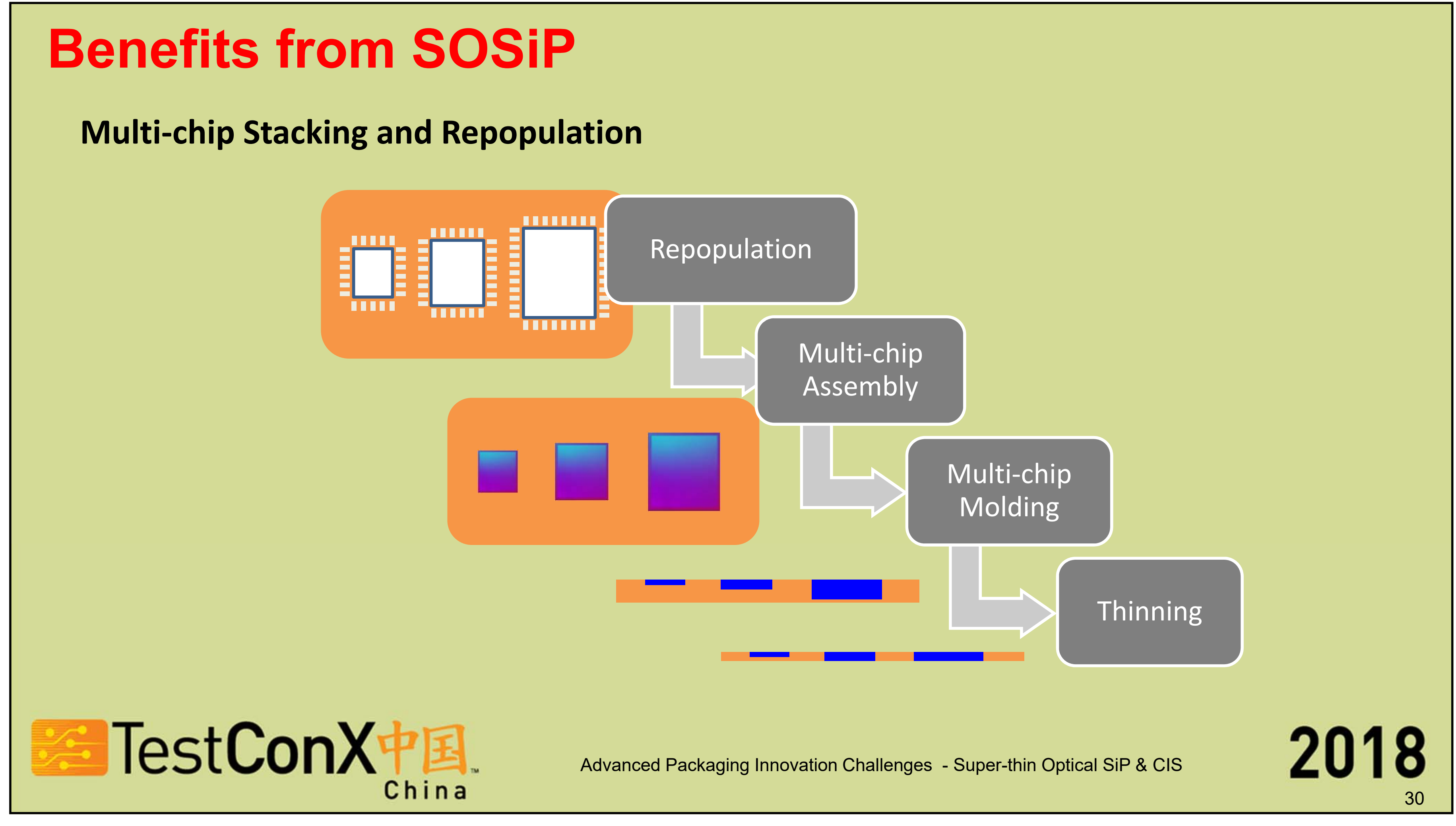
Filter Assembly M/C

Tester

Comparison between SOSiP & Existing Packages

Item	1st Generation	2nd Generation				3rd Generation
Process	COB	MOB	MOC	MONC	F/C	SOSiP
Assembly Methods						
Structure						
Area	100%	88%	77%	82%	85%	55~65%
Thickness	1.0~1.2	0.8~1.0	0.8~0.75	0.8~1.0	0.65	0.3~0.5
Cost	Very High	High	High	High	Expensive	Low
Process Flow	Complex	Long steps	Long steps	Long steps	Long steps	Simplified
Representative enterprise	ALL	SUNNY GROUP Q-Tech	SUNNY GROUP Q-Tech	SUNNY GROUP	APPLE	A-Kelon

Advantages of SOSiP: miniaturization, ultra-thin, simple process, low cost.


Benefits from SOSiP
Multi-chip Stacking and Repopulation
Repopulation
Multi-chip Assembly
Multi-chip Molding
Thinning
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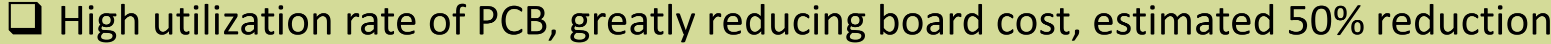
Competitive advantages of SOSiP

- ❑ Enhancement of Multi-chip design ability.
- ❑ Breaking the limitation of image chip thickness
- ❑ Simplification of the process and thus reduction of cost



- ❑ High utilization rate of PCB, greatly reducing board cost, estimated 50% reduction
- ❑ Easy to achieve buried components, reducing the material cost.
- ❑ High reliability and innovative modular manufacturing process, expanding modular commercialization application in mobile phone, industry security vehicle, medical devices and space vision.

Development on Super-thin CSP (SCSP)

What is SCSP?

❖ **Objective of Study:**

I. To develop super-thin CIS module by reducing 0.4mm in height

II. To materialize Cu-Pillar & Flip-chip Bonding

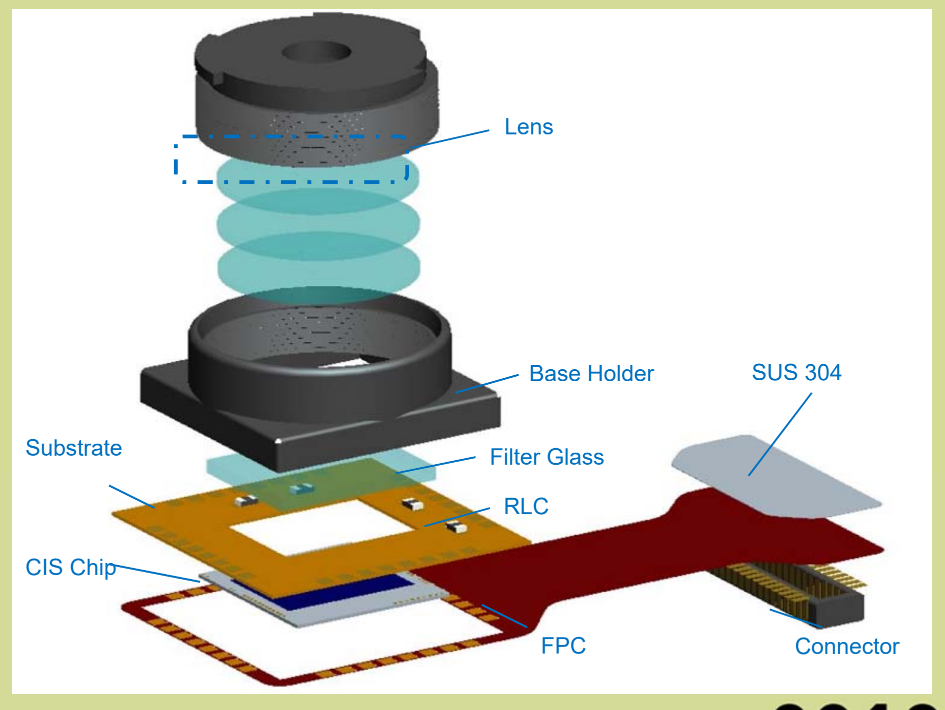
❖ **Challenges of Process:**

I. Protection of CIS Chip

II. Flip-Chip bonding

III. Underfilling Control

❖ **Structure of SCSP module**



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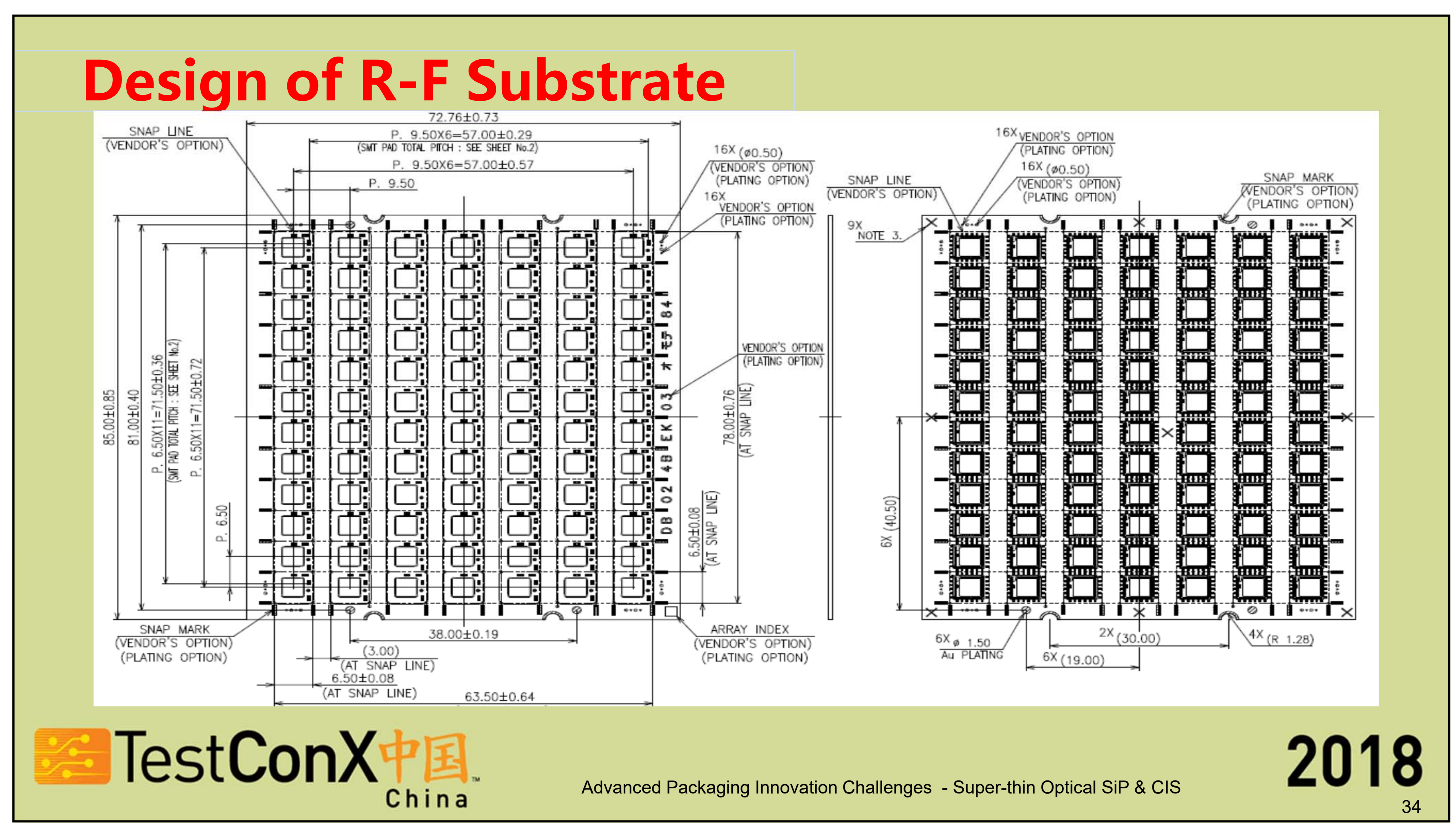

Design of R-F Substrate
72.76±0.73
SNAP LINE (VENDOR'S OPTION)
P. 9.50X6=57.00±0.29
(SMT PAD TOTAL PITCH : SEE SHEET No.2)
P. 9.50X6=57.00±0.57
P. 9.50
16X (ø0.50) (VENDOR'S OPTION) (PLATING OPTION)
16X VENDOR'S OPTION (PLATING OPTION)
VENDOR'S OPTION (PLATING OPTION)
SNAP MARK (VENDOR'S OPTION) (PLATING OPTION)
ARRAY INDEX (VENDOR'S OPTION) (PLATING OPTION)
38.00±0.19
(3.00) (AT SNAP LINE)
6.50±0.08 (AT SNAP LINE)
63.50±0.64
85.00±0.85
81.00±0.40
P. 6.50X11=71.50±0.36
P. 6.50X11=71.50±0.72
P. 6.50
78.00±0.76 (AT SNAP LINE)
6.50±0.08 (AT SNAP LINE)
9X NOTE 3.
6X (40.50)
6X ø 1.50 Au PLATING
2X (30.00)
6X (19.00)
4X (R 1.28)
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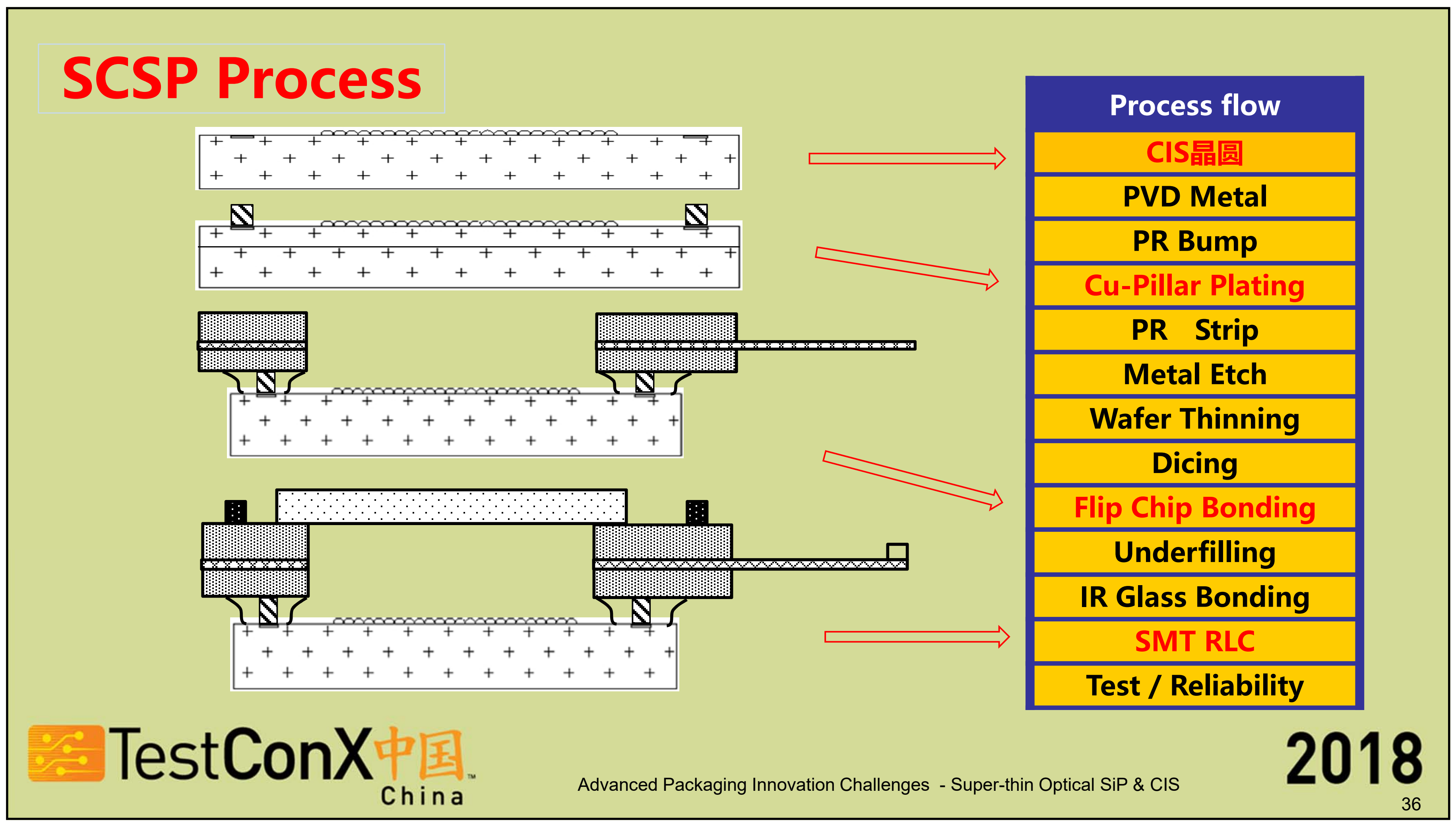
SCSP Process
Process flow
CIS晶圆
PVD Metal
PR Bump
Cu-Pillar Plating
PR Strip
Metal Etch
Wafer Thinning
Dicing
Flip Chip Bonding
Underfilling
IR Glass Bonding
SMT RLC
Test / Reliability
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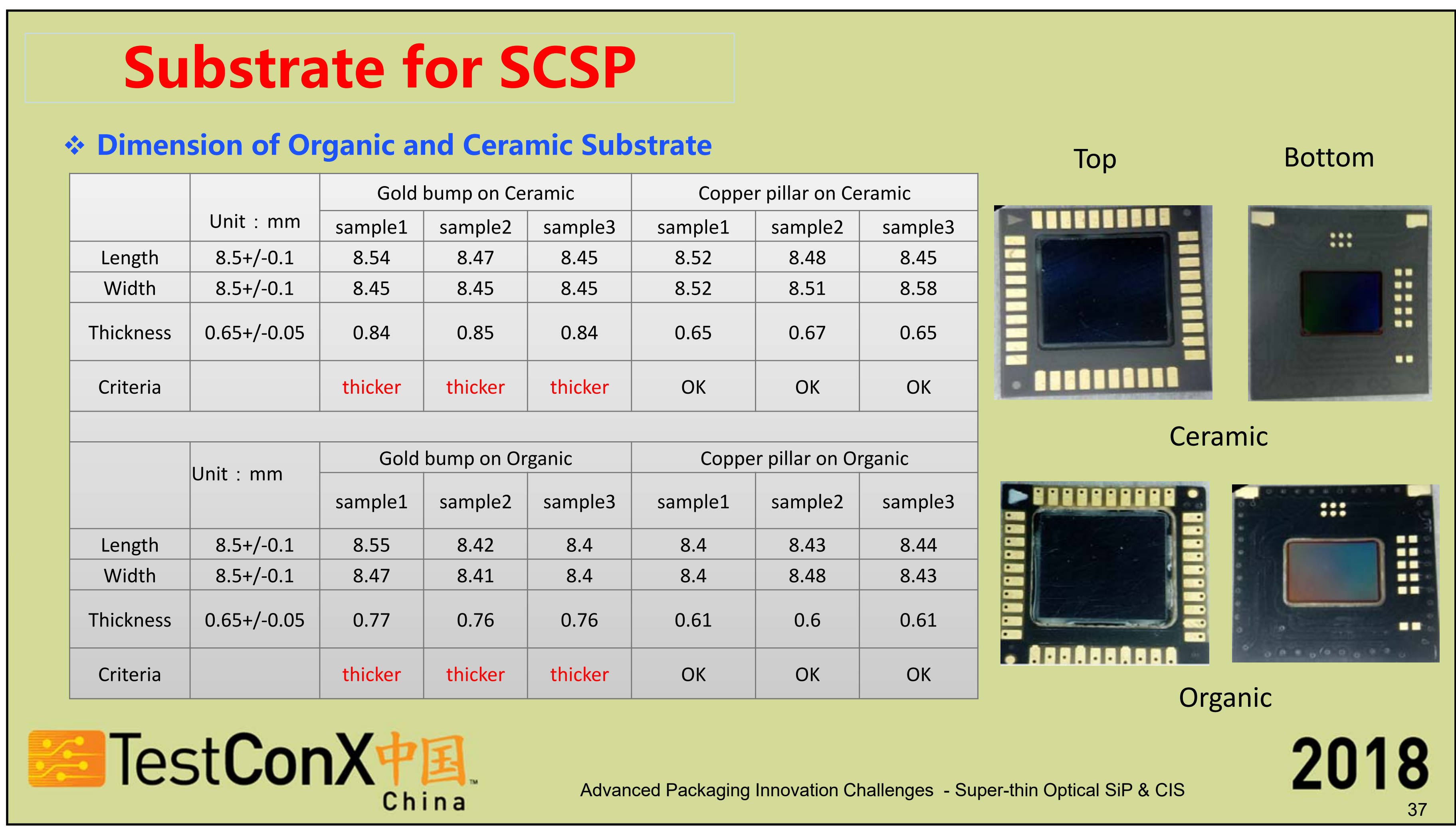
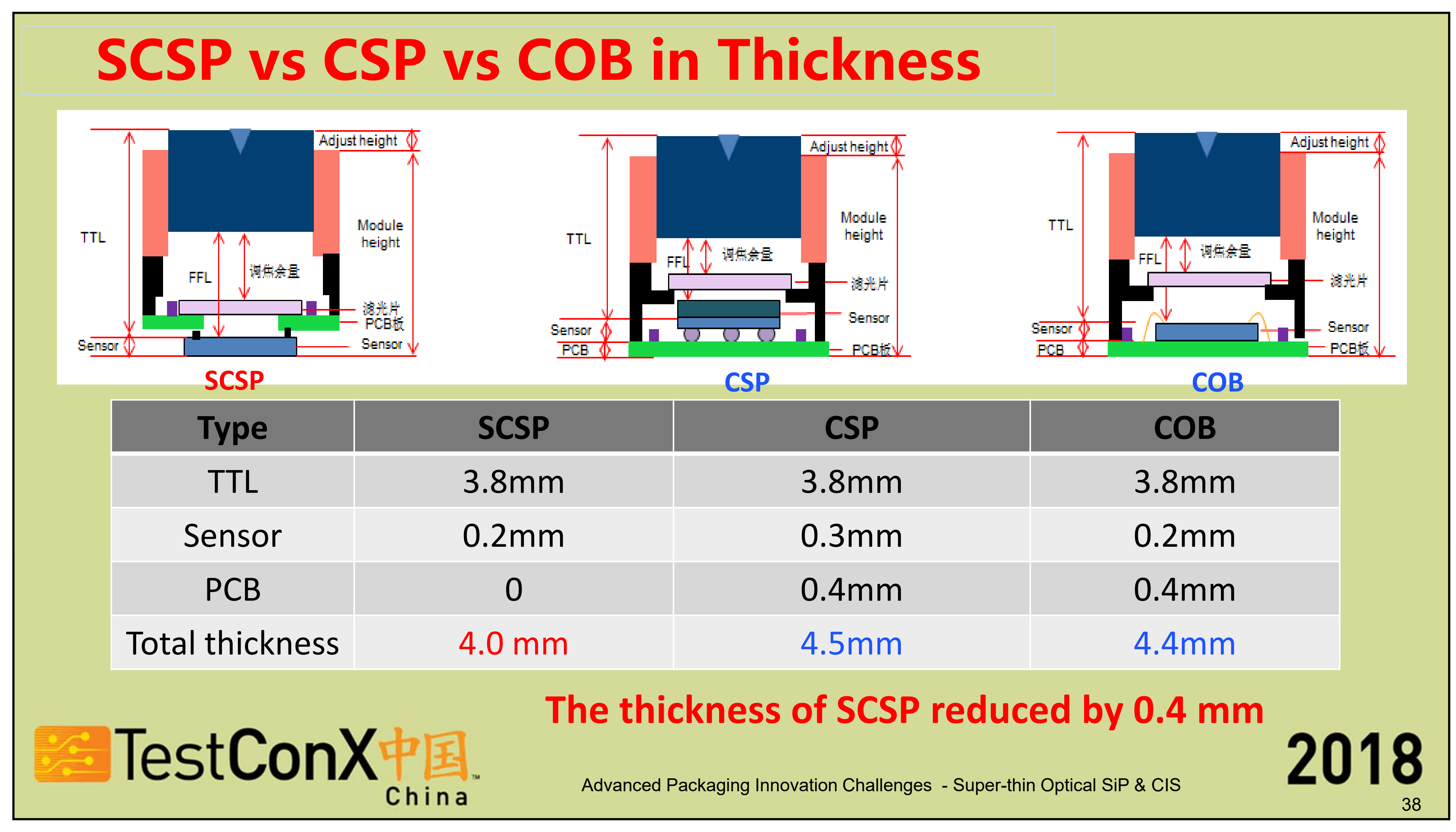


	Unit : mm	Gold bump on Ceramic			Copper pillar on Ceramic		
		sample1	sample2	sample3	sample1	sample2	sample3
Length	8.5+/-0.1	8.54	8.47	8.45	8.52	8.48	8.45
Width	8.5+/-0.1	8.45	8.45	8.45	8.52	8.51	8.58
Thickness	0.65+/-0.05	0.84	0.85	0.84	0.65	0.67	0.65
Criteria		thicker	thicker	thicker	OK	OK	OK

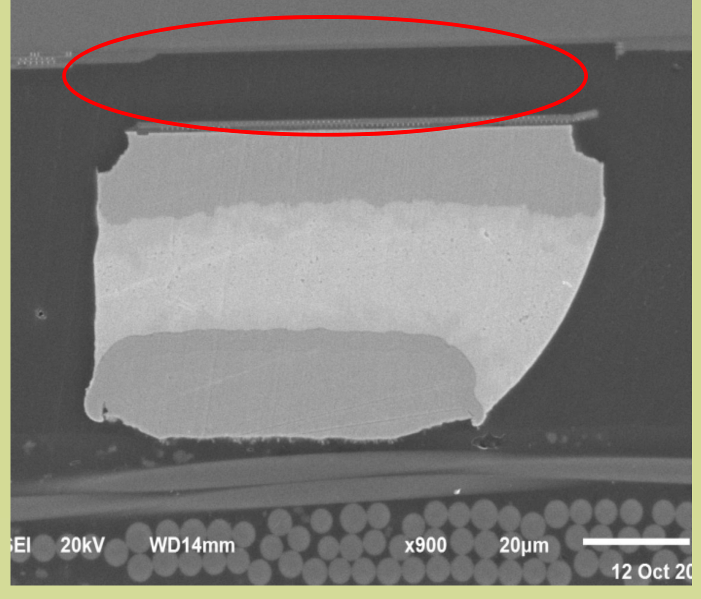
	Unit : mm	Gold bump on Organic			Copper pillar on Organic		
		sample1	sample2	sample3	sample1	sample2	sample3
Length	8.5+/-0.1	8.55	8.42	8.4	8.4	8.43	8.44
Width	8.5+/-0.1	8.47	8.41	8.4	8.4	8.48	8.43
Thickness	0.65+/-0.05	0.77	0.76	0.76	0.61	0.6	0.61
Criteria		thicker	thicker	thicker	OK	OK	OK



Type	SCSP	CSP	COB
TTL	3.8mm	3.8mm	3.8mm
Sensor	0.2mm	0.3mm	0.2mm
PCB	0	0.4mm	0.4mm
Total thickness	4.0 mm	4.5mm	4.4mm

Failure of Flip Chip Bumping

SEM Micrograph of Flip Chip bumps



Delamination of Cu-Pillar Bump after Reflow

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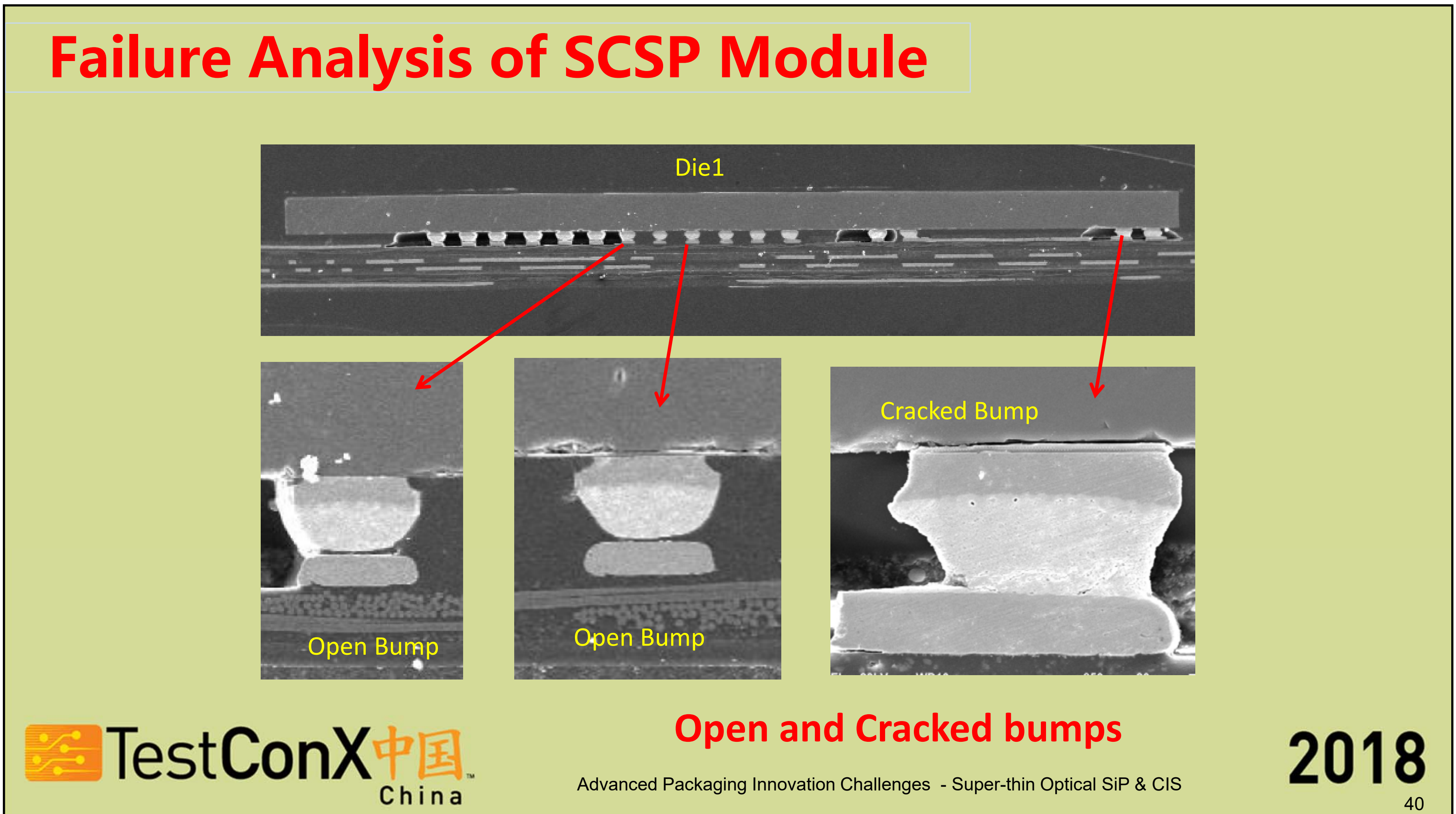
Failure Analysis of SCSP Module
Die1
Open Bump
Open Bump
Cracked Bump
Open and Cracked bumps
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Yield of SCSP Module

成品数量及SMT贴装情况

❑ 产品BOM成品及出货数量

Group	SMT成品	验证Reflow 焊接效果拆除IC	固化炉后未点Underfill胶 IC 脱落	出货数量	备注
CIS-1-A	30			30	Underfill 胶水评估过程中，同Panel未点胶物料会和单个已点胶的物料一起过固化炉，炉后发现有一定比例的没有点Underfill 胶水的物料有IC脱落的现象
CIS-1-B	62	2	6	54	
CIS-2-B	29		2	27	
CIS-3-B	20			20	
Total	141	2	8	131	

*所有原材料客户均已带走，抛料及固化炉后脱落原因需进一步分析

❑ 物料使用及贴装良率

SCSP Yield > 90%

物料 / Group NO	电容			插座			IC			
Group	投入数	贴装数	贴装良率	投入数	贴装数	贴装良率	投入数	贴装数	抛料	贴装率
CIS-1-A	390	390	100%	78	78	100%	34	30	4	88.2%
CIS-1-B	330	330	100%	66	66	100%	68	62	6	91.2%
CIS-2-B	330	330	100%	66	66	100%	31	29	2	93.5%
CIS-3-B	240	240	100%	49	48	98.0%	21	20	1	95.2%
Total	1290	1290	100%	259	258	99.6%	154	141	13	91.6%

*Reflow后1pc插座偏位不良

插座偏位

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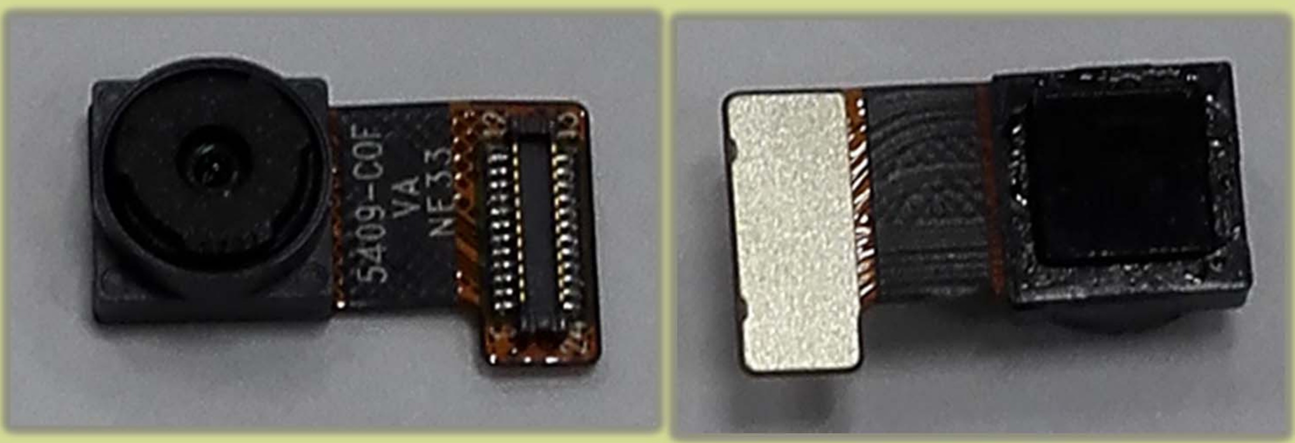
SCSP module



Front Side

Back Side

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Thank you for your attention!