NINETEENTH ANNUAL

BiTS™

Burn-in & Test Strategies Workshop

March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

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Thermal Performance of Burn-In Board for Bare Die Qualification

Sujata Paul - Cisco Systems
Jason Cullen - Plastronics

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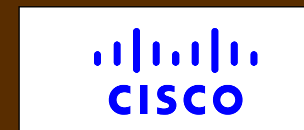


Agenda

- Introduction / Objective
- Overview of Project
- Theoretical Modeling – Thermal Simulations
- Real-World Testing – Thermal Measurements
- Conclusions

Objective: Re-Visit 2 BiTS Presentations to see if we can simulate & predict die temperature of CPAK Module Components on a Mother Board.

Reliability Characterization of Unpackaged (bare) die for Silicon Photonics module

Cisco: Sujata Paul, Andrew Fong, Samir Alqadhy, Huy Nguyen, Zoe Conroy
EAG (Evans Analytical Group): Jag Jassal, Tom Elliot

2016 BiTS Workshop
March 6 - 9, 2016

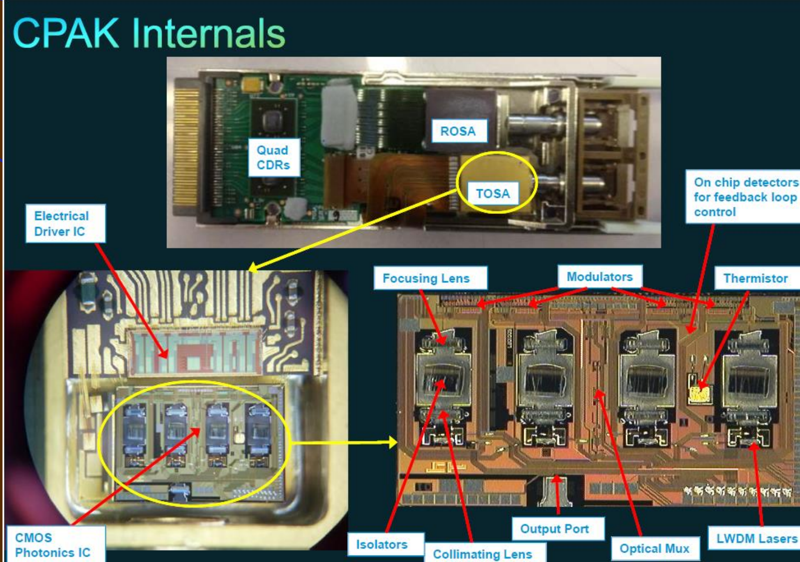
Modeling Socket Thermal Performance Inside a Burn-In Chamber

Jason Cullen
Plastronics Sockets & Connectors

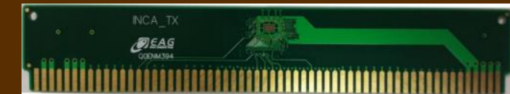
2016 BiTS Workshop
March 6 - 9, 2016

Quick Summary: Silicon Photonics Modules

Cisco CPAK 100Gbps Module

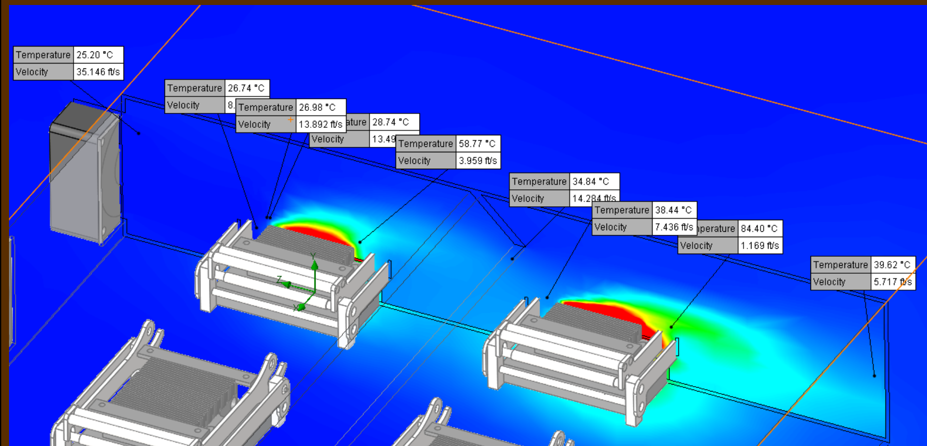


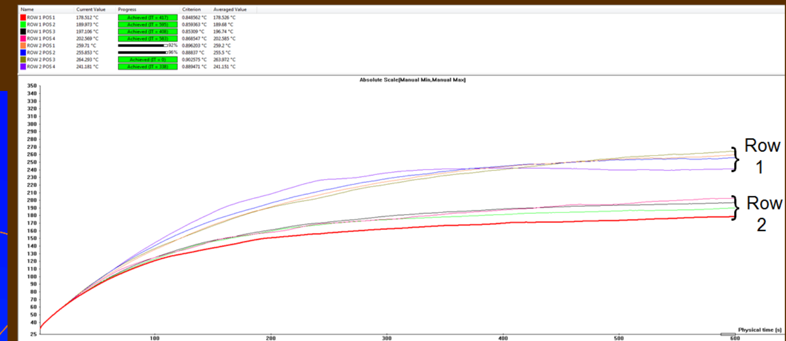
Original Mother Board (16 Positions)



Original Daughter Card

Quick Summary: Modeling Socket Thermal Performance





For passively cooled components, the temperature profile variance between socket locations on a BIB was significant, on the order of 10ºC.

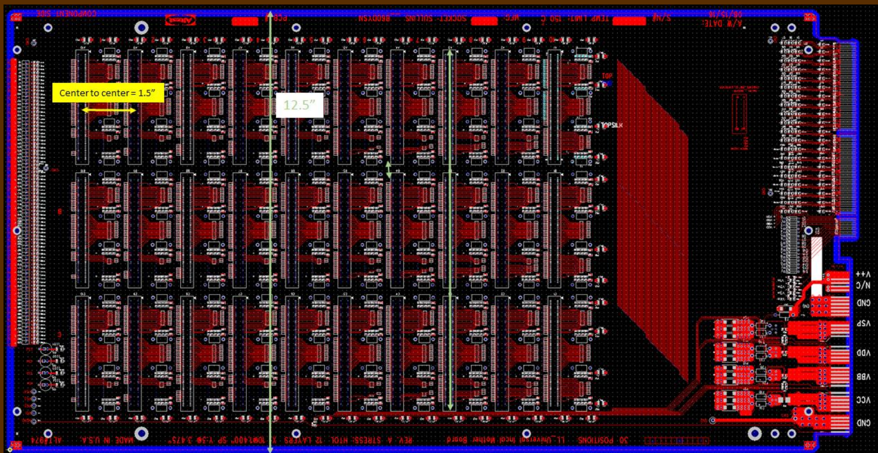
Thermal Performance of Burn-In Board for Bare Die Qualification

Theoretical Modeling – Thermal Simulation

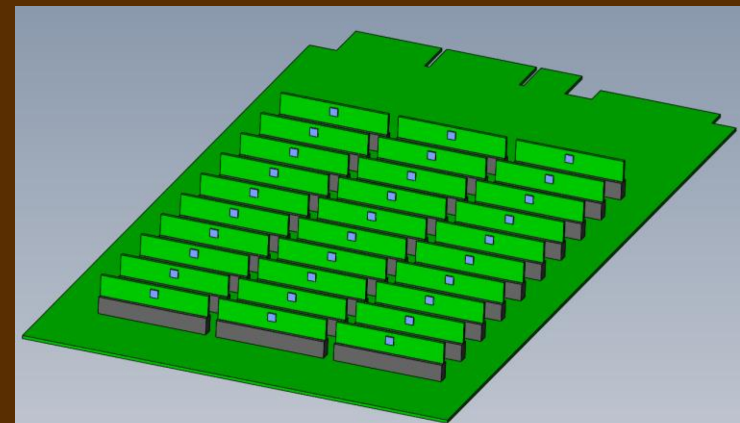
Since 2016, the HTOL BIB has changed:

-Larger profile to accommodate 30 modules (was 16).

-3 x 10 Configuration



BIB Layout



3D Solid Model of Populated BIB

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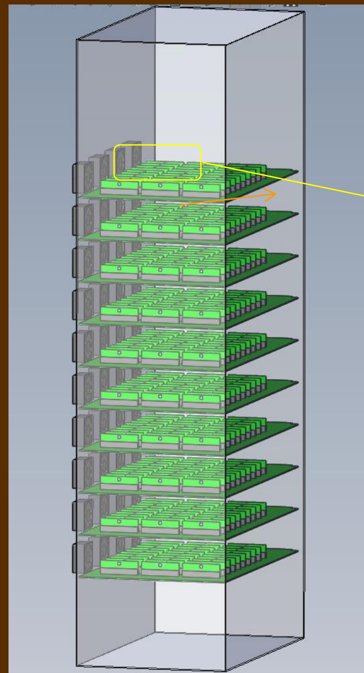
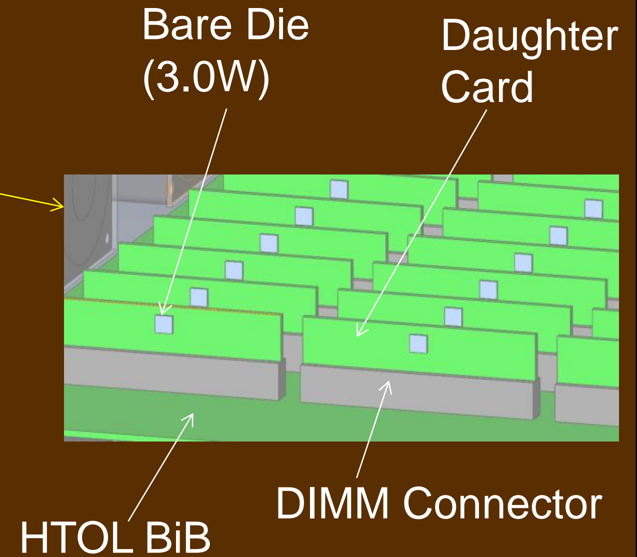
Theoretical Modeling – Thermal Simulation

HTOL Chamber



Simulated Chamber
- -10 populated Slots
- -30 Modules/BIB
- -3.5" spacing



Theoretical Modeling – Thermal Simulation

SIMPLIFIED MODEL:

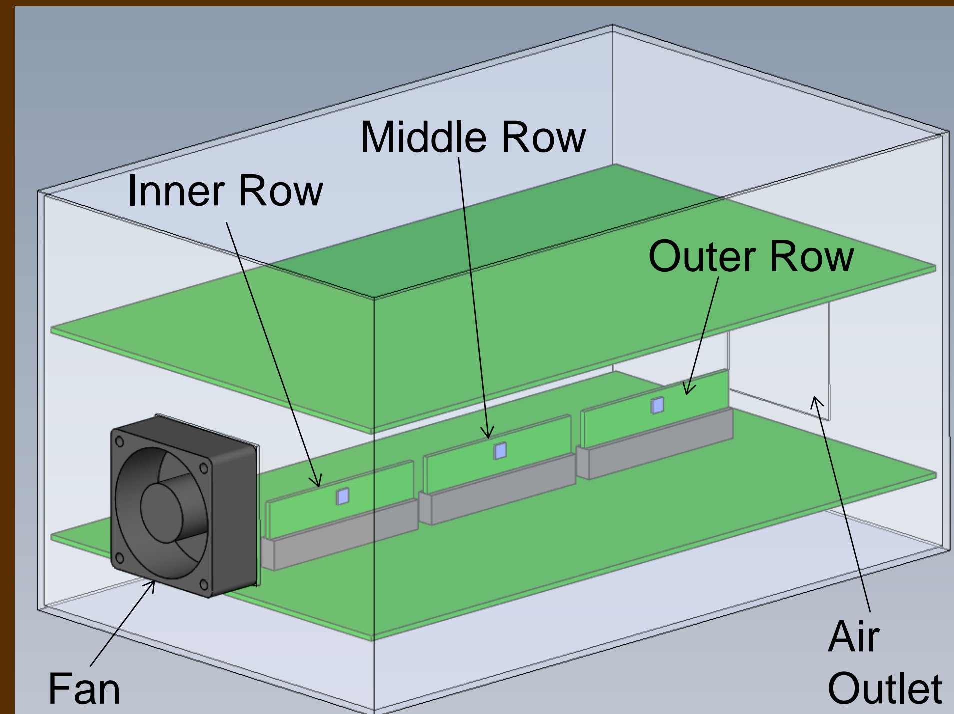
-Fully populated Chamber (3.5” Air Gap above PCB)

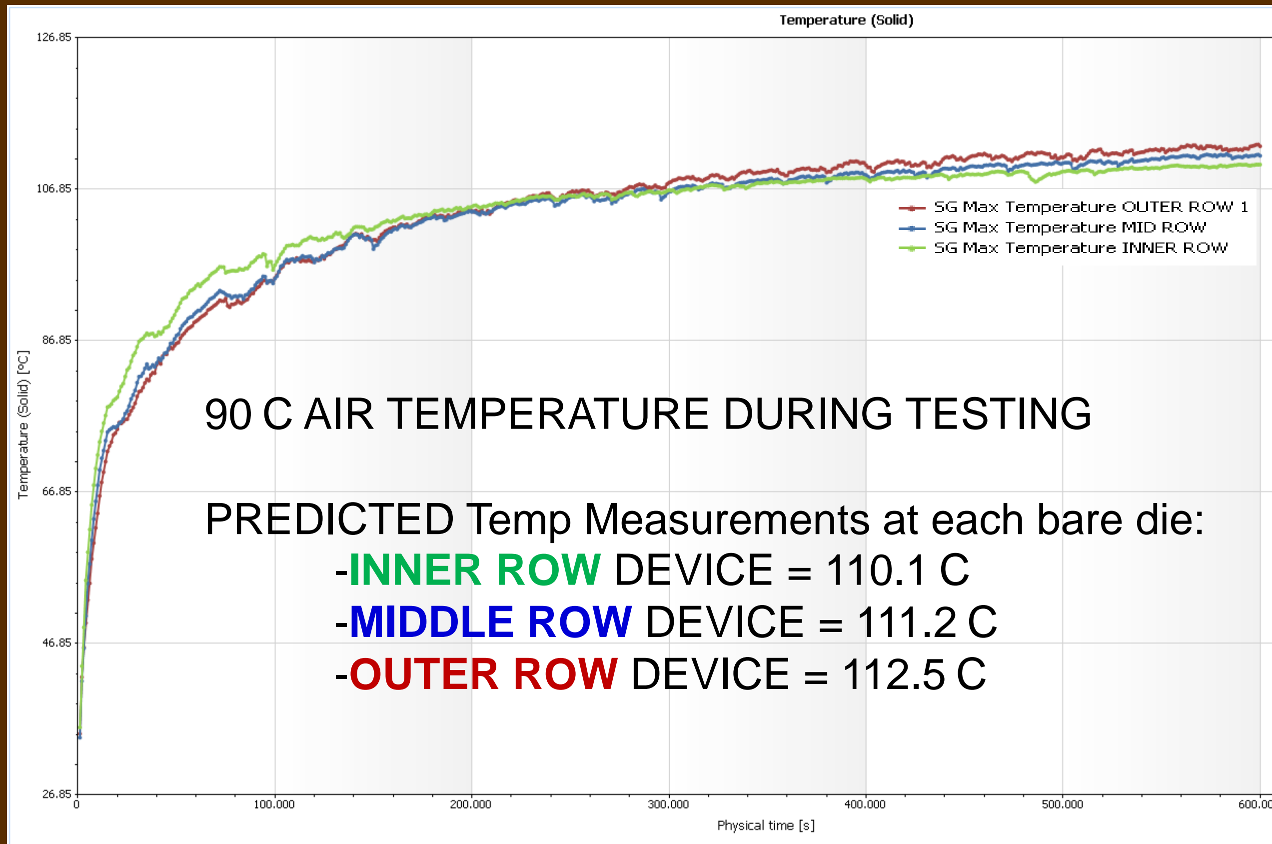
-3.0 W Module Dissipation

-3 MODULES ON PCB (Inner/Mid/Outer Module)

-10CFM COOLING FAN

90 C Chamber Temperature

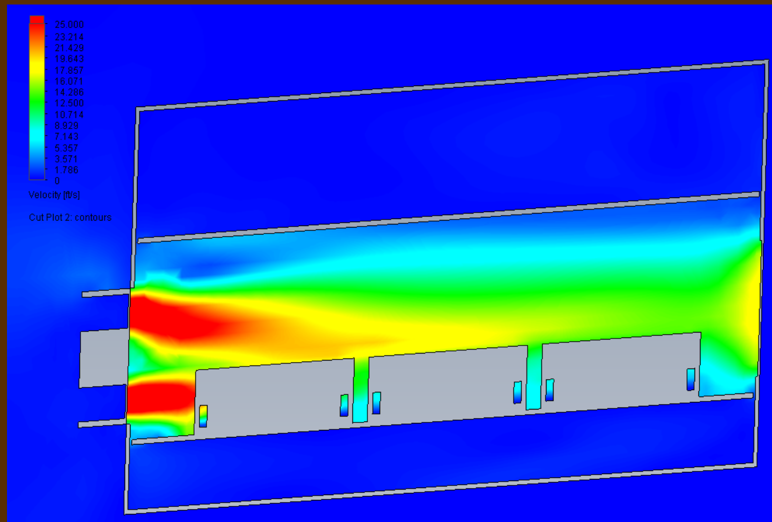




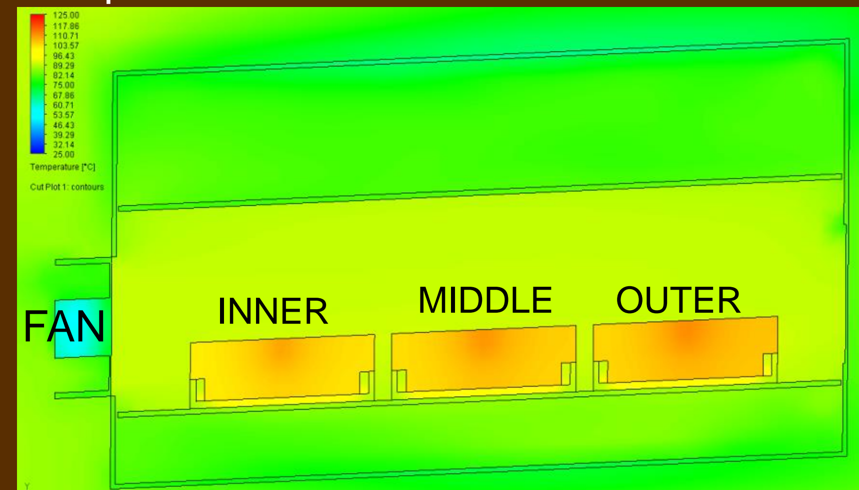
The model predicts devices will reach between 110 and 112.5 C

Theoretical Modeling – Thermal Simulation

Airflow Velocity Profile:



Temperature Profile:



Theoretical Modeling – Thermal Simulation

SIMPLIFIED MODEL:

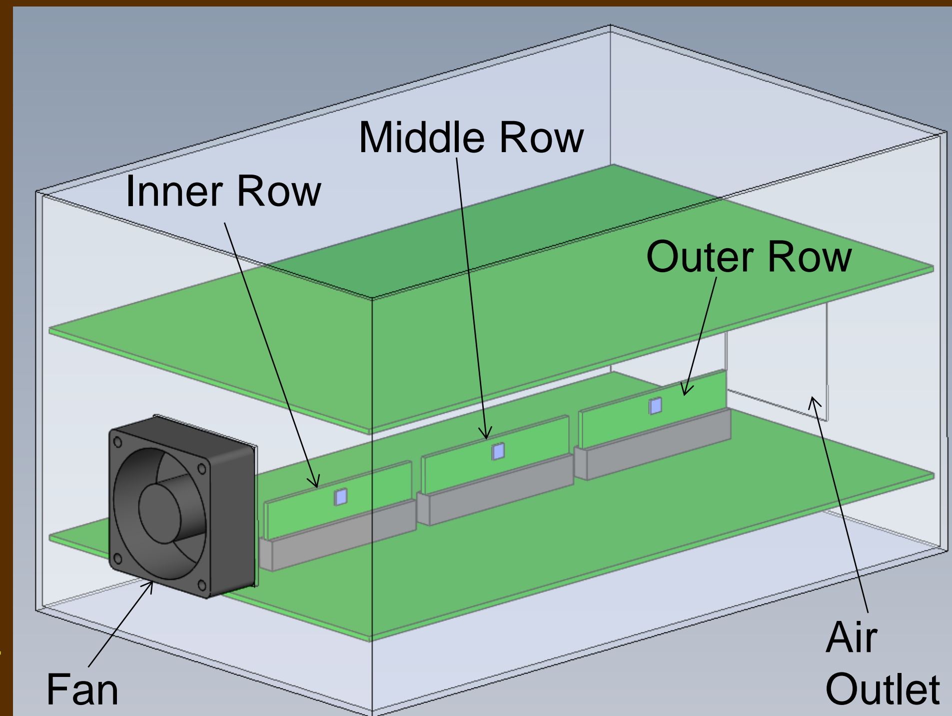
-Fully populated Chamber
(3.5” Air Gap above PCB)

-3.0 W Module Dissipation

-3 MODULES ON PCB
(Inner/Mid/Outer Module)

-10CFM COOLING FAN

110 C Chamber Temperature



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110 C AIR TEMPERATURE DURING TESTING

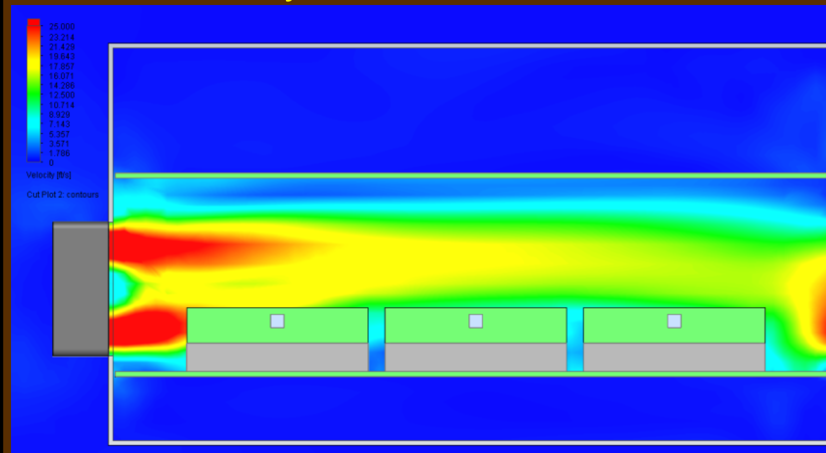
PREDICTED Temp Measurements at each bare die:

- -**INNER ROW** DEVICE = 129.2 C
- -**MIDDLE ROW** DEVICE = 130.2 C
- -**OUTER ROW** DEVICE = 131.3 C

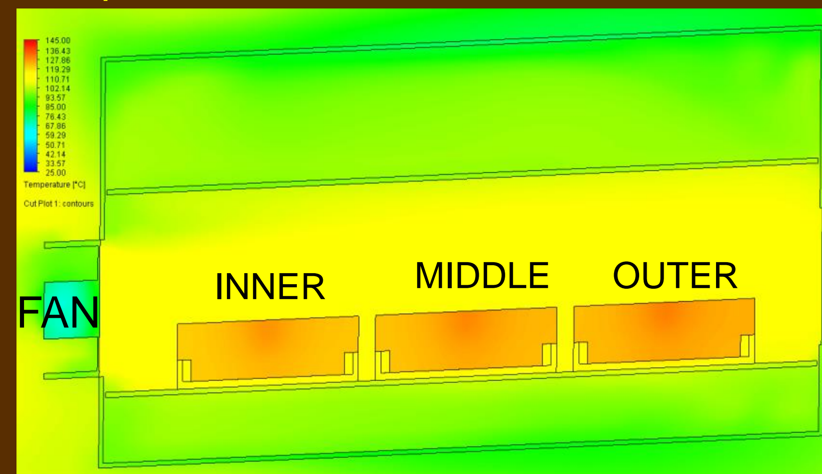
The model predicts devices will reach between 129 and 131.3 C

Theoretical Modeling – Thermal Simulation

Airflow Velocity Profile:



Temperature Profile:



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Real-World Testing – Thermal Measurements

-Measurements recorded with thermocouple at bare die surface
Die Location ID: Inner Row = A ; Middle Row = B; Outer Row = C

Oven temp set to 90C				
	4 parts to collect temp			
POSITION	A1	A8	B6	C10
DIE TEMPERATURE	103.5	103.9	102.6	101.9
SIMULATION VALUE	110.1	110.1	111.2	112.5
	6.4%	5.9%	8.4%	10.4%

Oven temp set to 110C				
	4 parts to collect temp			
POSITION	A1	A8	B6	C10
DIE TEMPERATURE	124.4	125.3	123.3	122.8
SIMULATION:	129.2	129.2	130.2	131.3
	3.8%	3.2%	5.6%	7.0%

Oven temp set to 100C				
	4 parts to collect temp			
POSITION	A1	A8	B6	C10
DIE TEMPERATURE	112.9	114.8	112.9	112.5
SIMULATION:	119.8	119.8	121.1	122.3
	6.1%	4.4%	7.2%	8.7%

Conclusions

- Simulated results were between 3.2% and 10.2% higher than actual measured values.
- The difference could be attributed to modeling of the Daughter Card (Negligible heat transfer to BIB) and/or the airflow inlet/exhaust values.
- Simulation results on the high side of temperature protect from a possible thermal runaway condition.

  (i.e. Initial Chamber Setting)
- Simulation is still not a full substitute for real-world testing, but it is a valuable starting point!