NINETEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

COPYRIGHT NOTICE

www.bitsworkshop.org

Path to First Boot and Volume Validation: Challenges and Opportunity

Vikas Kumar
Intel

BiTS Burn-in & Test Strategies Workshop

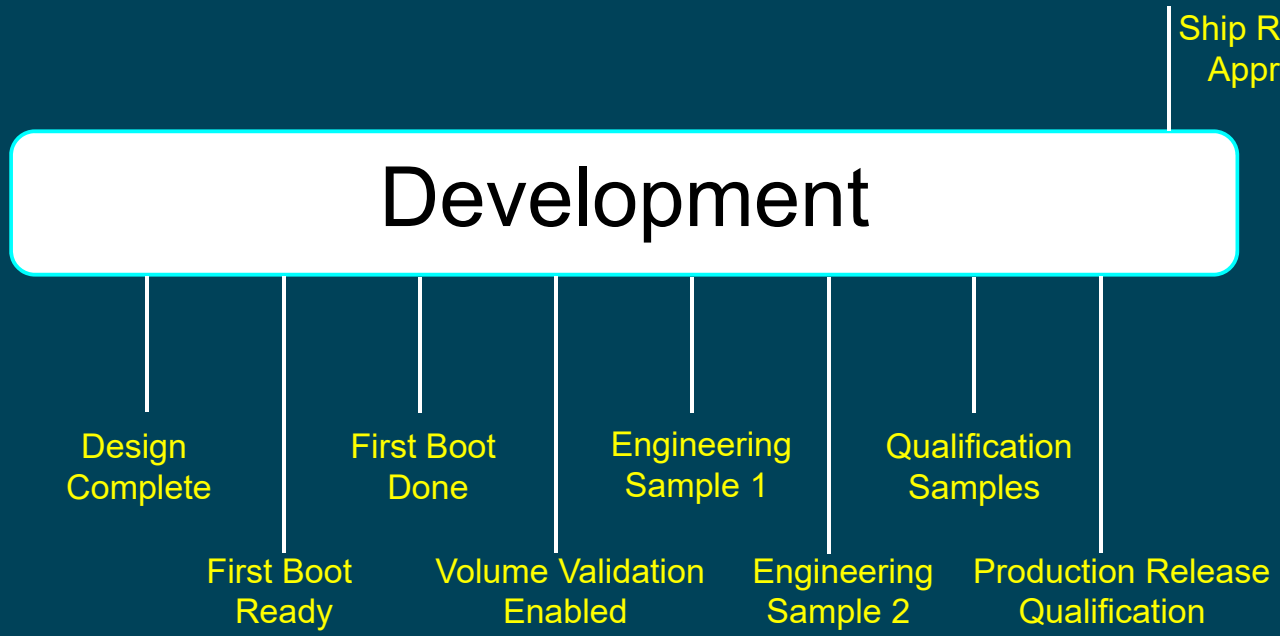
BiTS Workshop
March 4 - 7, 2018

intel

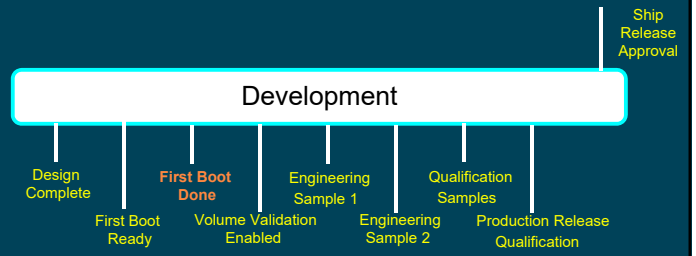
Agenda

- Post-Silicon Development Phase
- Importance of First Boot and Volume Validation Enabling of SoC.
- Pre-Silicon Challenges and Opportunity.
- First Boot and Volume Validation Enabling Stages.
- Post-Silicon Challenges and Opportunity.
- Call for Action.

Post-Silicon Development Phase

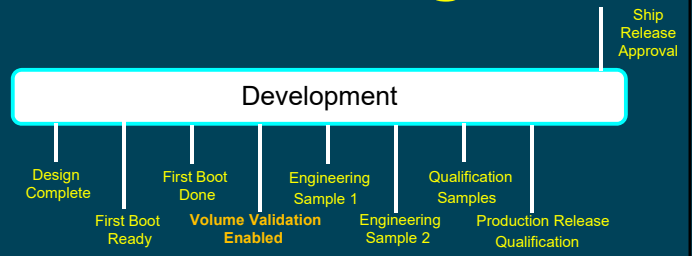


Importance of First Boot



- Boot is most critical flow and gross indicator of silicon health.
- Unblocks validation.

Importance of Volume Validation Enabling

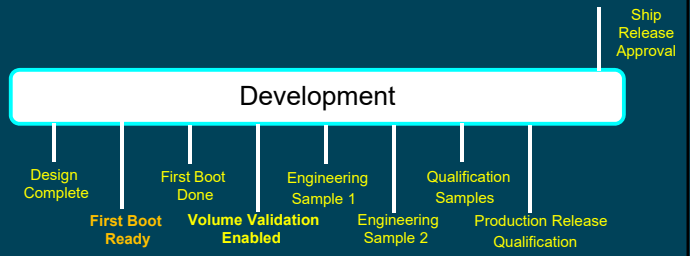


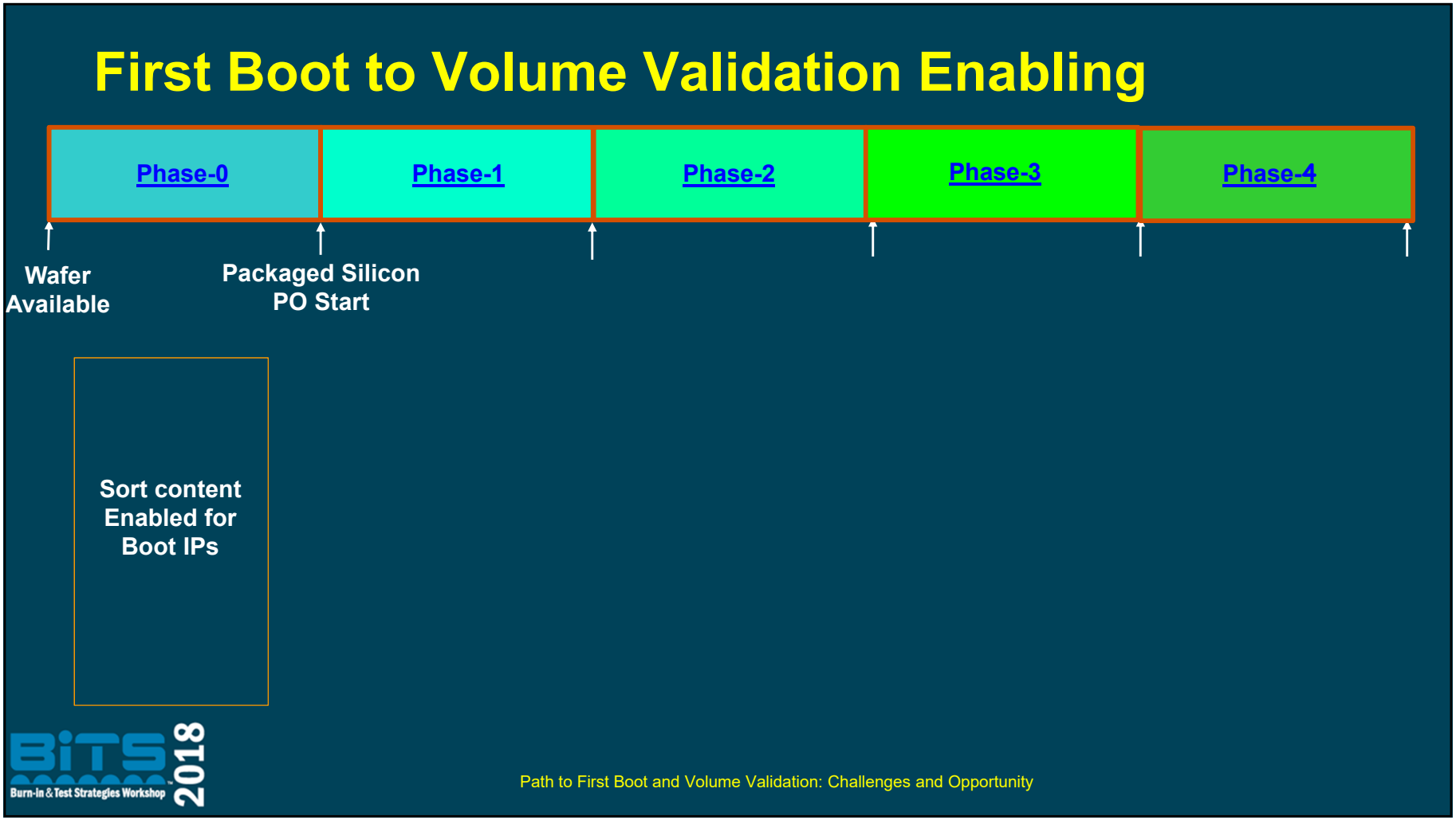
Volume Validation Enabling indicates

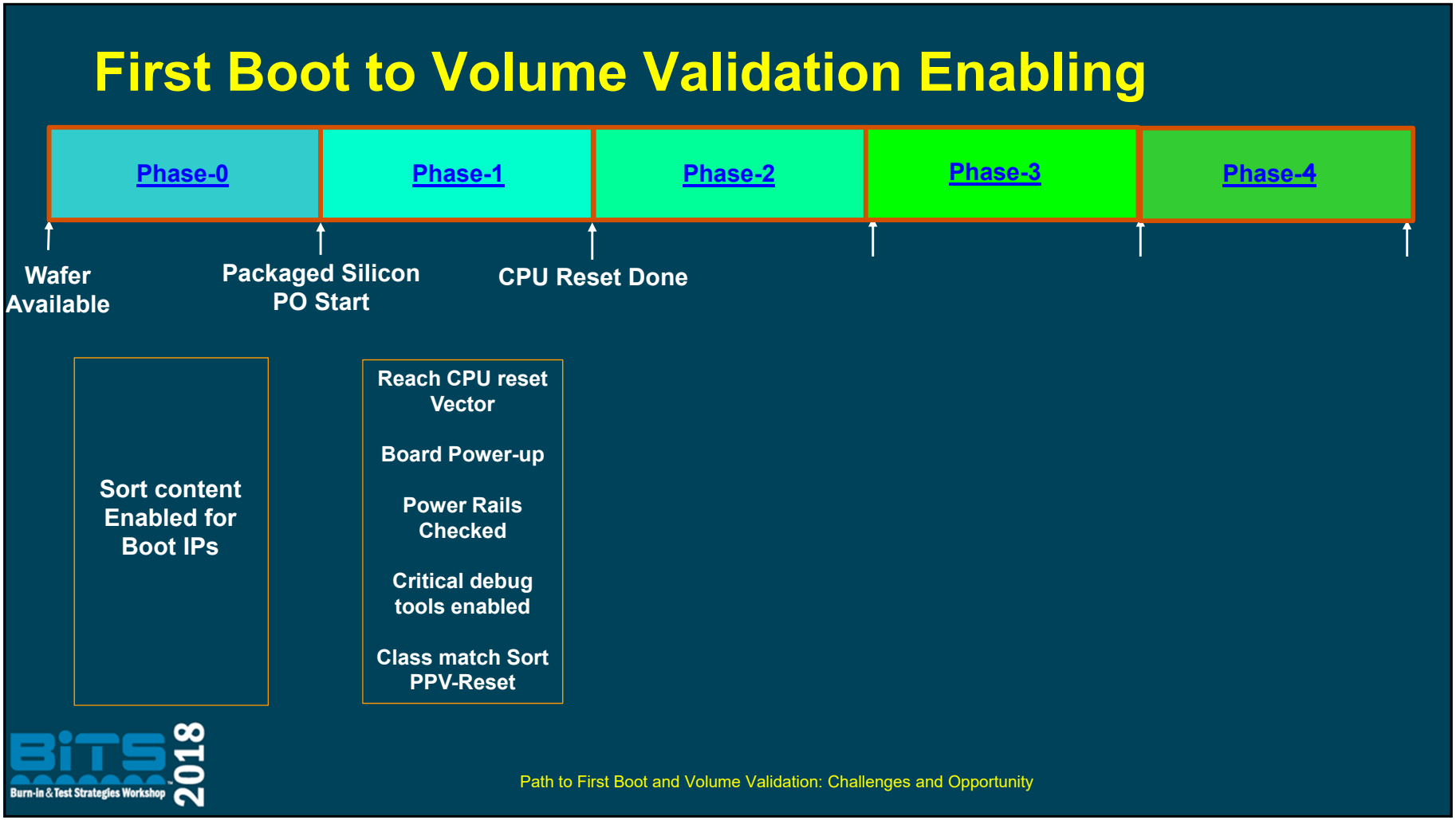
- All features enabled.
- Validation and Test Content enabled.
- Silicon/Platform/Software/Firmware Ready for Volume Deployment.
- Volume Validation can start.
- Can not be done without first boot done.

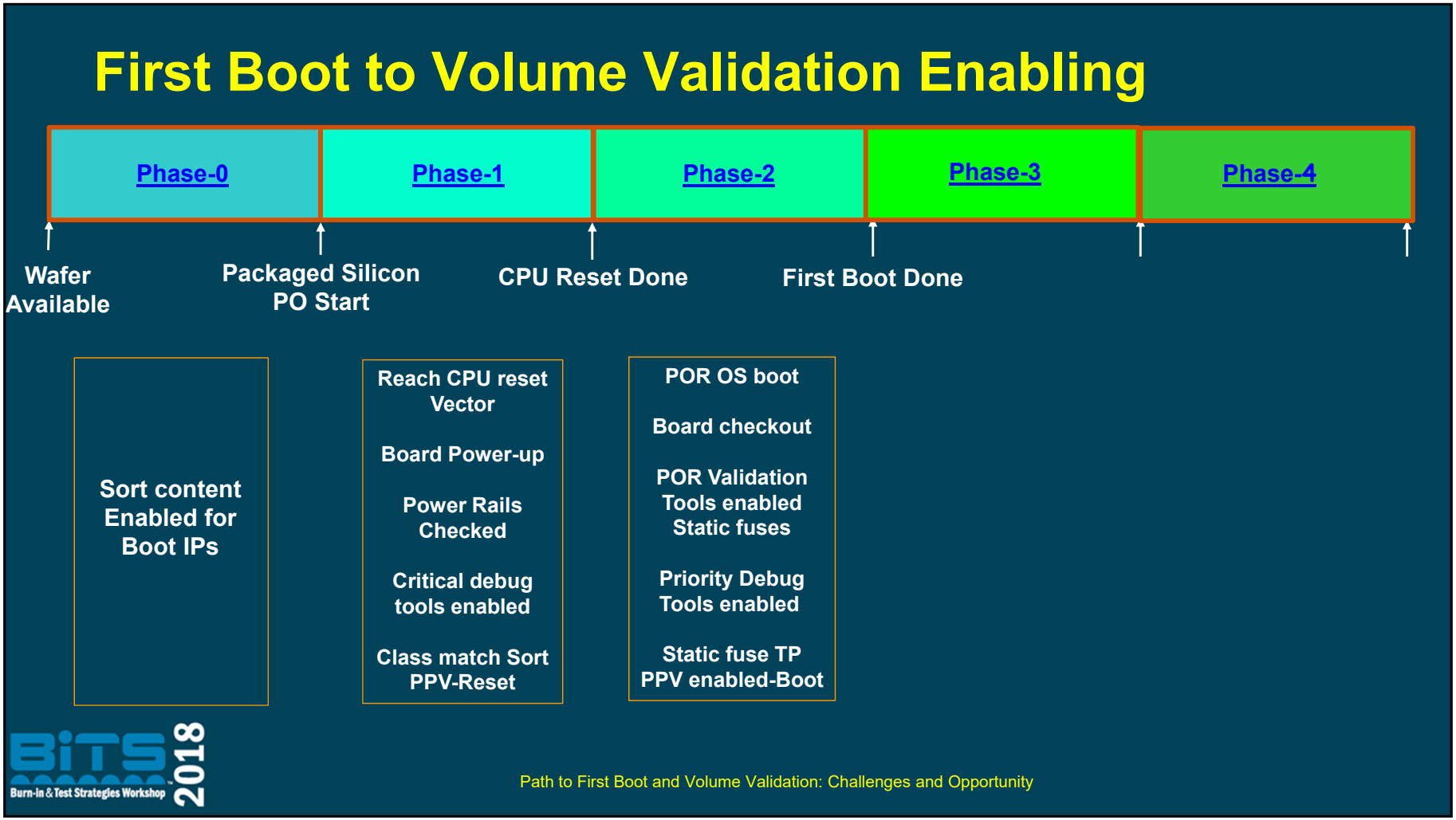
Pre-Silicon Activities

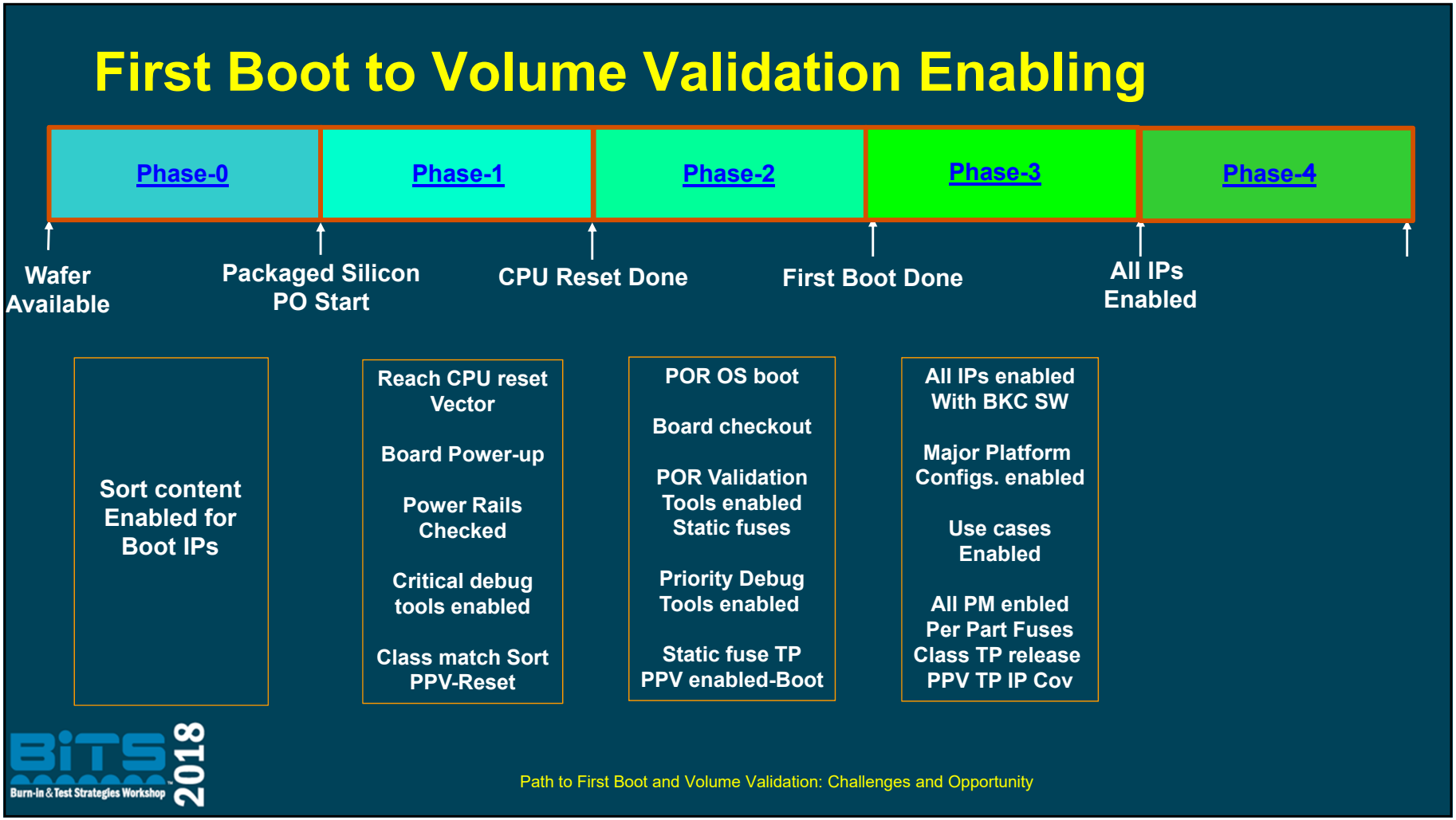
- Shift Left Validation
- Debug Tools.
- Survivability.
- Manufacturing and Test Content readiness
- SW/FW readiness.
- Board readiness.
- First Boot Package.
- Automation.

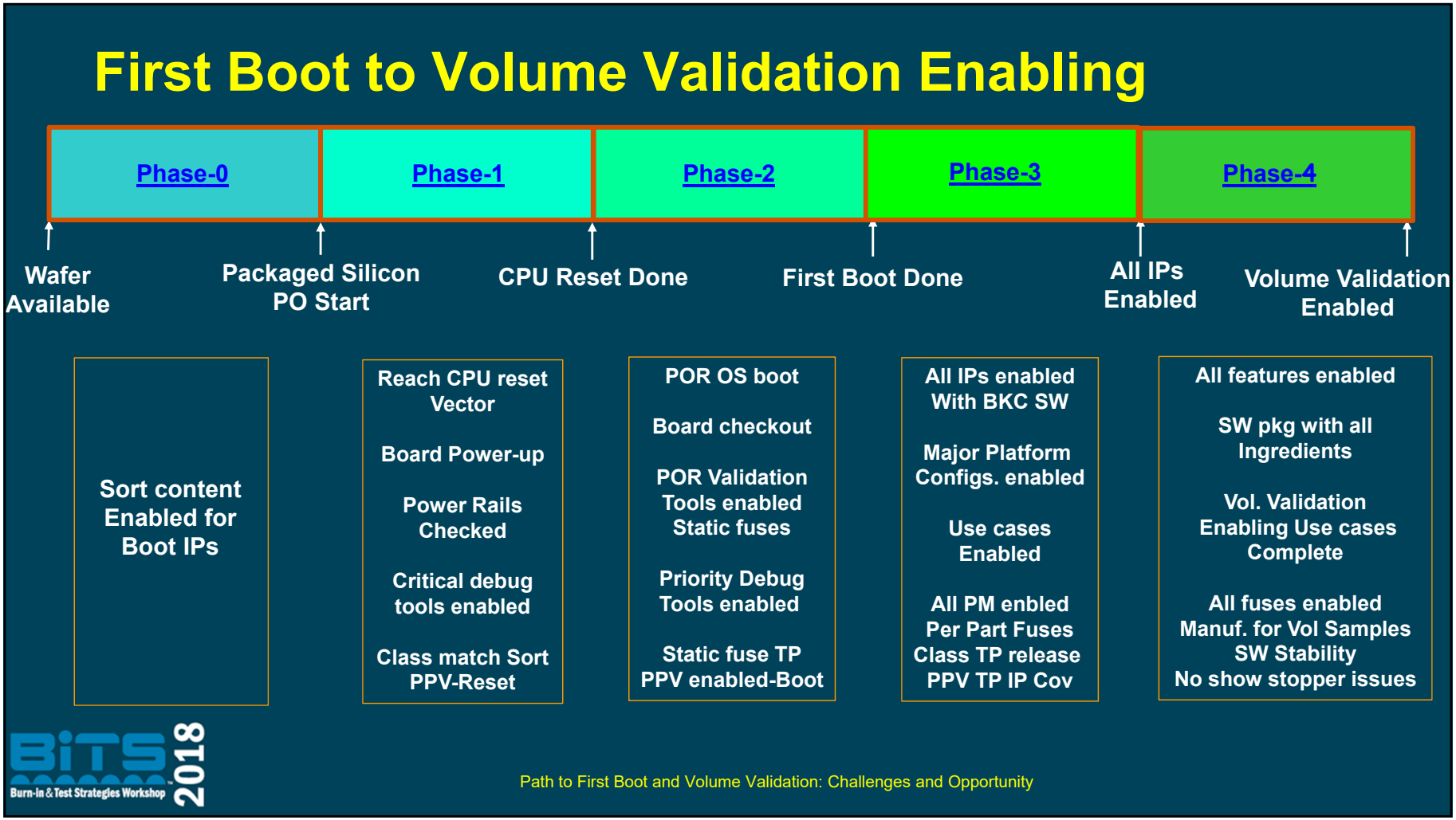


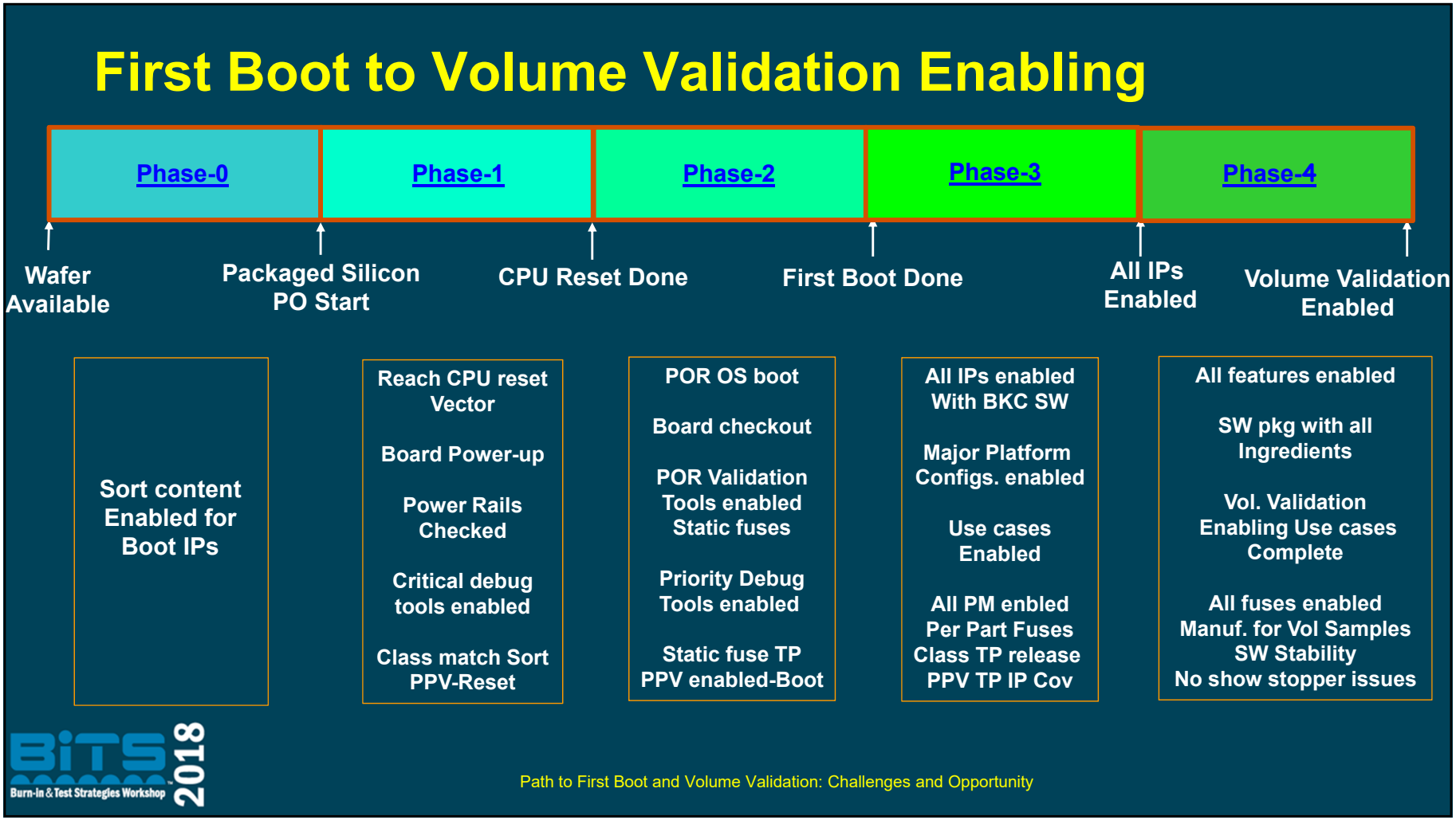

First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
Sort content Enabled for Boot IPs
BiTS 2018
Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity


First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
CPU Reset Done
Sort content Enabled for Boot IPs
Reach CPU reset Vector
Board Power-up
Power Rails Checked
Critical debug tools enabled
Class match Sort PPV-Reset
BiTS 2018
Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity


First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
CPU Reset Done
First Boot Done
Sort content Enabled for Boot IPs
Reach CPU reset Vector
Board Power-up
Power Rails Checked
Critical debug tools enabled
Class match Sort PPV-Reset
POR OS boot
Board checkout
POR Validation Tools enabled Static fuses
Priority Debug Tools enabled
Static fuse TP PPV enabled-Boot
BiTS 2018
Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity


First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
CPU Reset Done
First Boot Done
All IPs Enabled
Sort content Enabled for Boot IPs
Reach CPU reset Vector
Board Power-up
Power Rails Checked
Critical debug tools enabled
Class match Sort PPV-Reset
POR OS boot
Board checkout
POR Validation Tools enabled Static fuses
Priority Debug Tools enabled
Static fuse TP PPV enabled-Boot
All IPs enabled With BKC SW
Major Platform Configs. enabled
Use cases Enabled
All PM enbled Per Part Fuses Class TP release PPV TP IP Cov
BiTS 2018
Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity


First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
CPU Reset Done
First Boot Done
All IPs Enabled
Volume Validation Enabled
Sort content Enabled for Boot IPs
Reach CPU reset Vector
Board Power-up
Power Rails Checked
Critical debug tools enabled
Class match Sort PPV-Reset
POR OS boot
Board checkout
POR Validation Tools enabled Static fuses
Priority Debug Tools enabled
Static fuse TP PPV enabled-Boot
All IPs enabled With BKC SW
Major Platform Configs. enabled
Use cases Enabled
All PM enbled Per Part Fuses Class TP release PPV TP IP Cov
All features enabled
SW pkg with all Ingredients
Vol. Validation Enabling Use cases Complete
All fuses enabled Manuf. for Vol Samples SW Stability No show stopper issues
BiTS 2018 Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity


First Boot to Volume Validation Enabling
Phase-0
Phase-1
Phase-2
Phase-3
Phase-4
Wafer Available
Packaged Silicon PO Start
CPU Reset Done
First Boot Done
All IPs Enabled
Volume Validation Enabled
Sort content Enabled for Boot IPs
Reach CPU reset Vector
Board Power-up
Power Rails Checked
Critical debug tools enabled
Class match Sort PPV-Reset
POR OS boot
Board checkout
POR Validation Tools enabled Static fuses
Priority Debug Tools enabled
Static fuse TP PPV enabled-Boot
All IPs enabled With BKC SW
Major Platform Configs. enabled
Use cases Enabled
All PM enbled Per Part Fuses Class TP release PPV TP IP Cov
All features enabled
SW pkg with all Ingredients
Vol. Validation Enabling Use cases Complete
All fuses enabled Manuf. for Vol Samples SW Stability No show stopper issues
BiTS 2018 Burn-in & Test Strategies Workshop
Path to First Boot and Volume Validation: Challenges and Opportunity

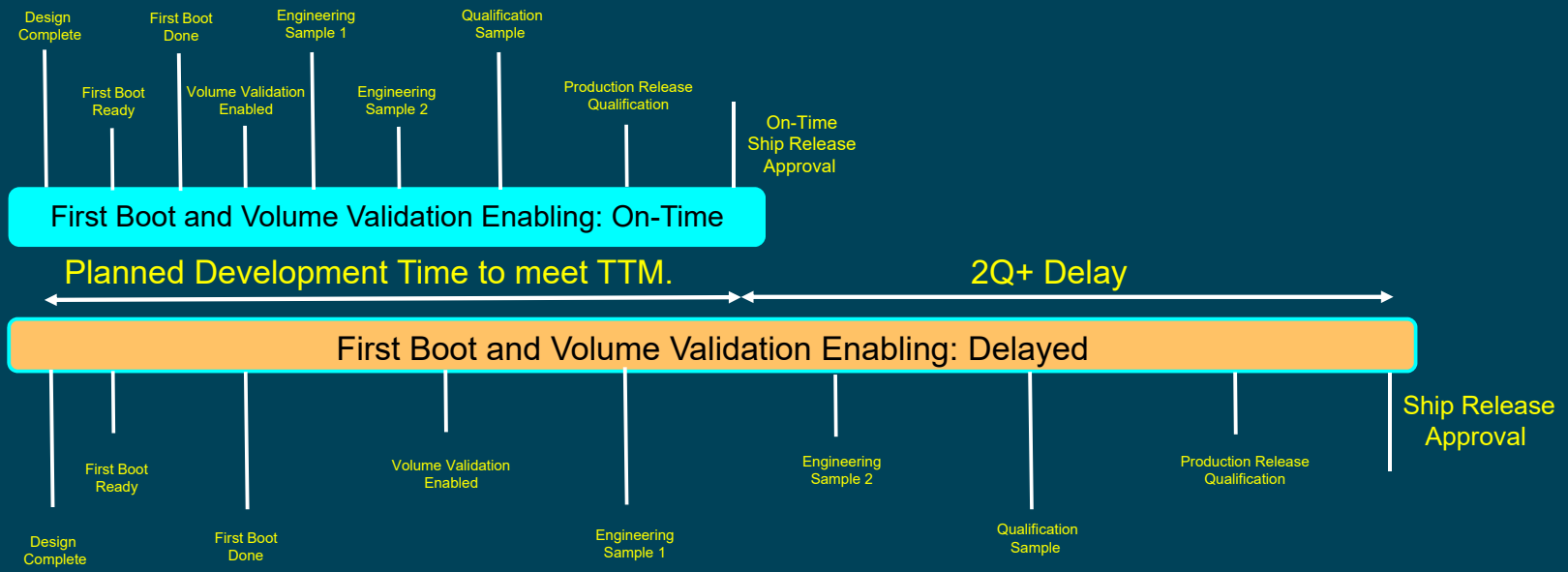
Post-Silicon Challenges and Opportunity …

- Multiple variables plays simultaneously
- Health of the Validation Board.
- Unfused silicon.
- Enabling DFX features.
- Uncharacterized analog circuits/IOs.

Post-Silicon Challenges and Opportunity ..

- Part to Part variation.
- Silicon health without manufacturing screen.
- Identifying, Localizing, Root causing and Fixing problem.
- Using Survivability and DFX features to bypass issues.
- Enabling system level content in manufacturing screen.

Result


Design Complete
First Boot Ready
First Boot Done
Volume Validation Enabled
Engineering Sample 1
Engineering Sample 2
Qualification Sample
Production Release Qualification
On-Time Ship Release Approval
First Boot and Volume Validation Enabling: On-Time
Planned Development Time to meet TTM.
2Q+ Delay
First Boot and Volume Validation Enabling: Delayed
Ship Release Approval
First Boot Ready
Design Complete
First Boot Done
Volume Validation Enabled
Engineering Sample 1
Engineering Sample 2
Qualification Sample
Production Release Qualification

Call For Action

- Techniques for Faster root cause of a silicon bug.
- How to avoid re-spin of silicon to fix a problem.
- Resilient System Design.

Disclaimer

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at www.intel.com.