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28G Test Hardware Signal Integrity Design

Noel Del Rio (NXP), Don Thompson (RDA)

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Scope and target application:

- Electrical performance as presented in this study are specific to the hardware. This paper is about a methodology and partnership (i.e. NXP, RDA, Leeno, Yamaichi, other socket vendors…)
- Applicable to any ATE platform Loadboard. This program started on Advantest 93K™, and propagated to Teradyne UltraFlex™.
- Methods and concepts can be applied to industry test sockets, loadboards, connectors, and fixtures.

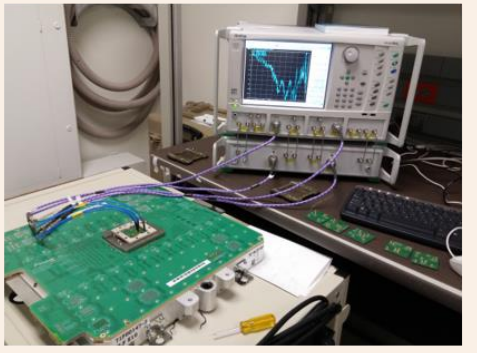
Agenda

- Software Tools , LAB Validation Setup, and fixtures
  - Signal path segment measurement capability
- Bandwidth, Rise/Fall Time, Wave Length
- Signal Path Analysis and Design Target
  - Metric base assessment of the signal path (i.e. serdes I/O)
- Signal Path
  - Dielectric Material and PCB Process
  - DUT Field or Package Ball Grid
  - VIA for 28G
  - Test Strategy : Loop Back, and Loop Back Components.
  - Test Socket…Welcome to the real world
- Signal Path review, target vs actual measurements
- Conclusion

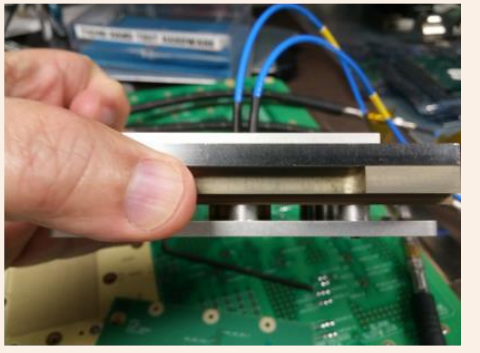
Software for modeling and simulation. Hardware validation tools

Key Software Tools

- ANSYS HFSS
- Advance Design System
- Mentor Graphics HyperLynx SI
- Mathlab
- Cadence Allegro
- Solidworks



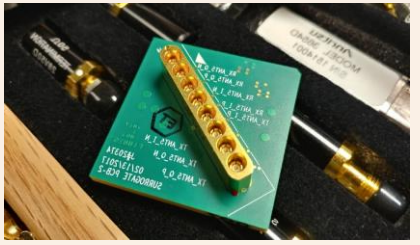
Load Board and Test Socket

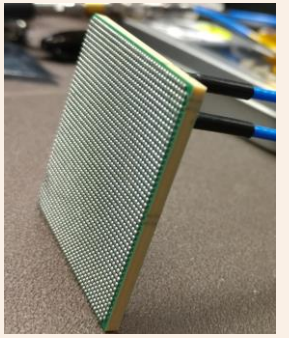


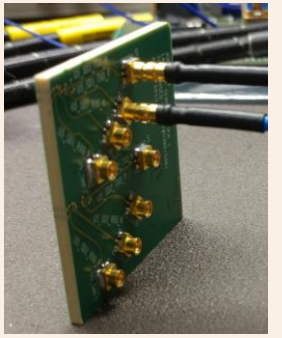
Isolated Test Socket

Hardware Validation :70 Ghz VNA: Load Board and Test Socket Measurement Setup

Test socket interface (Package surrogate)

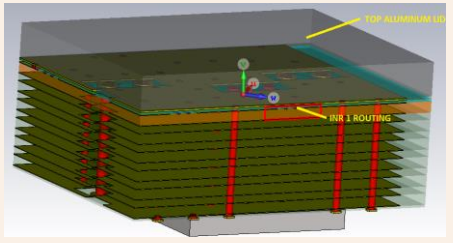






DUT Package Surrogate(Venom RF 5G, UA RF 5G, T4/TV1/LX2 28G)

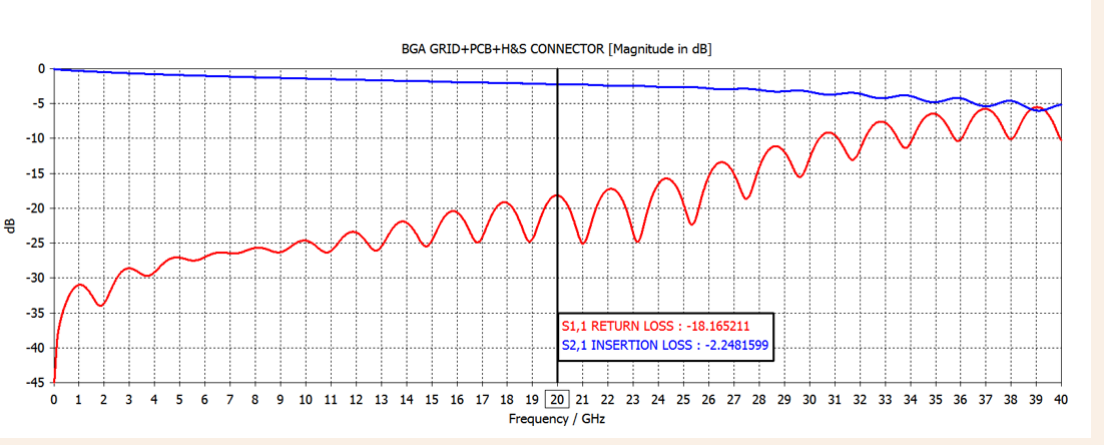
- Precision electrical interface to enable access at the Pogo-pin top
- It is modeled, simulated, and validated with VNA(Vector Network Analyzer)
- Performance Specifications for 28G
  - S21 3dB point >20Ghz
  - S11 -11dB to -15dB at 3dB point
  - Differential Impedance 100 Ohms +5, -5
- De-embed point up to surrogate balls



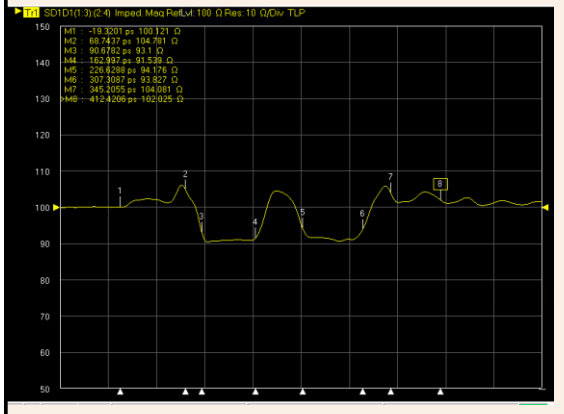
Model and simulation (S21, S11) results for LX2 package surrogate Complete signal path to H&S Connector

Surrogate Performance Targets (for all lanes)

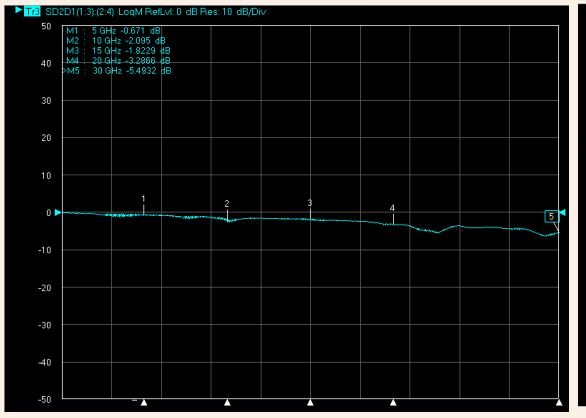
- **S21 3dB point, > 20Ghz**
- **S-11 @ 3dB point, -15dB**
- **Differential Impedance 100 Ohms +/- 5**
- **Correlation or variance for all lanes(i.e. 32 lanes) <<< 1dB @ 3dB Point**



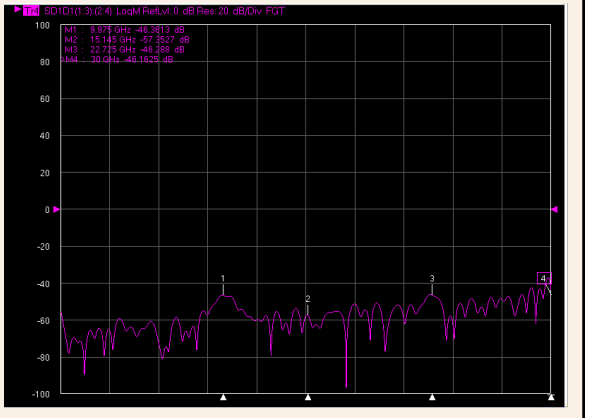
TV1 28G Surrogate Validation Setup, S-parameters, and TDR Plots



TV1 Surrogate TDR Profile, TX & RX Loop



TV1 Surrogate S21 Insertion Loss Profile, TX & RX Loop



TV1 Surrogate S11 Return Loss Profile, TX & RX Loop

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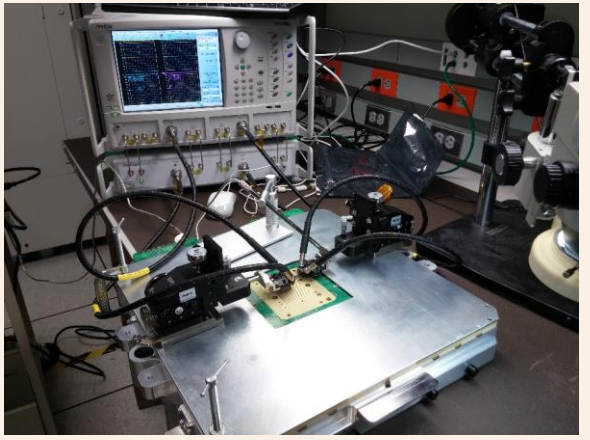
Test Loadboard Validation Setup

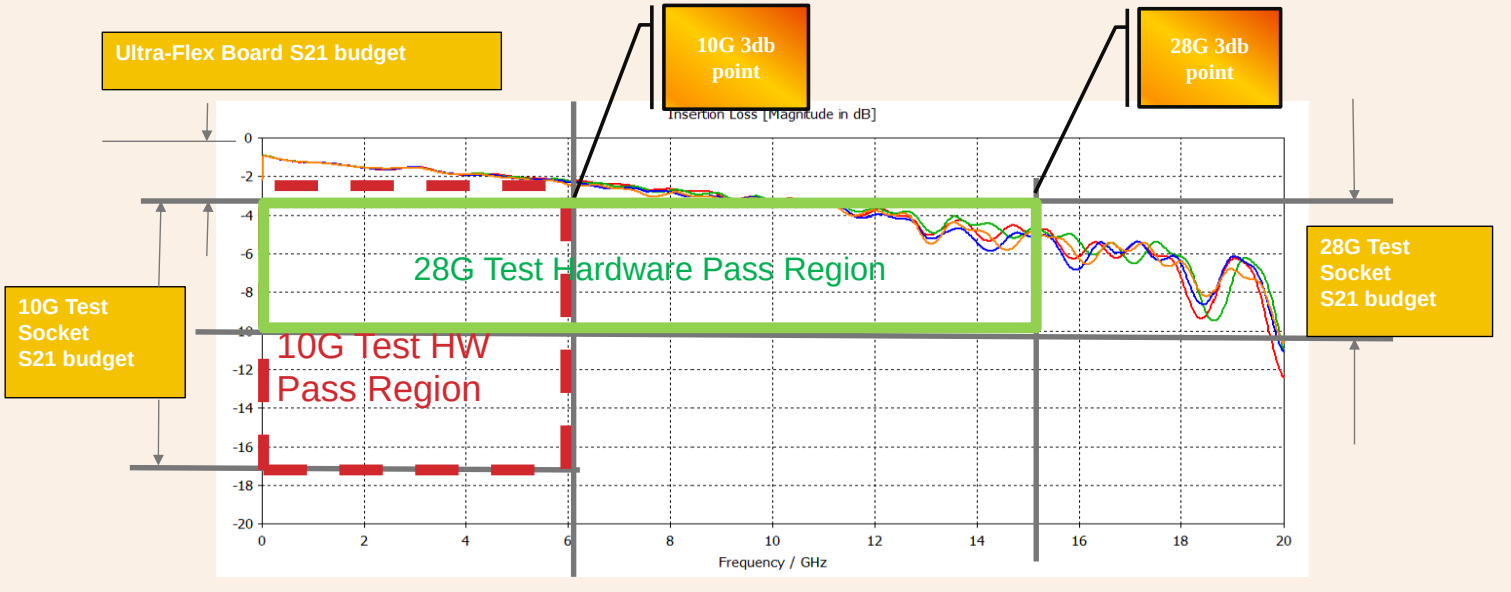


~ 50Ghz Probe setup up differential and single ended

Application of board connectors and interfaces for segmented DUT signal path

Different methodologies and techniques to assess the different segment of the DUT signal path. Individual, isolated and or combined. Full DUT signal path or accumulated effects of the different segment

Loadboard (PCB pad to pad) Measured S21



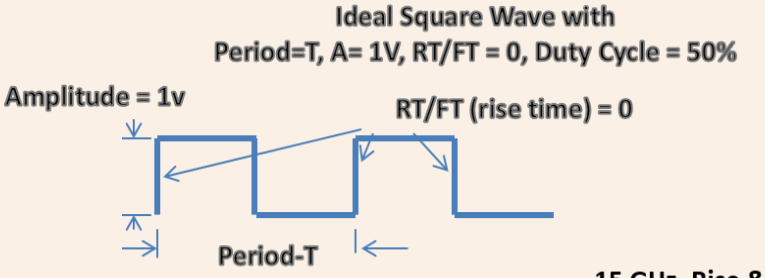
- Enable NXP to validate actual board (populated loadboard) against performance target, models, and simulation results.
- DN populated loadboards undergo 100% VNA performance validation test

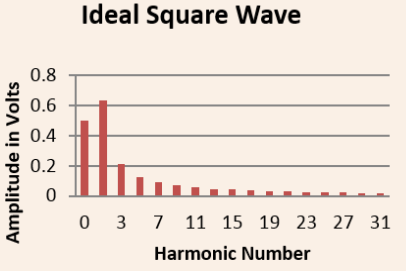
28G Test Hardware Signal Integrity Design

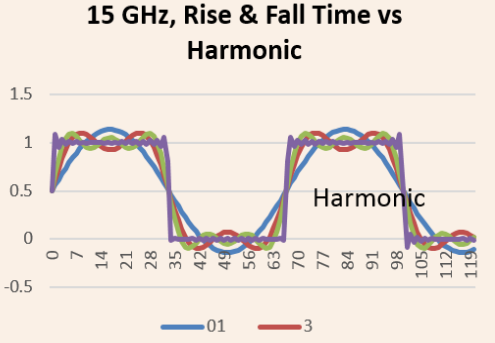
BANDWIDTH ASSESSMENT

Bandwidth Consideration

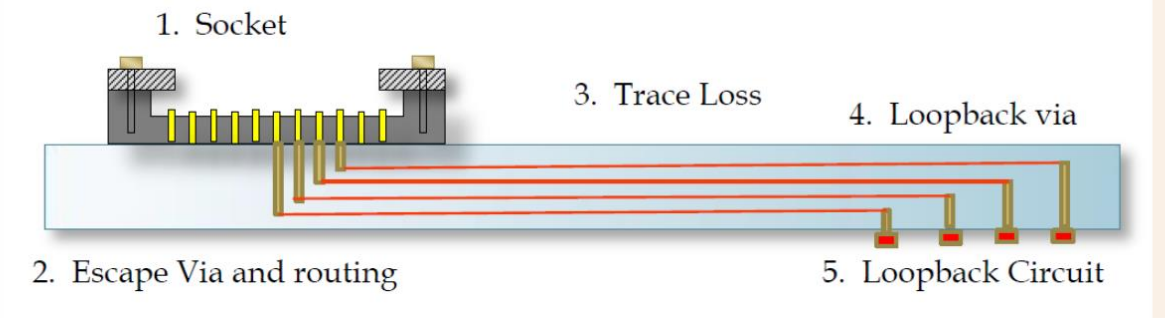
- DFT (Design for Testability)
- Test Strategy
- Cost







SIGNAL PATH ANALYSIS, what are we dealing with



Total Loss = (socket*2) + (escape) + (trace loss) + (LB via*2) + (LB circuit)

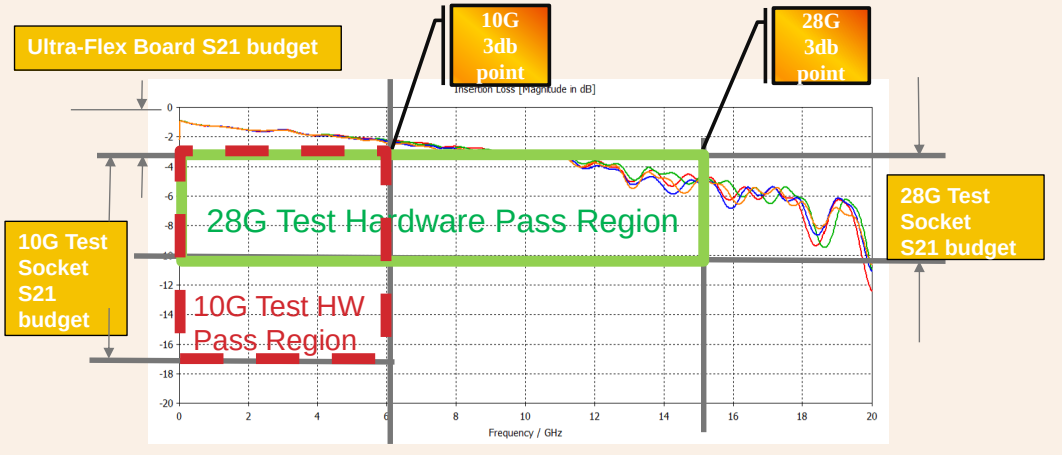
Design Consideration: Data path loss budget & source of discontinuity

- Signal Loss
- Source of discontinuity

DEFINE YOUR DESIGN TARGETS & PARAMETERS

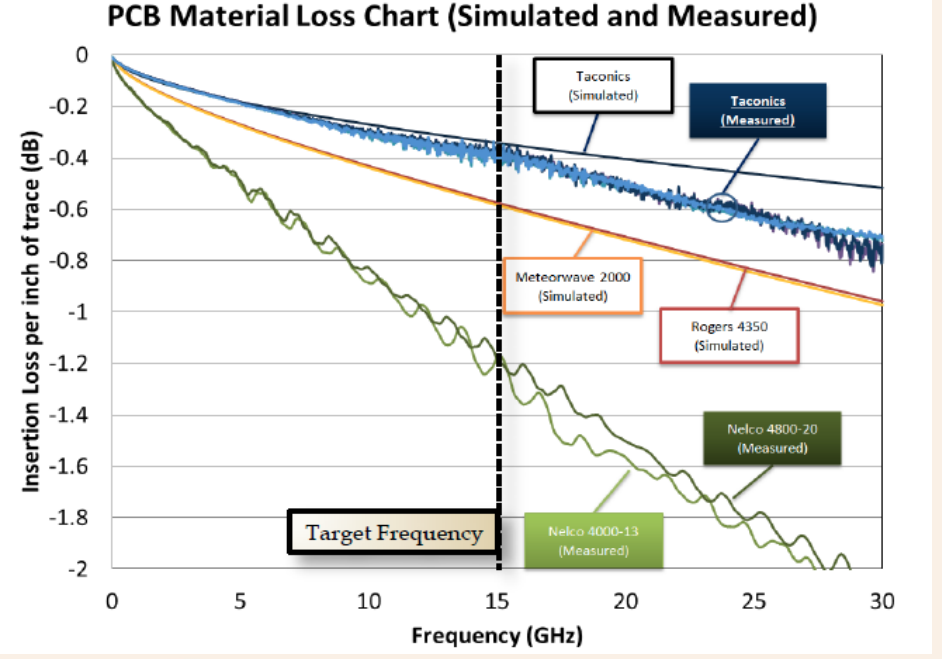
Target Metrics

- S21 3db Point is 15 GHz
- S11 ~ (-10db) at 3db point
- Lane to Lane Correlation <1 dB
- Lane to Layer Correlation <1 dB
- Board to Board Correlation ~ 1 dB
- Loop-Back Impedance @ RX within 10% or 90 Ohm Differential



- Defined performance target based on metrics …S-Parameters, TDR impedance profile
- Objective targets vs traditional practice of litany of design-rules and hope it works.

DIELECTRIC AND PCB FABRICATION PROCESS



- Digital Networking has stopped using PCB design-houses and PCB fabrication vendors that can't present PCB-Process Data (Simulated vs Measured)
- Board validation @ frequency domain is required.
- **PCB Trace is the biggest source of loss in the signal path**

DIELECTRIC AND PCB FABRICATION PROCESS

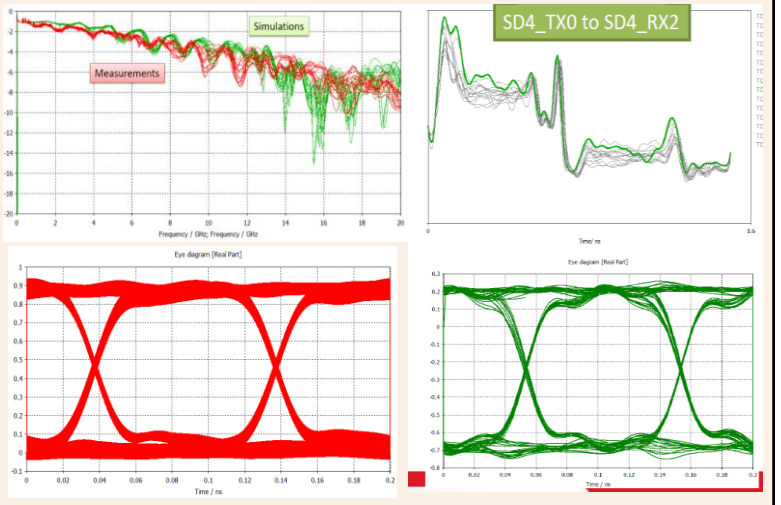
Blind Built Board

Board with Verifiable Target Performance

T4: 4 of 32 Lanes 10G Loadboard
Wide Performance Variance
Inferior insertion loss plot

32 Lanes 10G Designed board
3db pt @ ~ 6ghz
Modeled, Simulated, VNA Tested
High Correlation between Lanes

T4 Dielectric Meteorwave 2000



Measured **Simulated**

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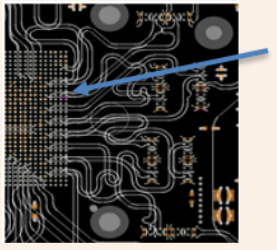
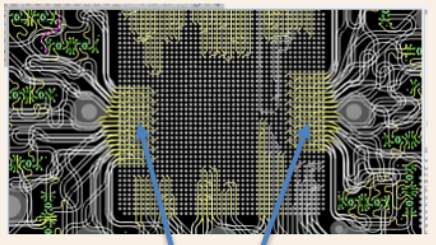
SERDES BALL MAP AND DUTFIELD



16 Serdes I/O at package edge 8 per side



32 Serdes I/O 8 rows deep 16 per side

UltraFlex Board Insertion Loss (S21), Measured

B4 S21

T4 S21

6.000 Ghz

15.000 Ghz

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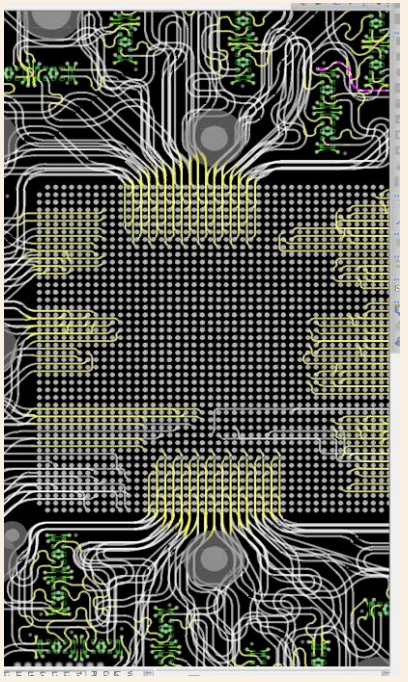
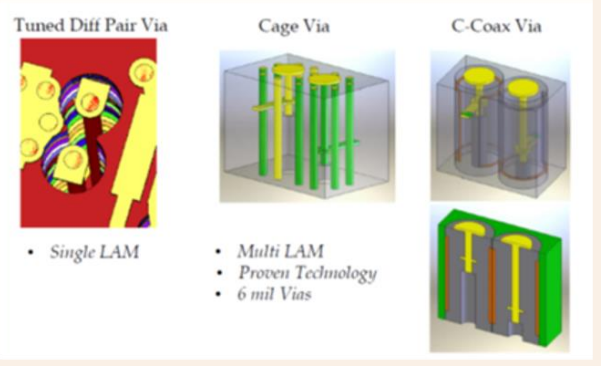
DUTFIELD 28G Summary



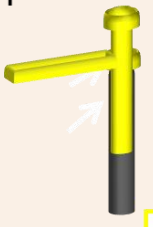
- The SERDES BALLMAP location has profound effect on I/O Performance
- Meet with package designers for preferential ball map profile
- SERDES deep inside the DUTFIELD is most likely to present challenges for 28G.
- SERDES I/O Profile can impact loadboard design, socket and cost
- Additional optimization is required to address issues on high speed I/O s deep inside the grid
- Layer Management is used to mitigate DUTFIELD related routing issues

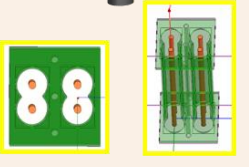
VIA DESIGN as a function of data rate



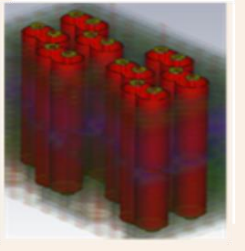
VIA Technologies considered for 28G Test Hardware (RD Altanova)

Optimize Via



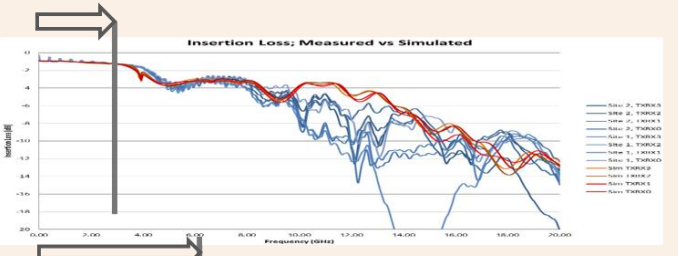


Twin Axial Via

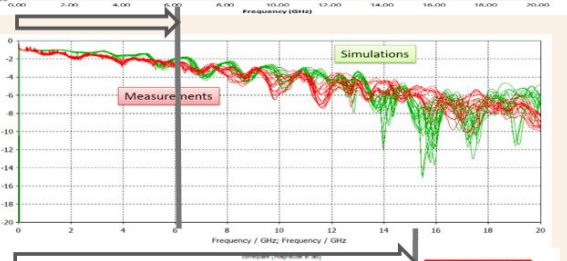


Coax Via

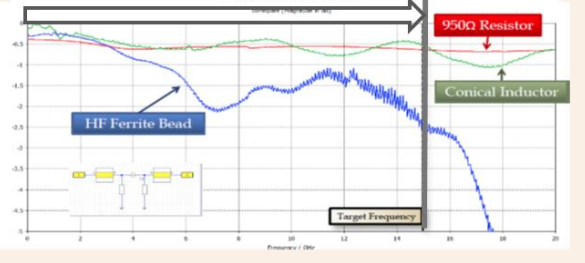
5G



10G

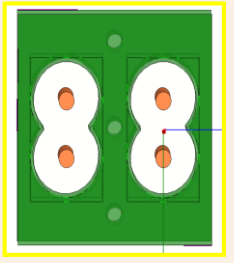


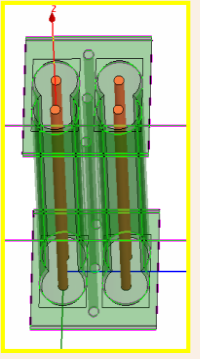
28G



28G Test Hardware Signal Integrity Design

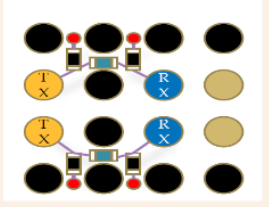
Twin-Axial Via 28G Summary





- Differential Impedance control closer to 100 Simulation results indicate 28G performance is attainable
- Base on mature PCB process
- Can be implemented on >300mil thick boards
- Cheaper than COAX VIA

LOOP BACK DESIGN CONSIDERATION



Performance Verification @ 28G and above

Probe Points / SMP Connectors

Embedded RC on PCB Cavity Under the DUT

Test Contact/Socket

Frame compresses package

Loop Back Circuit
Different Mounting Options
Shortest Trace Length Possible

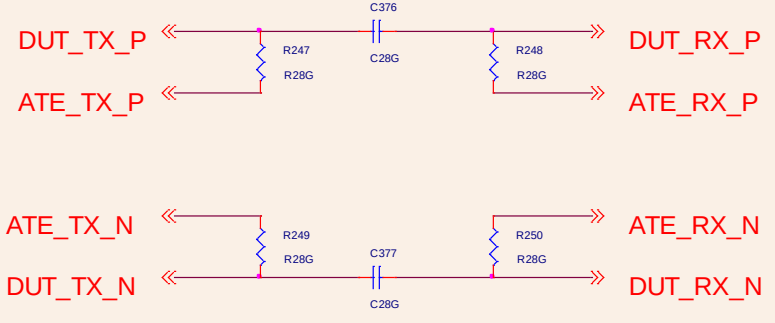
Surrogate Package

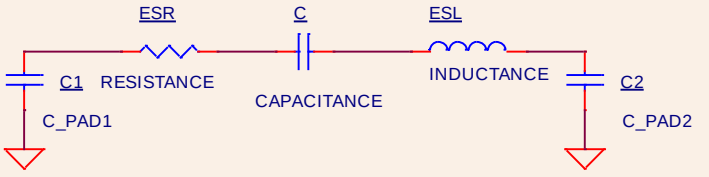
VIA

Ultra Flex Loadboard

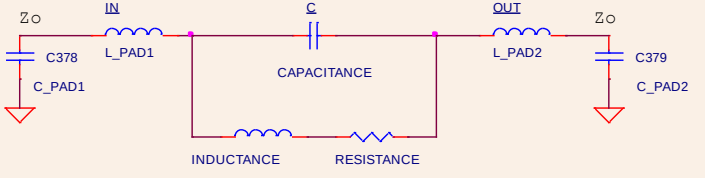
BSLB --Back Side Loop-Back

LOOP BACK DESIGN CONSIDERATION



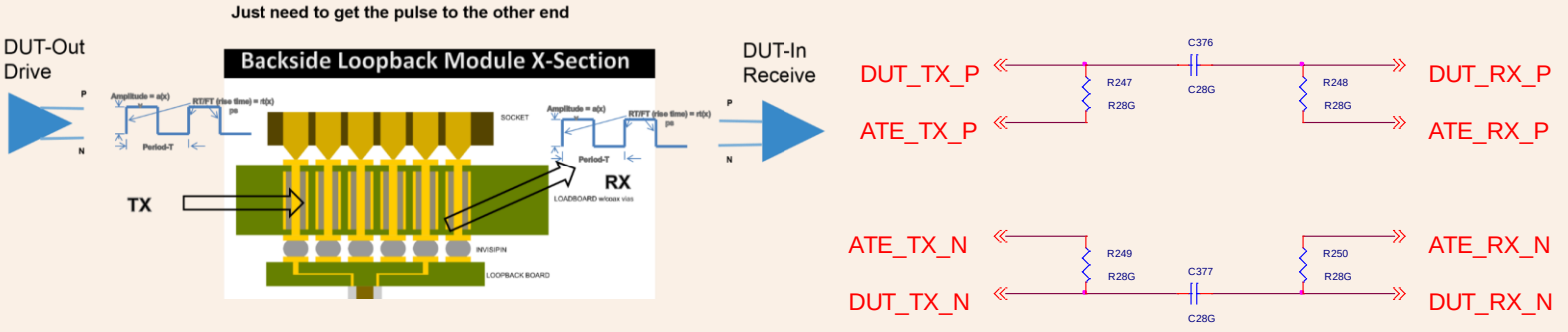


R28G Resistor equivalent circuit

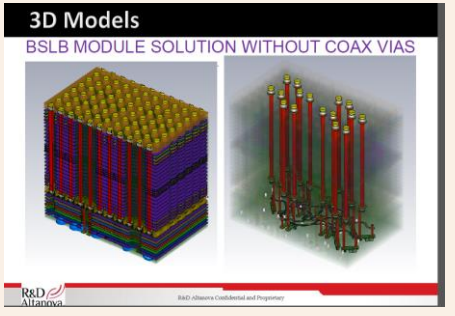


C28G Capacitor equivalent circuit

LOOP BACK DESIGN CONSIDERATION

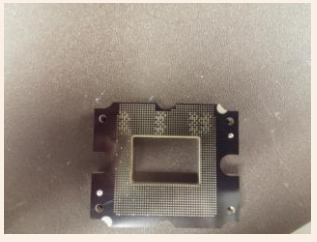


BSLB 3D Model

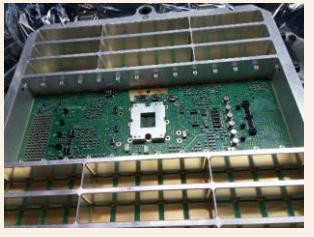


Advantages of RC over relay

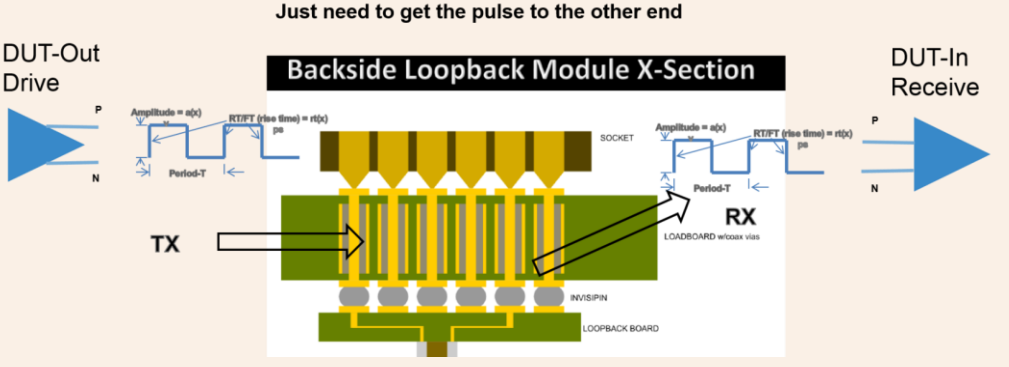
1. **Reliability**
2. Eliminate layout related issues resulting to discontinuities (component size, impedance control, via count.)
3. Enable the shortest possible trace length



BSLB Module



BSLB Module &
UltraFlex Loadboard

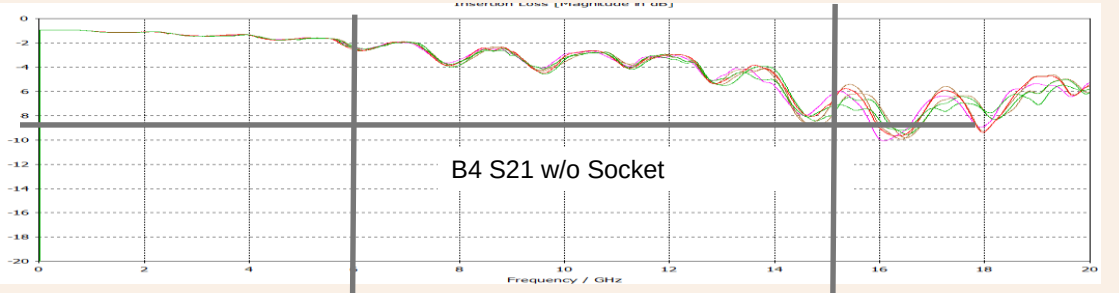


SUMMARY : (BSLB) Backside Loop Back Module Solution

1. Eliminated ~2 weeks on 16 Week fabrication schedule
2. Lower Cost compare to Embedded RC component
3. Provided option for several configuration: RC, C, Direct to ATE(No loopback)

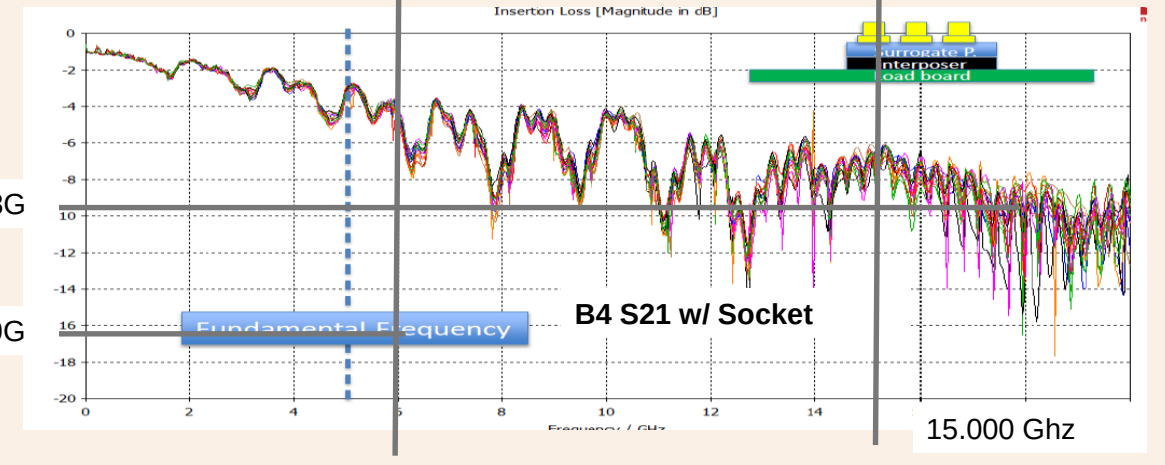
Test socket(blind built) induced performance degradation

28G



28G

10G



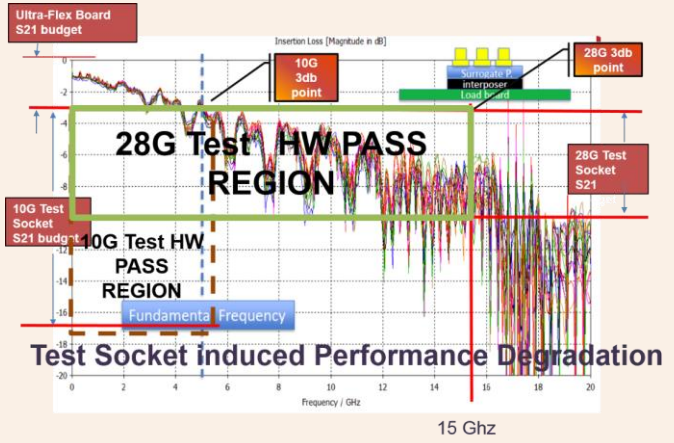
6.000 Ghz

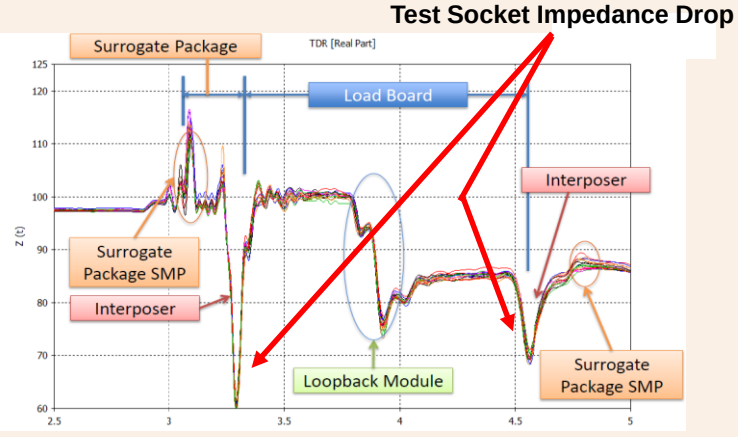
15.000 Ghz

15.000 Ghz

28G Test Hardware Signal Integrity Design

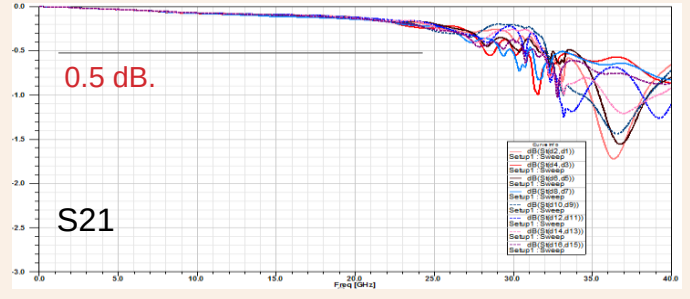
TEST SOCKET, MAJOR SOURCE OF DISCONUITY

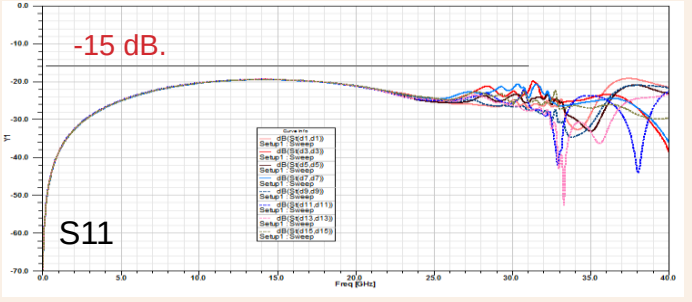




Unless measured or tested there is no assurance that a test socket for high speed SerDes I/O test impedance is ~100 Ohms differential or ~50 Ohms for single ended application.

DESIGN PARAMETERS FOR TEST SOCKET



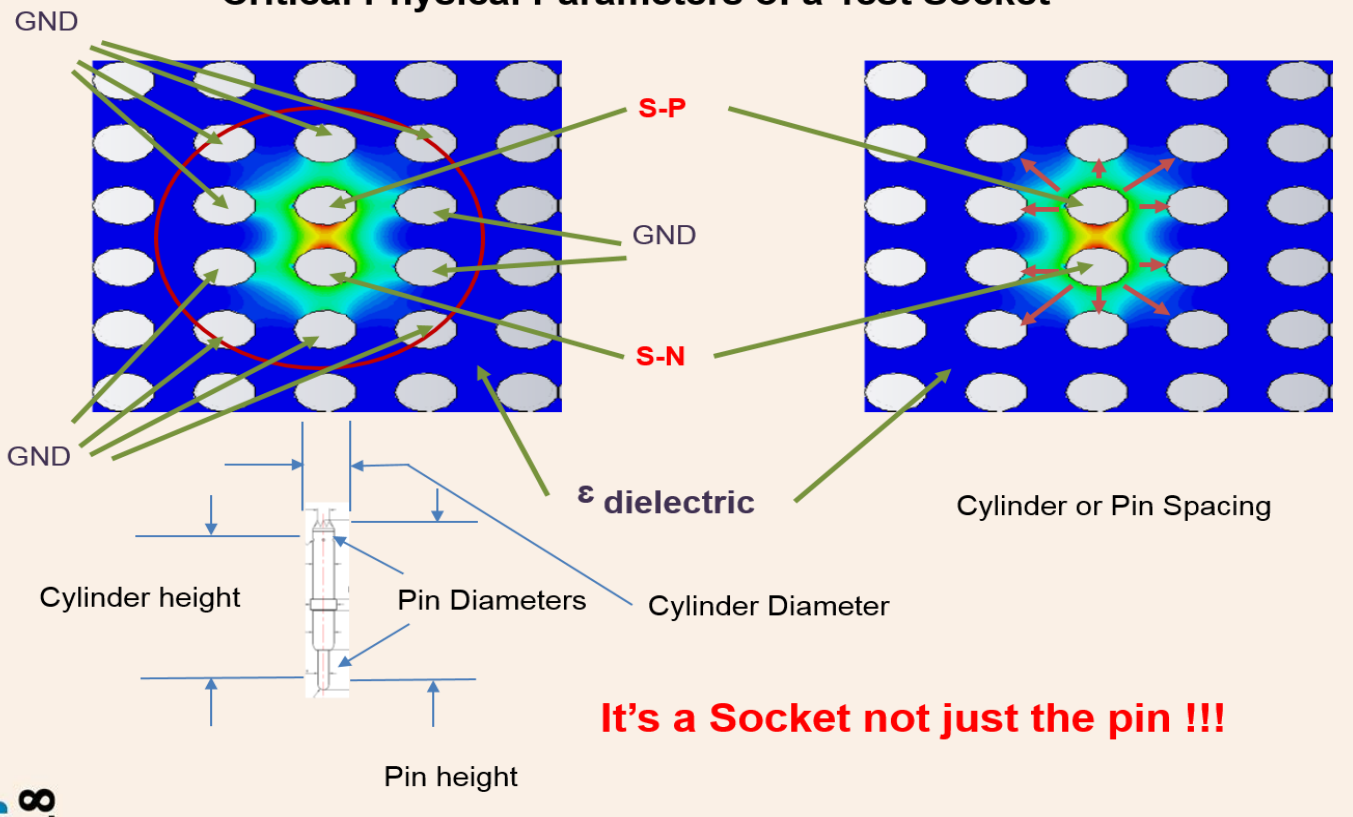


15 Ghz

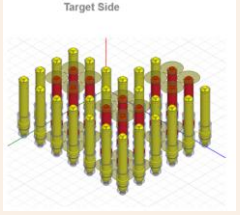
28G Test Socket Target Performance

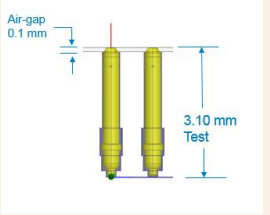
- ❑ S21 0.5 dB Point is 15 GHz
- ❑ S11 ~ (-15db) at 0.5 dB point
- ❑ SerDes Lane to Lane Correlation <0.5 dB
- ❑ Differential Impedance 100 0hms + / - 5%
- ❑ Insertion Life (i.e. 10k, 20k…500k) cycles
  - ❑ S21 degraded to -5db at 15Ghz
  - ❑ S11 (-15db) at 15 GHz
  - ❑ Differential Impedance is above 90 Ohms
- ❑ All parameters are to be measured by VNA (Vector Network Analyzer)

Critical Physical Parameters of a Test Socket

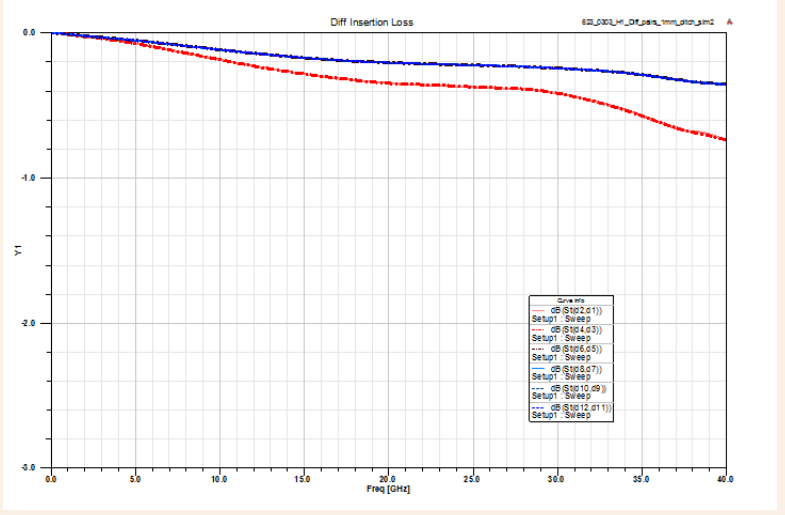


It's a Socket not just the pin !!!

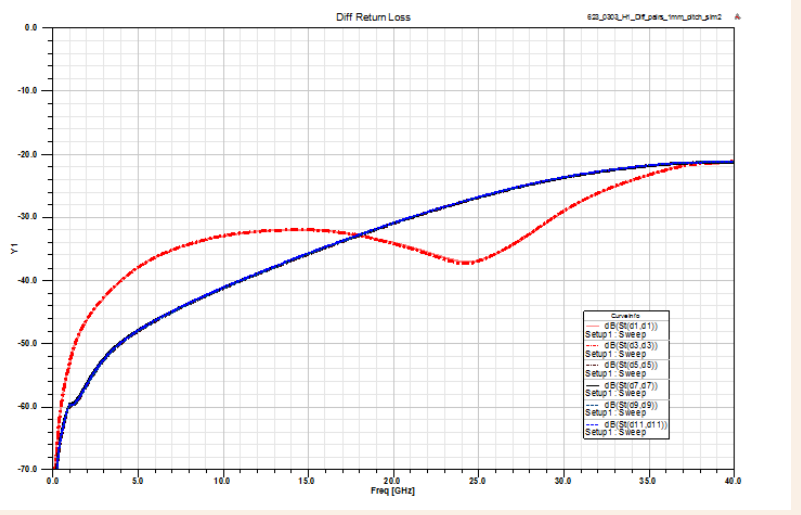




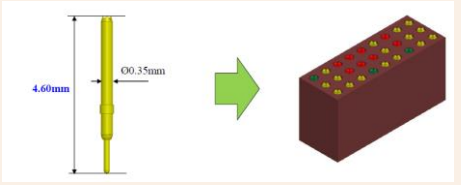
Test Socket serdes I/O Models
&
Simulation Results

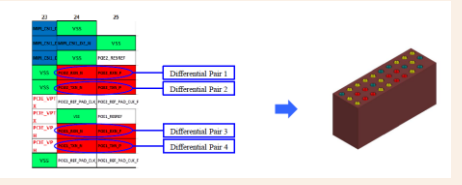


Test Socket S21 Insertion Loss



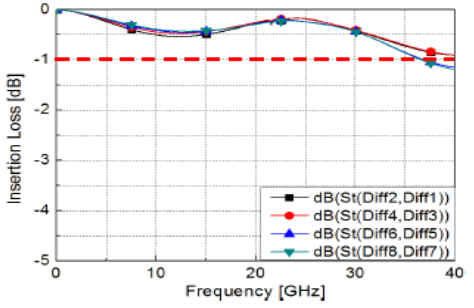
Test Socket S11 Return Loss





Test Socket serdes I/O Models & Simulation Results

<Insertion Loss>



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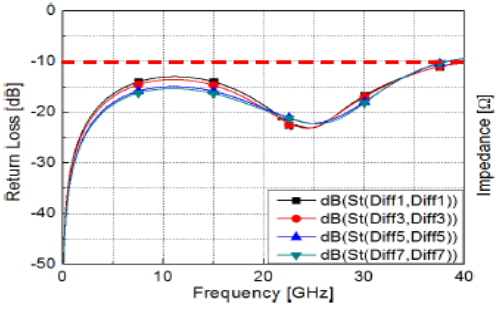
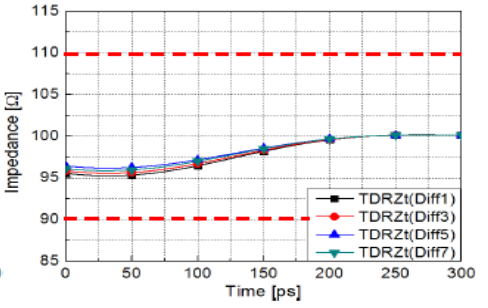


<Impedance>



Signal Pin	Insertion Loss		Return Loss		Impedance	
	@ 2.5 GHz	@ -1 dB	@ 2.5 GHz	@ -10 dB	@ Min	@ Max
Differential Pair 1	-0.08 dB	> 40.0 GHz	-21.8 dB	> 40.0 GHz	95.3 Ω	100.1 Ω
Differential Pair 2	-0.07 dB	> 40.0 GHz	-22.3 dB	> 40.0 GHz	95.6 Ω	100.1 Ω
Differential Pair 3	-0.07 dB	36.9 GHz	-23.5 dB	38.2 GHz	96.2 Ω	100.1 Ω
Differential Pair 4	-0.06 dB	36.6 GHz	-23.8 dB	38.1 GHz	95.9 Ω	100.1 Ω

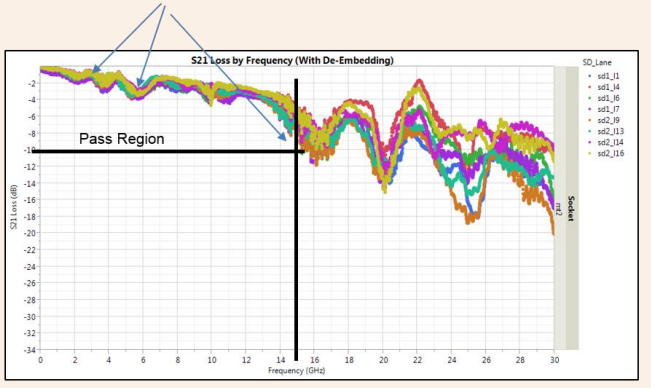
TEST SOCKET DOE SUMMARY:

1. Five test socket vendors provided prototypes 28G capable sockets for the 32 I/O device (T4): Leeno, Yamaichi, Socket-4B, Socket-4A, RDA
2. Each Socket benchmarked for S-parameters, TDR Impedance Plots, functional, parametric test. Time 0, 10K to 20K cycles
    1. Test temperature as function of typical product flow (25C, 110C, -40C)
    2. 400 Mechanical Samples, 100 known good devices use for electrical characterization for all test conditions
3. Leeno and Socket-4B vendors were selected to continue to the 16 - 28G I/O network processor (TV1). Yamaichi pursued a mechanical cycling study with NXP (50K cycles).

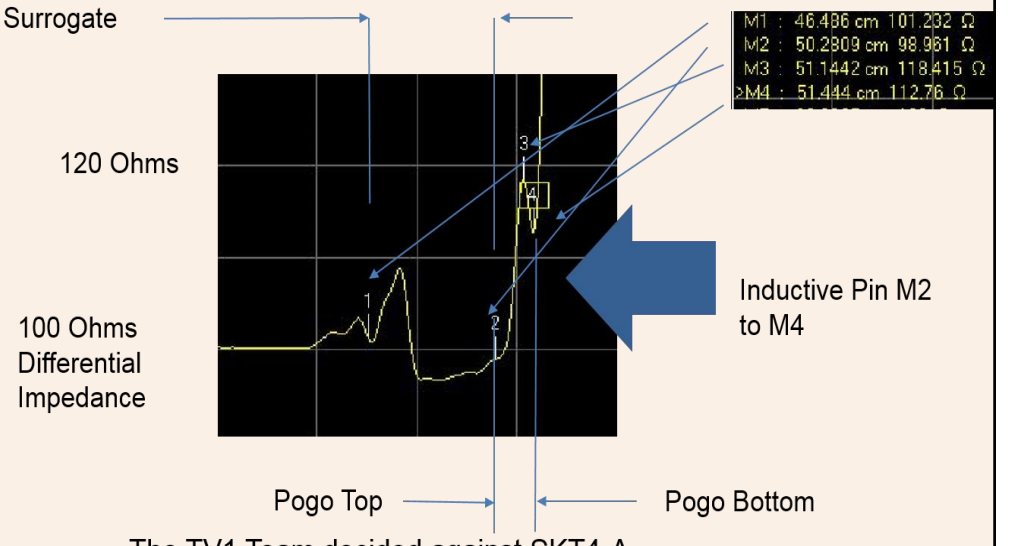
Note: This is high level summary. Socket DOE is another presentation by itself…

Case-1: Inductive test socket resulting to rippling

High level of rippling for inductive Test Socket SKT4-A



The TV1 Team decided against SKT4-A
1. High discontinuity (> 120 ohms impedance)
2. S21 failed to clear the -10db limit at 15 Ghz @ cycle=0



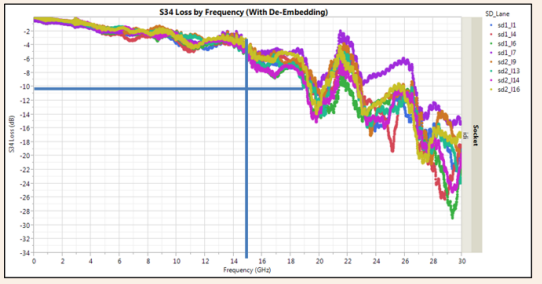
The TV1 Team decided against SKT4-A
1. High discontinuity (> 120 ohms impedance)
2. S21 failed to clear the -10db limit at 15 Ghz @ cycle=0

28G Test Hardware Signal Integrity Design

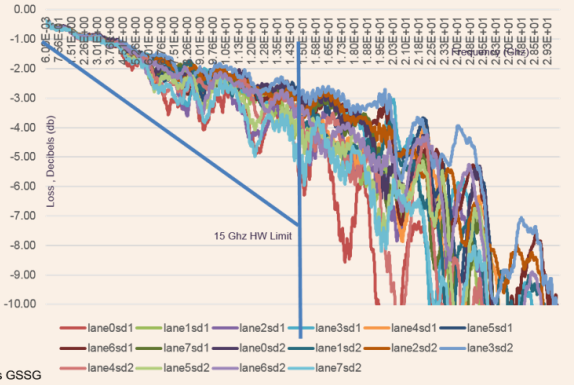
Case-2: Socket manufacturing challenges. Correlation problem between models and fabrication

Same model different performance from T4 to TV1

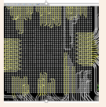
SKT4-B 28G S21 Insertion Loss Plot



SCKT4-B, TV1 LB#3 S21 Insertion Loss

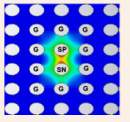


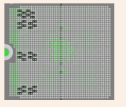
- SCKT4-B was used for 28G Characterization
- No performance issues that can be attributed to SCKT4-B degradation detected as a function of insertion
- Rippling was not a major issue at 20K cycles.



T4 Package

Differential Signal Pads GSSG

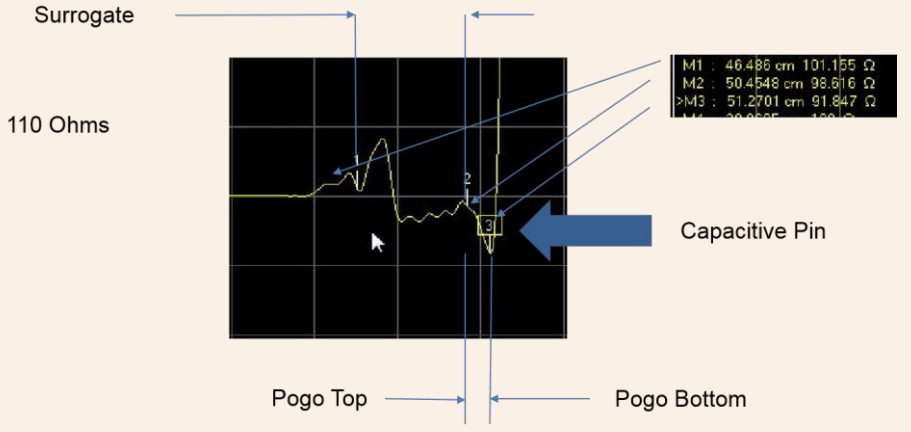


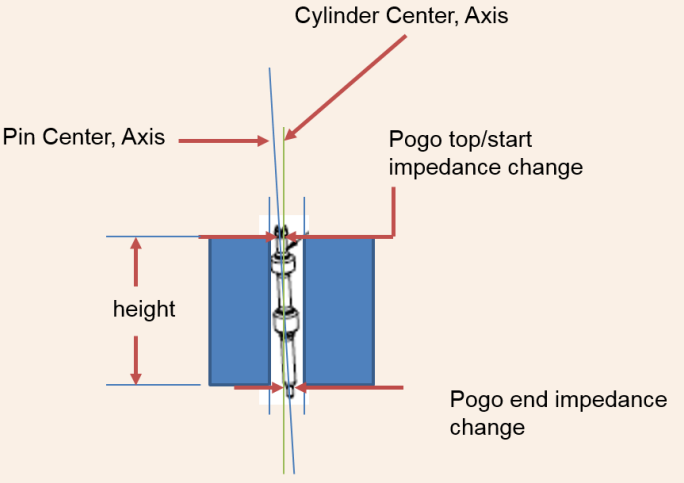


TV1 Package

Case-2: Socket manufacturing challenges. Correlation problem between models and fabrication

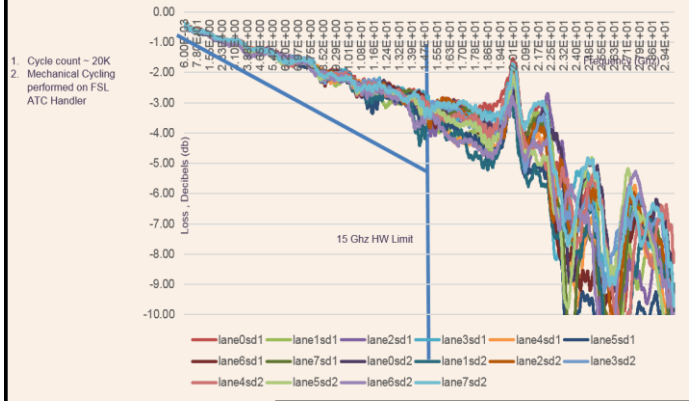
Socket SCKT4-B to TV1 conversion resulted capacitive pin

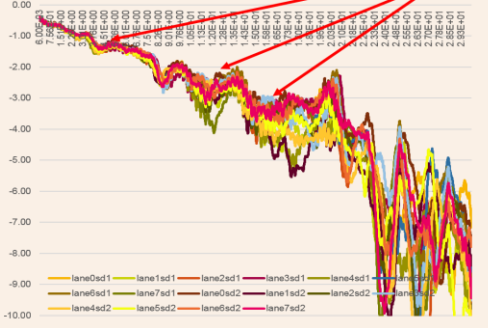


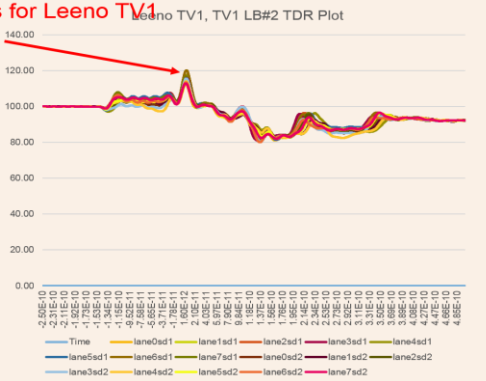


Pin wobble within the cylinder a source of discontinuity

Case-3: Correlation problem between models and fabrication







Leeno R1 TV1 Test Socket

Leeno T4 to TV1 28G Conversion challenges.. We have a case of validation and instrumentation correlation question

- TV1 R1 Models resulted to inductive pin/socket
- TV1 R2 (Change pin diameter, Change package material with better dielectric constant)

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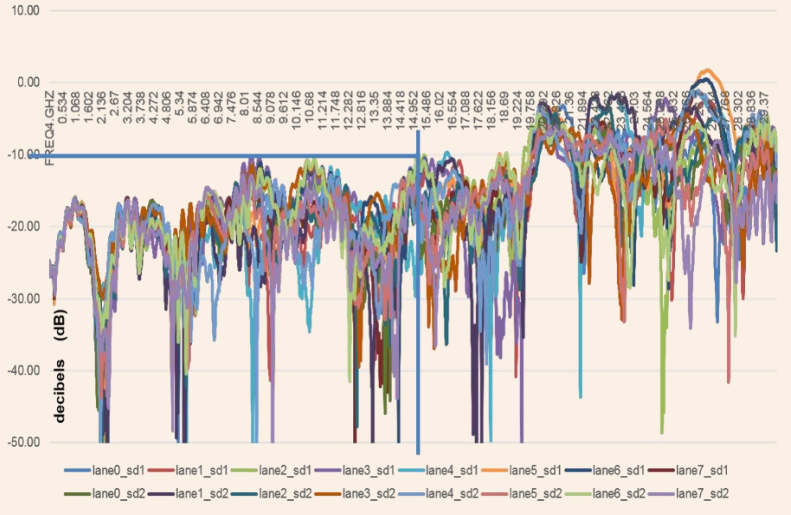
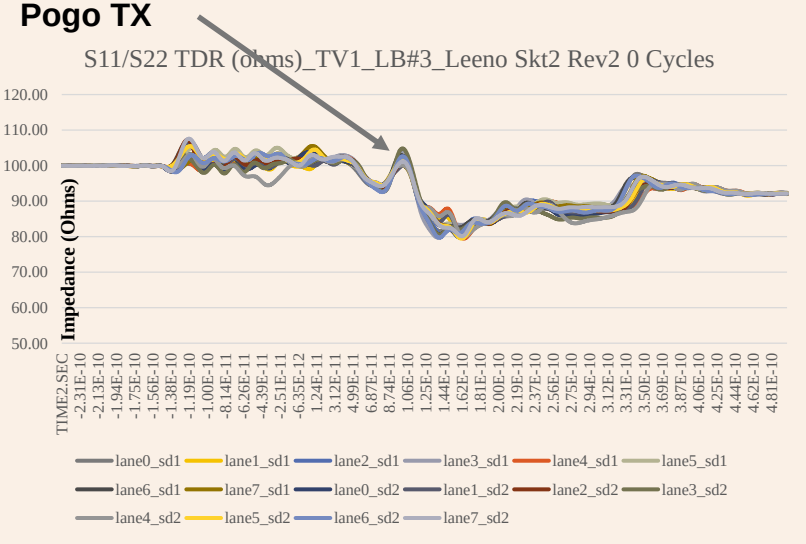
Leeno R2 TV1, S11 and Improve TDR Impedance



Pogo TX



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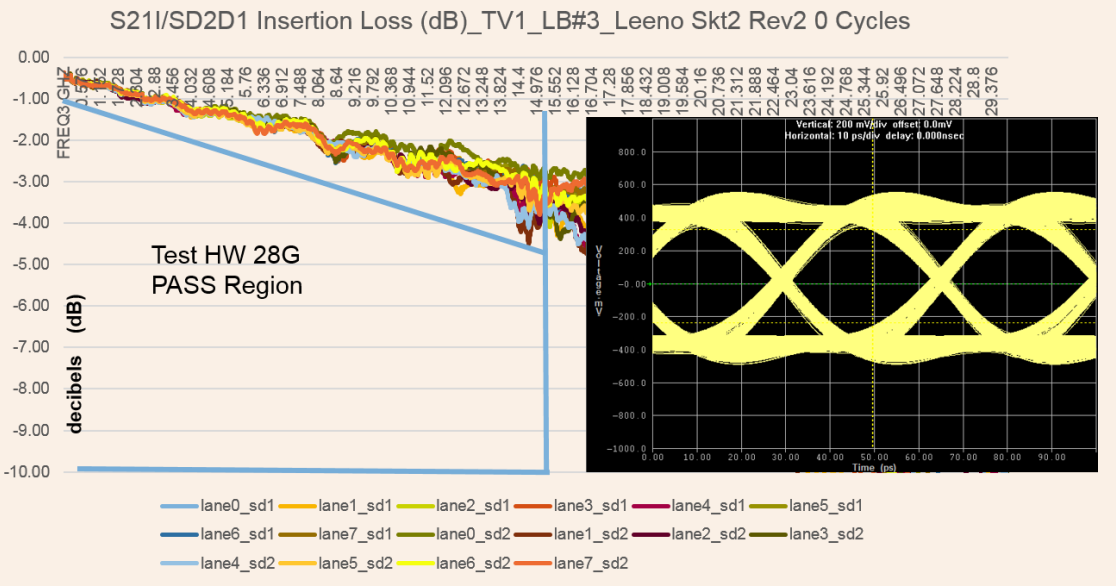
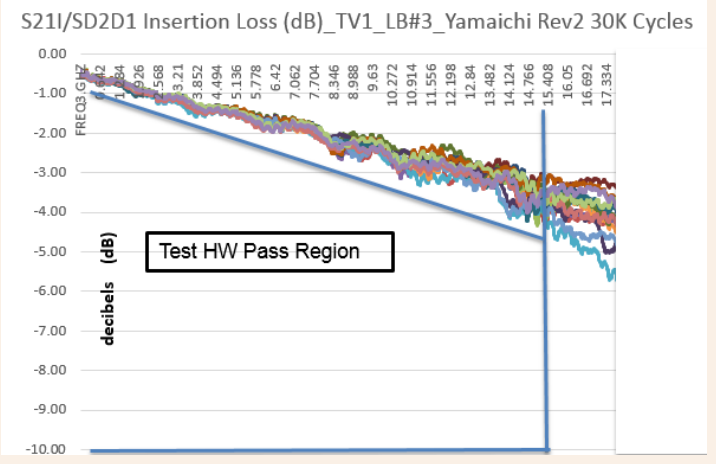
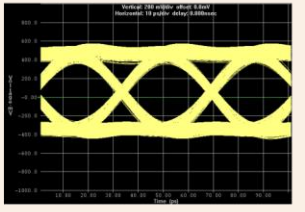


28G Test Hardware Signal Integrity Design

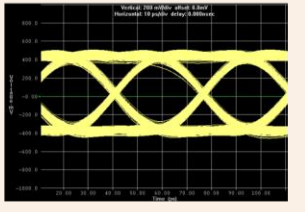
Case-4: Frequency domain performance as function of insertion cycle



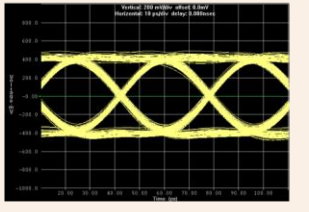
Yamaichi T4 Rev-2 Data Eye from 10K to 30K cycles



Yamaichi R2 28G, @ 30K Cycles



Yamaichi R2 28G, @ 20K Cycles



Yamaichi R2 28G, @ 10K Cycles

- Yamaichi R2 use a socket material with better dielectric
- Data eye remained in excellent condition at ~ 30K cycles
- Date eye height is affected by cycle count
- Device pass TV1 Electrical Test
- Socket, pin has not been cleaned to date

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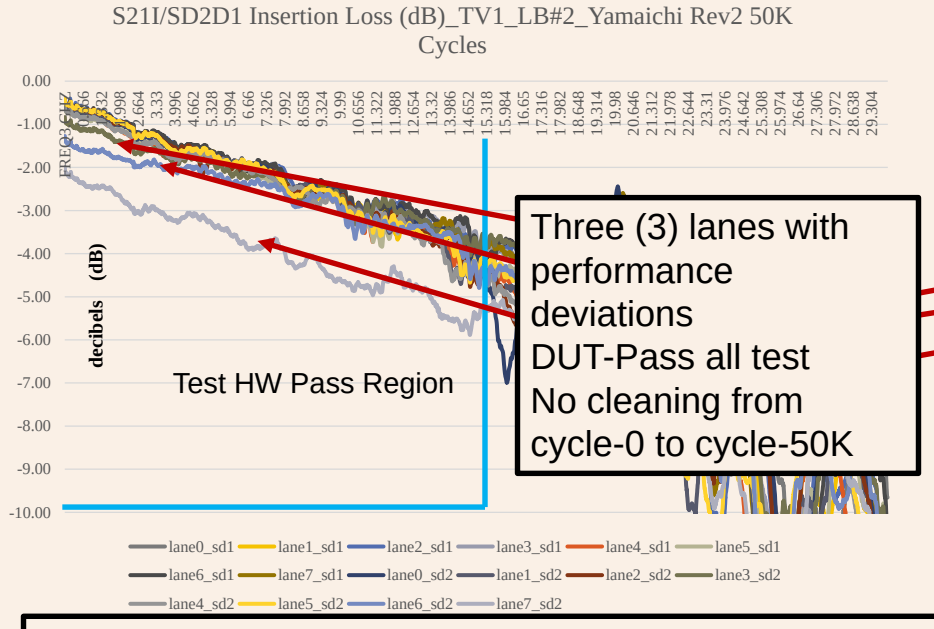
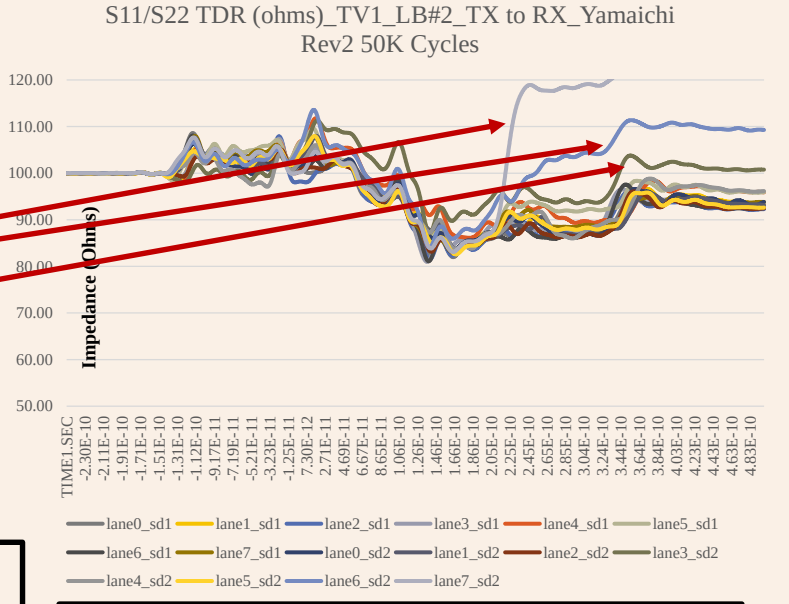
28G Test Hardware Signal Integrity Design

Performance inflection point was detected in between 40K and 50K cycles



Three (3) lanes with performance deviations
DUT-Pass all test
No cleaning from cycle-0 to cycle-50K



Frequency domain plot shows the effect of specific physical defect across frequency range. Takes out the guessing game

Time domain impedance plot will indicate specific failure on the signal path. For this case on TIP of the pogo.

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28G Test Hardware Signal Integrity Design

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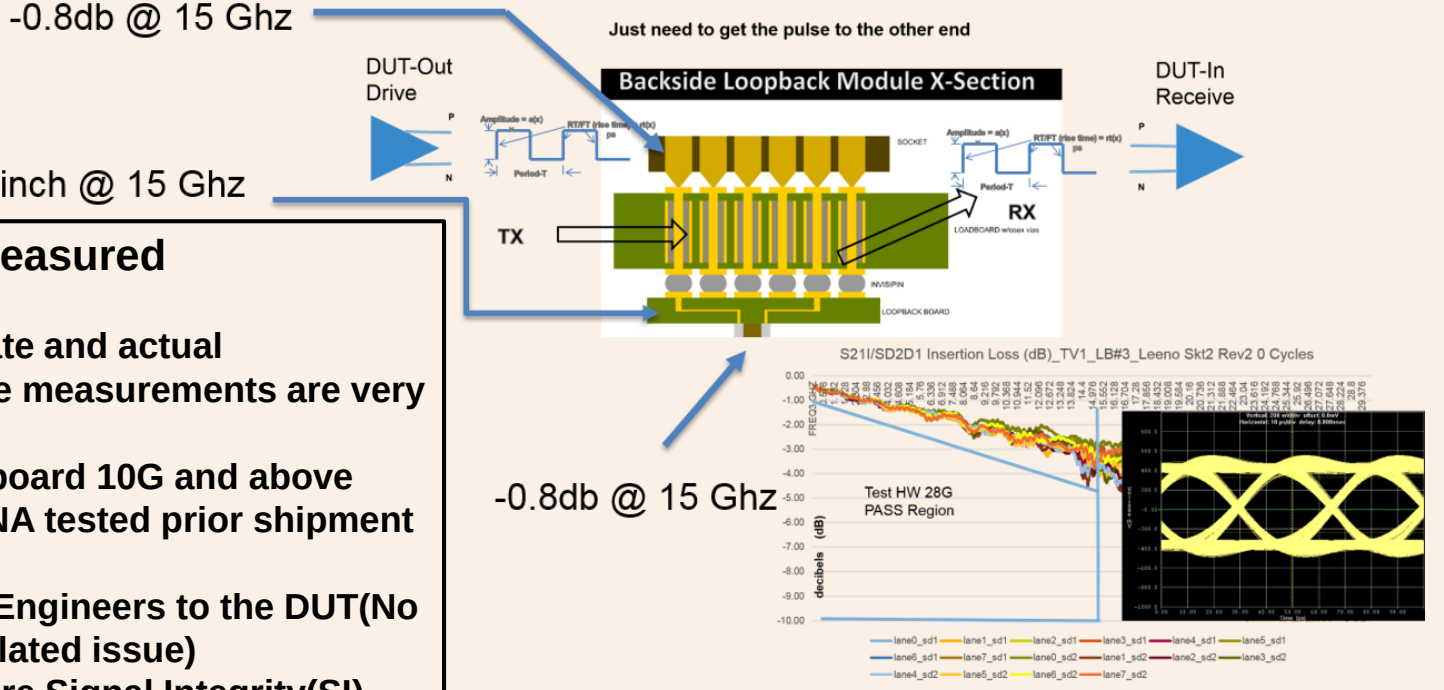

Target VS Measured

- **Loss estimate and actual performance measurements are very close**
- **All DN loadboard 10G and above (28G) are VNA tested prior shipment to NXP**
- **Focus Test Engineers to the DUT(No hardware related issue)**
- **Test hardware Signal Integrity(SI) performance ascertained before 1st silicon**

Conclusion

1. Analytical approach is highly recommended for signal integrity design for test hardware for short wavelength applications.
2. Understanding and quantitative assessment of the signal path is key to ascertain exposure to sources of discontinuity and signal loss.
3. Definition of performance budget for the Test Hardware Signal Path, in reference to DUT SERDES 28G I/O requirements, is highly recommended.
4. Performance Validation of Test Hardware for 28G I/O application and higher is a necessity. Compliance to design target performance must be confirmed not assumed.
5. PCB vendor SI capability and PCB process control is a major area for improvement in the industry .SI design models must be tied to PCB fabrication process
6. Socket vendors need to tool up for SI model and performance validation to ensure compliance of its product. Socket Vendors need VNA to validate 28G test socket performance.

References:

- Signal Integrity Simplified (Eric Bogatin), ISBN 0-13-066946-6
- High Speed Digital Design(Howard Johnson, Martin Graham), ISBN 0-13-395724-1
- Practical RF Circuit Design (Les Besser, Rowan Gilmore), ISBN 1-58053-521-6
- Production Testing of RF and System on a Chip(SOC) for wireless Communications(Keith B. Schaub, Joe Kelly), ISBN 1-58053-692-1