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Key Drivers for SLT (System Level Test)

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ASTRONICS TEST SYSTEMS

Agenda

- What is System-Level Test (SLT)?
- How is SLT done today?
- What are the trends driving need for more SLT?
- What are the key challenges and opportunities?

What is System-Level Test (SLT)?

- **Application-specific functional tests that are performed**
  - on an IC Device Under Test (DUT)
  - which is temporarily placed in a socket while SLT tests are applied
  - to help "guarantee" that a device will meet its targeted specs and performance goals when it is ultimately used in the final system.

- **System includes both hardware and software**
  - Hardware – Device Under Test (DUT), sockets, application boards, power supplies, etc.
  - Software – firmware, device drivers, operating systems, applications, etc.

System-Level Test ensures that the device is tested similar to the end user experience

What is System-Level Test (SLT)?

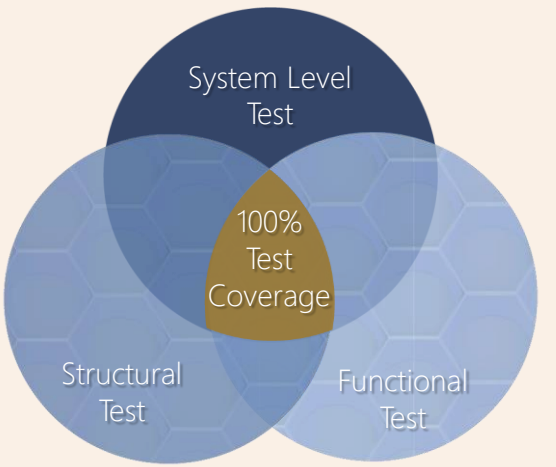
- **2 perspectives … component vs system**
  - Component perspective - does the device meet its specs?
  - System perspective – does the "system" work when all the DUTs are combined with software at the board level?

System-Level Test ensures that the device is tested similar to the end user experience

How is System-Level Test Done Today?

A Brief History of Time…

- Functional Test used to be the way to go
  - *then designs started to get more complex*
- Structural Test emerged; improved fault coverage
  - *device complexity continued to increase, quality became important as well (hardware & software working together)*
- System-Level Test is emerging to insure optimal performance of the integrated system
  - *but how do we afford it?*



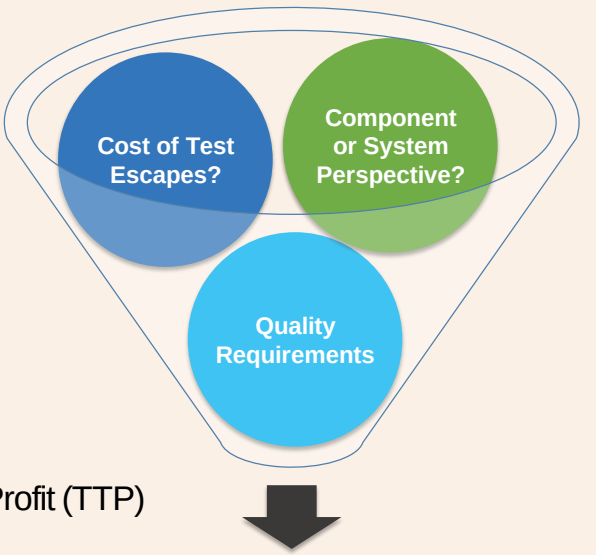
Mesh of SLT, structural and functional test leads to maximum test coverage

How is System-Level Test Done Today?

Key Considerations

"How much SLT" is determined by:

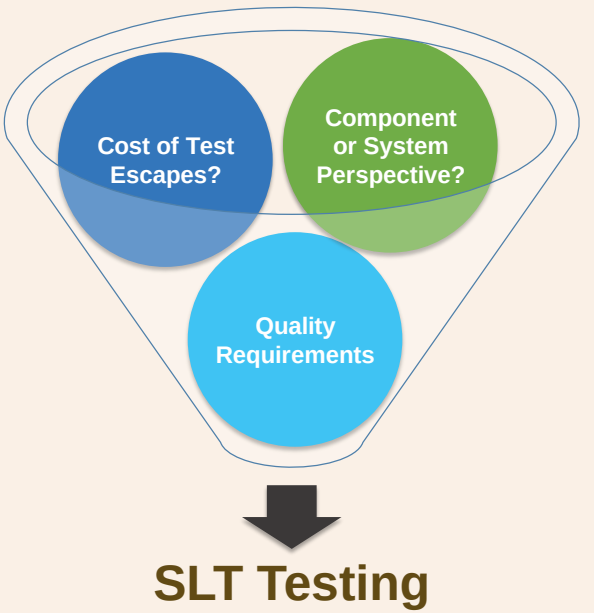
- "Component" or "System" perspective not covered by ATE
- Importance of hardware and software interactions
- Volume, Market segment, Product Life Time
- Product Quality and Reliability Requirements
- Thermal Requirements
- Time-to-Market (TTM), Time-To-Volume (TTV), Time-To-Profit (TTP)
- Cost of test escapes
- End Market Requirements (i.e., safety)



How is System-Level Test Done Today?

Other Considerations for SLT

- Test Time: seconds, minutes, hours
- Purpose: for TTM, qualification, production
- Tester:
  - "SLT on ATE"
  - "SLT specialized equipment"
  - "SLT Massively Parallel"



How is System-Level Test Done Today?

Examples of equipment used today

SLT on ATE

SLT on custom hardware

Low Parallel SLT

Massively Parallel SLT

Cost per DUT

Volume

Increasing SLT Unit Volume

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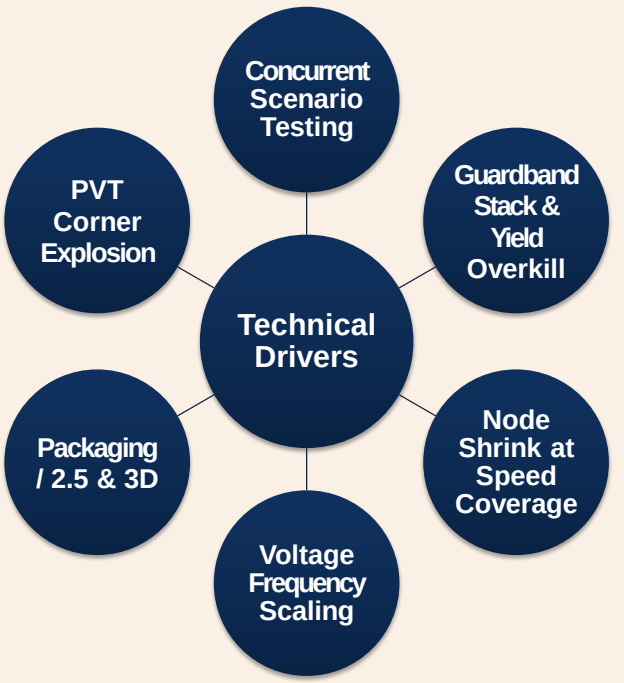
What drives increasing need for more SLT?



Key Drivers for SLT (System Level Test)

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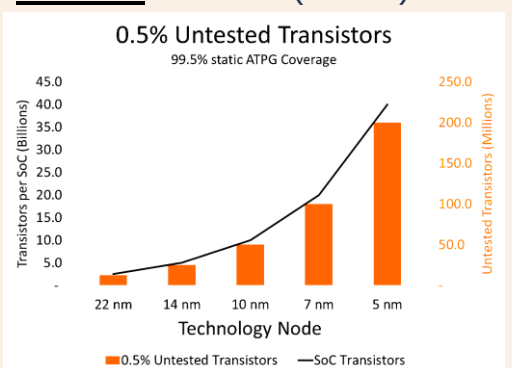
Lower technology nodes dramatically increase number of ***untested*** transistors

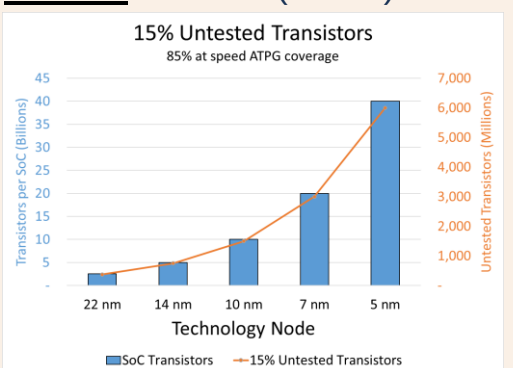
Moore's Law doubles transistor count every technology node

of Untested Transistors increasing:

At 99.5% coverage (static ATPG)
Millions untested (10 nm)



At 85% coverage (at speed ATPG)
Billions untested (10 nm)



Concurrent Scenario Testing: real-world scenarios

Consumer DUT **Automotive Infotainment DUT** **Medical Pacemaker DUT**

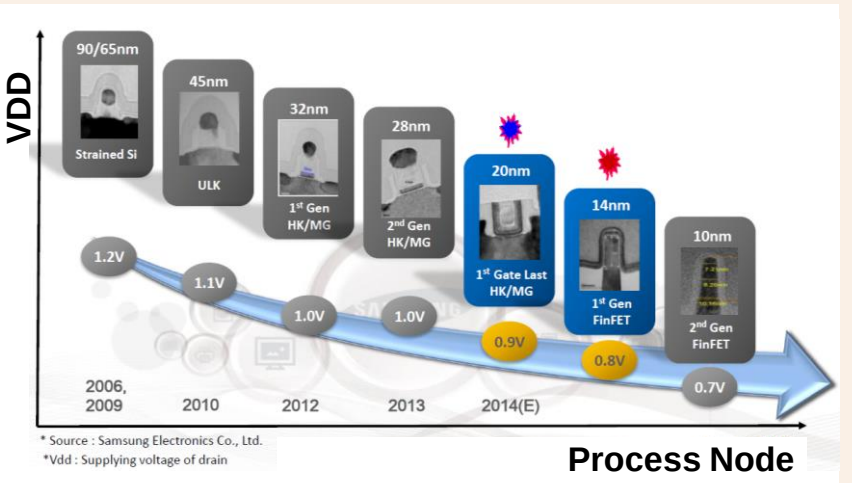
Production ATE: Replicating real world scenarios: **MONTHS**

System-Level Test: Replicating real world scenarios: **MINUTES**

How to generate test patterns for these scenarios without significant overkill?

Guard Band Stack and Yield Overkill

- **Definitions**
  - **Guard Band** added margin for worst case / ATE test
  - **Headroom** = VDD (Supply Voltage) / CMOS threshold (turn on voltage



Source: Samsung

SLT can help reduce the "fear of throwing away good parts" that comes with lower nodes

Guard Band Stack and Yield Overkill

With lower nodes, Guard Band becomes a higher percentage of VDD, "eating into the headroom"

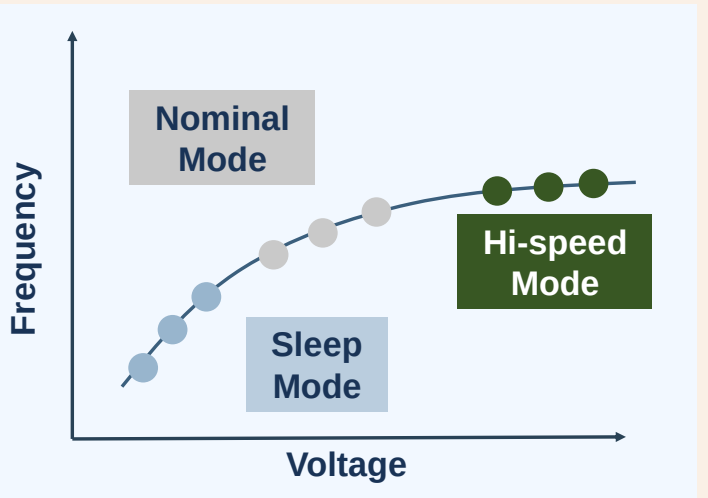
Technology Node (nm)	Vdd (V)	100 mV Guardband as a % of Vdd	CMOS Threshold (V)	Headroom Vdd- Threshold (V)	100mV Guardband as % of headroom
90	1.4	7.1%	0.5	0.9	11.1%
65	1.2	8.3%	0.5	0.7	14.3%
45	1.1	9.1%	0.5	0.6	16.7%
28	**1**	**10.0%**	**0.5**	**0.5**	**20.0%**
20	0.9	11.1%	0.45	0.45	22.2%
14	**0.8**	**12.5%**	**0.4**	**0.4**	**25.0%**
10	**0.7**	**14.3%**	**0.4**	**0.3**	**33.3%**

Assume: 100mV Guard Band (could also be ~100MHz Guard Band)

SLT can help reduce the "fear of throwing away good parts" that comes with lower nodes

DVFS Explosion + PVT Corners

- **Dynamic Voltage Frequency Scaling (DVFS)**
  - Ensures the DUT works at different power conditions by simulation and testing of each power situation
- **Process Voltage Temperature (PVT) Corners**
  - Addresses process and temperature variations with simulation and testing

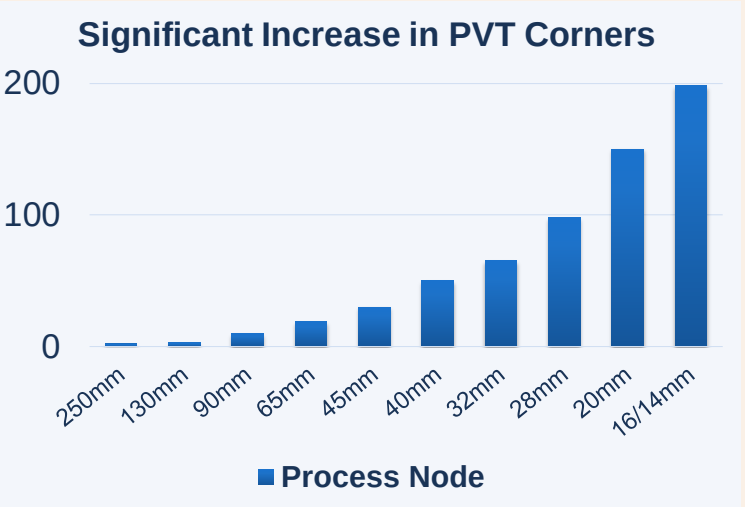


Without SLT, it is difficult if not impossible to test all scenarios!

DVFS Explosion + PVT Corners

Designers lack time to compensate for the DVFS and PVT Corner Explosion: there isn't enough test time to run all the patterns!

SLT offers the advantages of booting and running the DUT natively in different voltage modes, simulating end user experience



Source: Mentor

Without SLT, it is difficult if not impossible to test all scenarios!

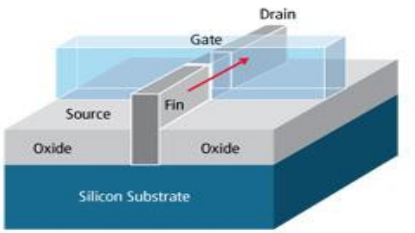
Conventional Test Methods No Longer Catch Fails

3D process geometries are driving new defect types that aren't covered by static ATPG*, at speed ATPG (TDF**), and other test methods

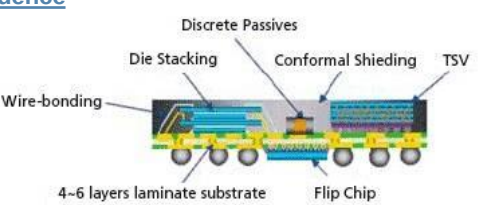
IPs from different vendors: coverage was easier with one IP.

High speed, bidirectional interfaces have faster read/write turnaround times than the latency of ATE

*ATPG – Automatic test pattern generation for structural test



FinFET Cross Section
Source: Cadence



SiP Module Cross Section
Source: ASE Group

System-Level Test screens for these fail mechanisms

Challenges and Opportunities

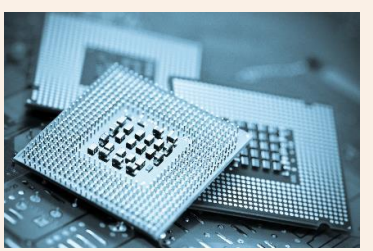
Challenges

- Lack of fault coverage metric to assess SLT effectiveness
- Complex nature of System-Level Test Failures makes it difficult to diagnose root cause of failures
- SLT Equipment Challenges
  - No “one size fits all”
  - Correlation between SLT and ATE
  - Cost to add SLT
  - Limited throughput
  - Large form factors

Being Addressed with Massively Parallel SLT

Opportunities

- More systematic approaches to create “commonality”
- Ecosystem of standards, tools, and equipment for efficient SLT flow
- Close the loop with Data Analytics



Summary: Why is more SLT needed?

- ✓ We need higher yield!
- ✓ My customers demand quality!
- ✓ My new 3D packaging prevents using certain test modes
- ✓ Our TTM and TTV ramps are fast but our test pattern generation is slow
- ✓ People's lives depend on us!

More SLT

- Marginal defects
- PVT Corners
- Mission Test
- Concurrent Scenarios
- Guard Band Overkill
- High Speed Buses
- Complexity

Less SLT

- Cost of SLT
- Lower quality targets

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Reference

For additional information about SLT, please see our whitepaper at:

https://www.astronics.com/test-systems/whitepaper-system-level-testing-for-semiconductors