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Optimal Platform Design and Analysis for High Speed I/O Electrical Validations

Xiao-Ming Gao
Intel Corporation

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Agenda

- High speed I/O EV platform design challenges
- Optimal PCB stackup selection
- High speed connector footprint optimization
- Post layout SI analysis
- Measurement data and simulations correlations
- Summary
- Q & A
- Acknowledgments

High speed I/O EV platform design challenges

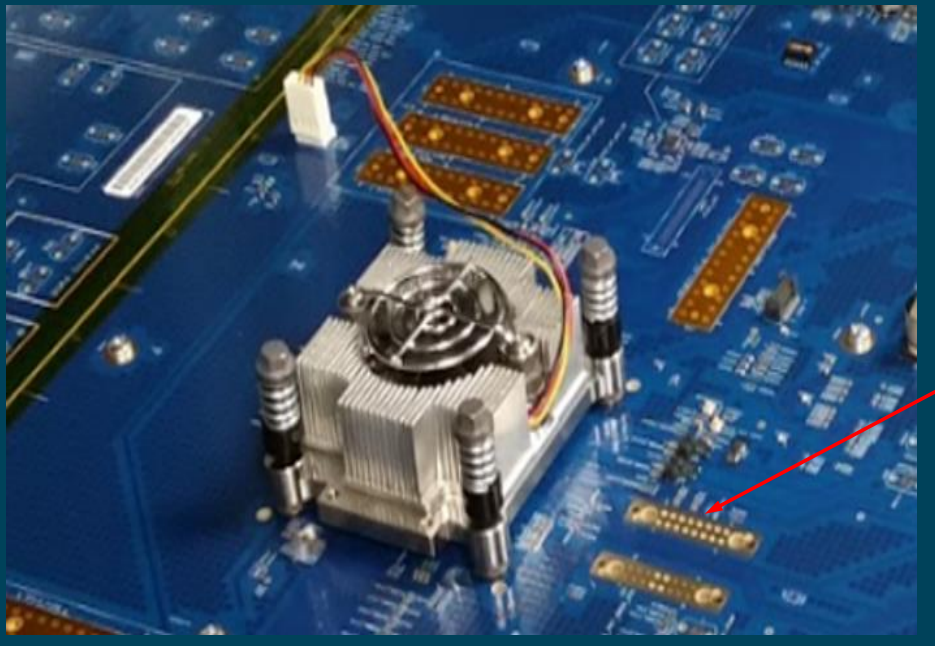
- HSIO speed is surpassing 20 Gb/s and marching towards 100 Gb/s.
- Platform interconnect components are not able to scale well as the silicon.
- Thermal, mechanical, and automation testers are all pushing testing points further way from the silicon.
- PCB material selections further limit the platform performance.

Optimal PCB stackup selection

Layer	Cu Weight		
1	.5 oz	Top Layer	
		Prepreg	Megtron 6
2	0.5 oz	GND	
		Core	Core Megtron 6
3	0.5 oz	Signal	
		Prepreg	Megtron 6
4	0.5 oz	GND	
		Core	Core Megtron 6
5	0.5 oz	Signal	
		Prepreg	Megtron 6
6	.5 oz	GND	
		Prepreg	Megtron 6
7	0.5 oz	Signal	
		Core	Core Megtron 6
8	0.5 oz	GND	
		Prepreg	Megtron 6
9	0.5 oz	Signal	
		Core	Core Megtron 6
10	1 oz	GND	
		Prepreg	Megtron 6
11	2 oz	Power	
		Core	Core Megtron 6
12	2 oz	Power	
		Prepreg	Megtron 6
13	1 oz	GND	
		Core	Core Megtron 6
14	0.5 oz	Signal	
		Prepreg	Megtron 6
15	0.5 oz	GND	
		Core	Core Megtron 6
16	0.5 oz	Signal	
		Prepreg	Megtron 6
17	.5 oz	GND	
		Prepreg	Megtron 6
18	0.5 oz	Signal	
		Core	Core Megtron 6
19	0.5 oz	GND	
		Prepreg	Megtron 6
20	0.5 oz	Signal	
		Core	Core Megtron 6
21	0.5 oz	GND	
		Prepreg	Megtron 6
22	.5 oz	Bottom	

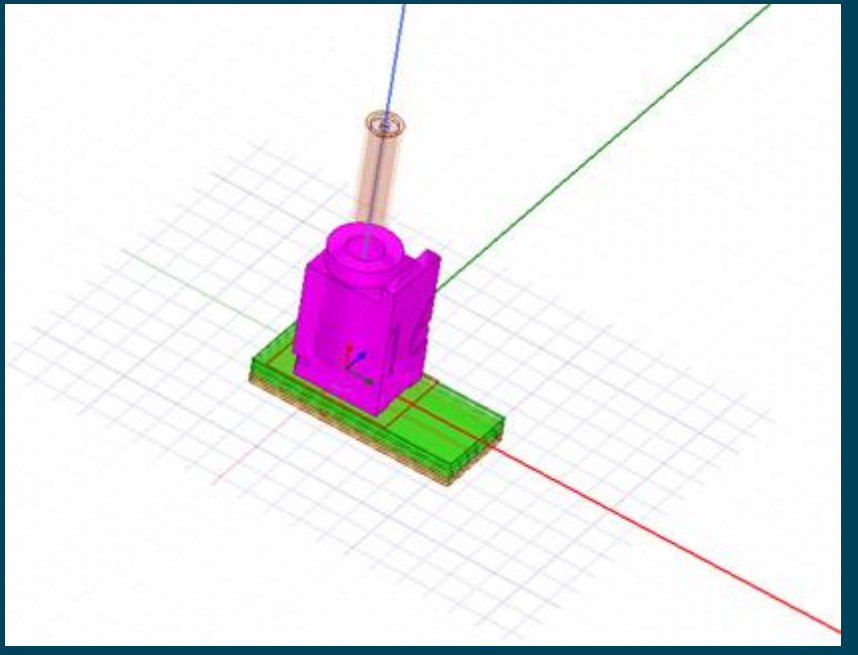
Finished Thickness: 118 mils

High speed connector footprint optimization



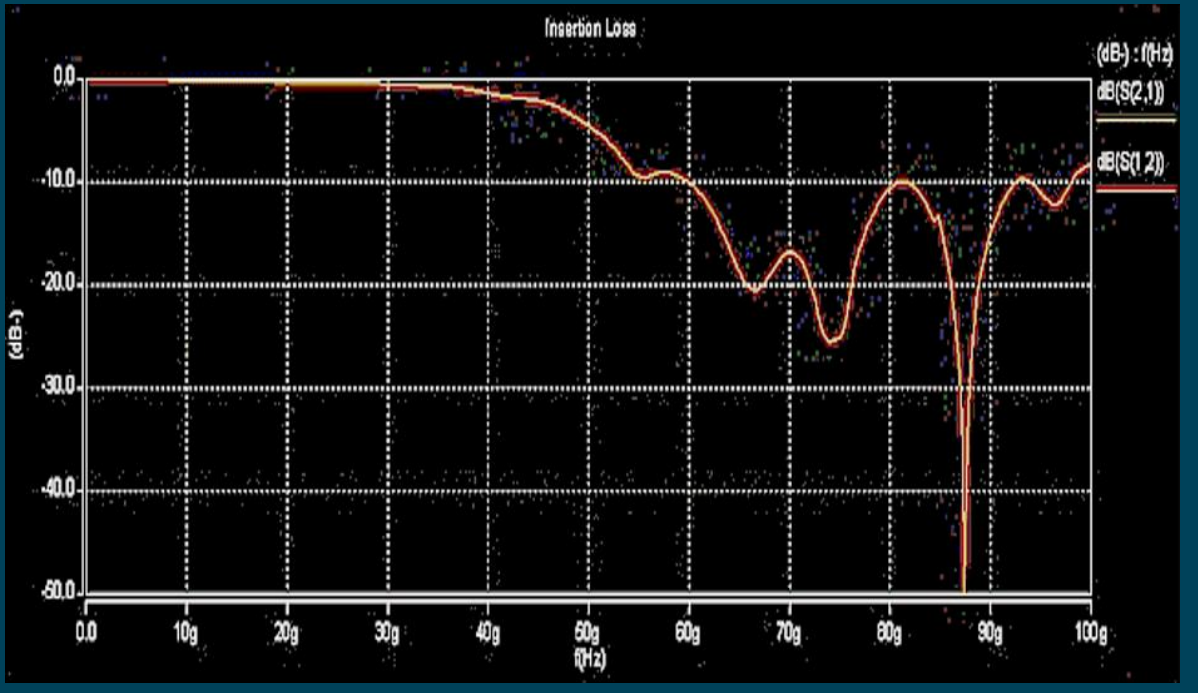
* Connector of Ardent Concepts.

Connector footprint optimization



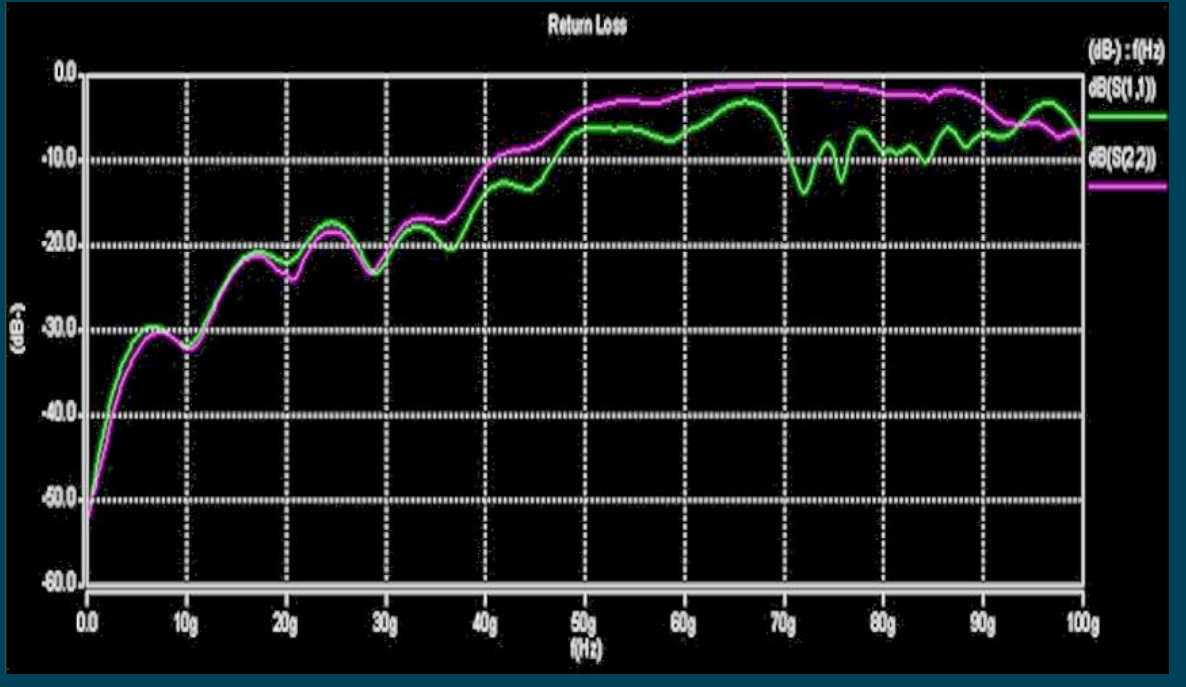
PCB board and connector pad stack co-optimization

Optimized connector performance



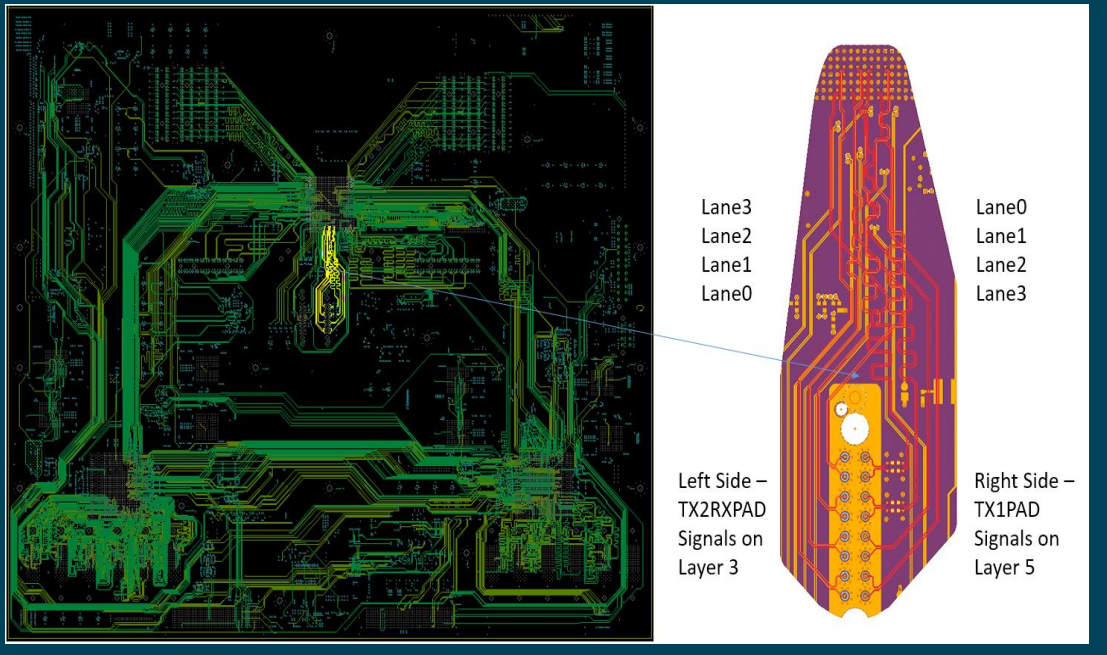
Insertion loss

Optimized connector performance



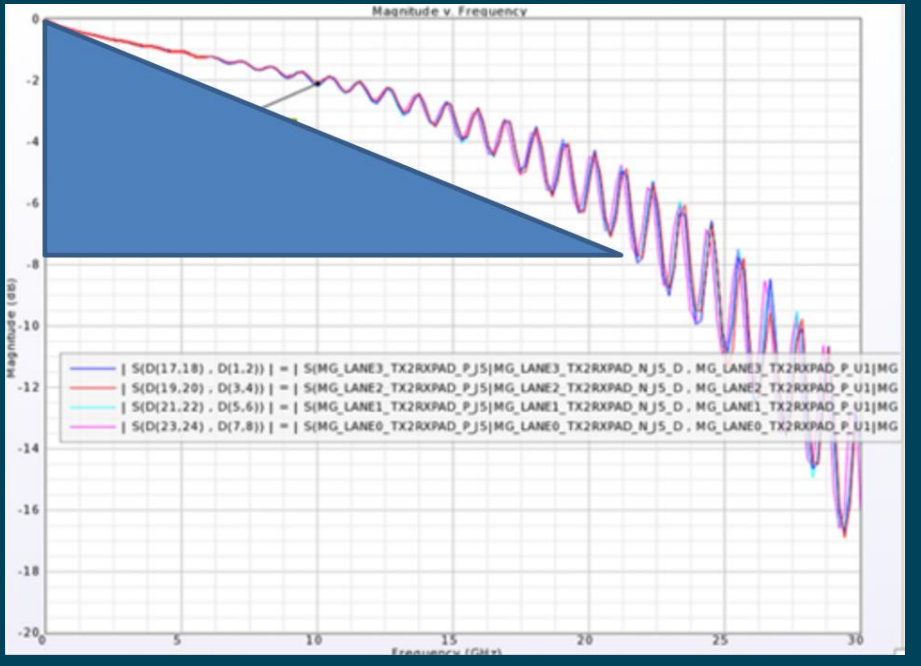
Return loss

Post layout SI simulation



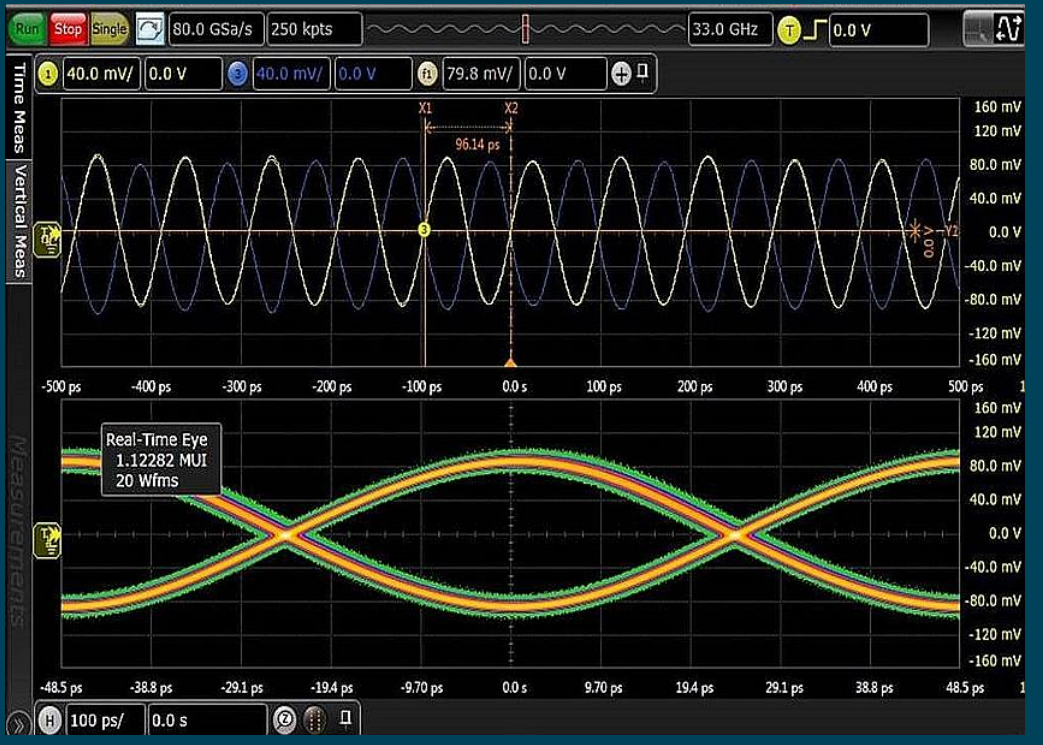
High speed I/O layout extraction

HSIO channel performance

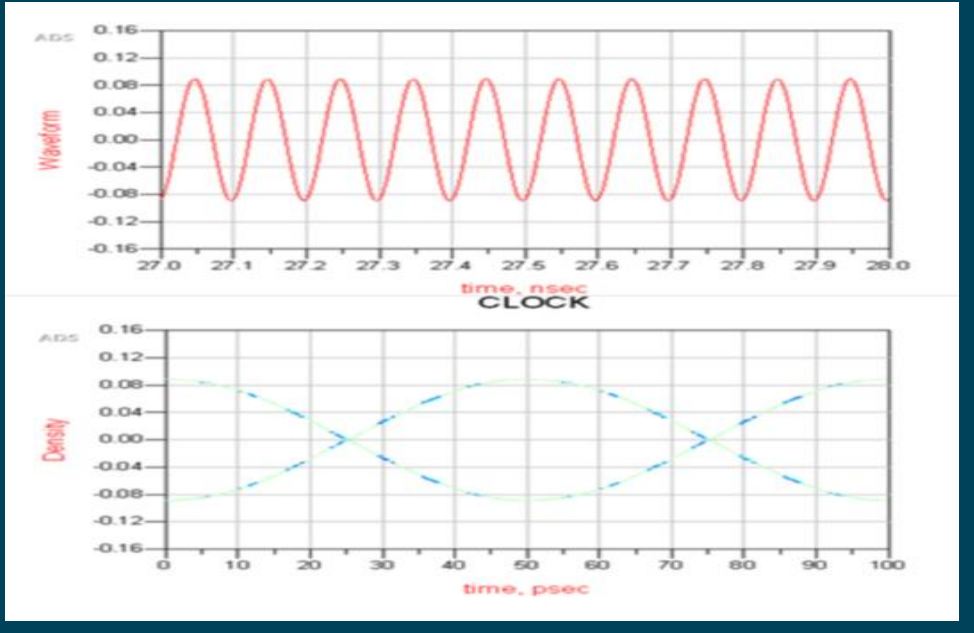


High speed I/O channels insertion loss

Measurement data



Correlations with SI simulations



Full channel SI simulation

Summary

Key areas of optimal high speed platform designs:

- Low loss PCB stack up definition
- High speed connector footprint optimization
- Post layout SI simulation
- Measurement data and correlation

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