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Design & Implementation of Universal or Common BIBs Methodology

Krishna Mohan Chavali
Sivakumar Pasupathi
GLOBALFOUNDRIES

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ABSTRACT

- The cost of burn-in boards (BIBs) are a major component of Technology Qualification budget.
- The Cost of BIBs is significantly high due to:
  - Increase in size, density and complexity of the Chips.
  - Higher Voltage & Temperature requirements.
- Dedicated BIBs for each device will be repetitive spending.
- With early planning at TQV* design, it is possible to design Universal BIBs for at least 2-3 Devices.

*TQV: Technology Qualification Vehicle

INTRODUCTION

- Cost of BIBs for EFR* & HTOL is significantly high.
  - Due to huge sample size for EFR from 3 or more lots
  - Continue to 1000hrs for HTOL qualification.
- Presents different techniques, guidelines or methods
  - For design & implementation of common / UBIBs.
  - That can be used for 2 or more devices.
- Explores on System-wise compatible UBIBs.
- SRAMs are used as example devices for UBIBs.

*EFR: Early Failure Rate

Prior Requirements

The Universal/common BIBs, can be designed for different devices.

- The devices to satisfy below minimum requirements:

Same Package: As sockets on UBIBs will be same, all the devices to have:

- Same package type & number of package pins
- Same Package dimensions (POD*).

Same Package Assignments: Package pin assignments are:

- Known prior to designing of the UBIBs and preferably be same.

*POD: Package Outline Dimensions

UBIB Design Guidelines: Power Supplies

1. **Power Supplies:** UBIBs to be designed with
   - Maximum number of supply voltages/ PSUs required
   - Out of the 2~3 devices that are to be used.
     - Device Power supply needs < PSU's of the UBIBs design.

- Converse is not true:
  - Device that needs more PSU can't use BIBs with less PSU's

Guidelines – Address & Signals

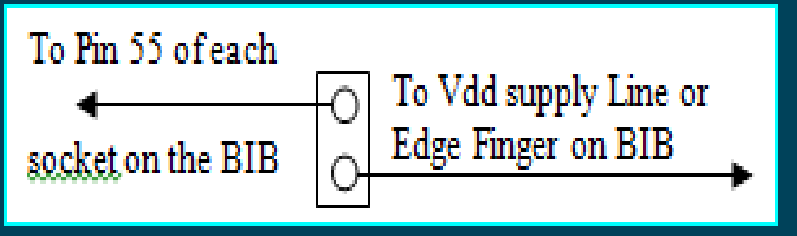
2. Address & Signal Lines:

- UBIBs to have maximum number of Channels connected.
- Out of the 2 or 3 devices that are to be used.
- Device Channel needs < # of Channels UBIBs designed for.
- Exchange of Address/Data/Control signals is possible
  - Provided BIB has Scramble Connector Option &
  - Additional signal lines are available.

3. Use of Jumper Options -1

(a) Two Header Jumper Option:

- In case of one of the device pins, need to be floated while others require a connection.
- This is resolved using a two header jumper with either “NC” or “Connect To” for that device.



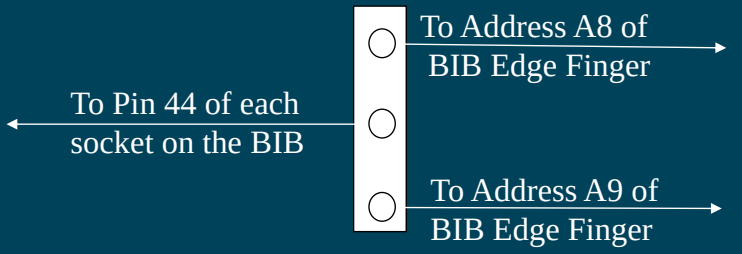
With the above arrangement made, for:

- For Device-1 to float: Keep the Jumper Open.
- For Device-2 to connect to VDD: Short jumper to get connection to Vdd

Jumper Option - 2

(b) Three Header Jumper Option:

- One of device pins (supply, IO, Control) requires a different connection Vs other devices.
- This be resolved using a three header jumper option as shown below:



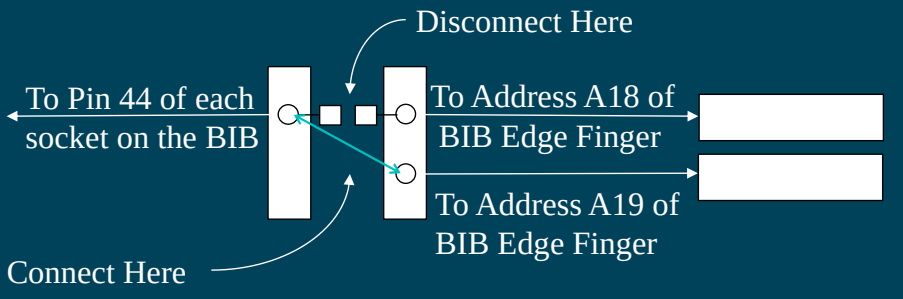
With the above arrangement made:

- To use Device 1: Keep the Jumper Open, which satisfies the condition for that device.
- To use the Device 2: Short Upper Jumper, this gives a connection to “A8” for that device.
- For the Device 3: Short Lower Jumper, which gives a connection to by “A9” for that device.

Channel Scrambler Option

4. Use of Channel Scrambler Option: To make boards compatible for more device

- It is good practice to have the Scrambler & Pad Connection Option on the UBIBs.
- Other new devices with same pinouts and satisfies the supply requirements of existing BIBs.



Option can be modified for new devices compatible, requires additional changes on the connections.

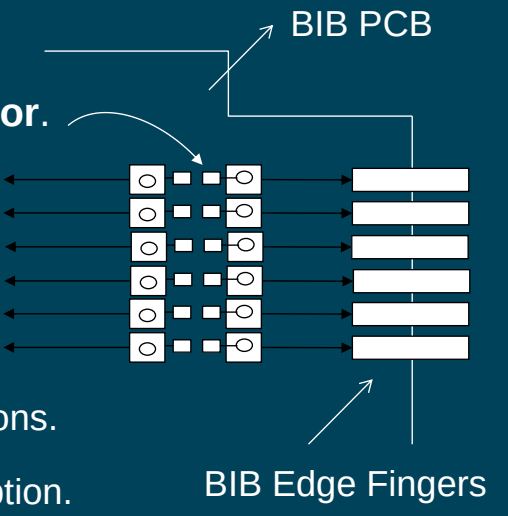
Scrambler Option Techniques

UBIB Design to:

- Bring "Un-used channels" from Edge to **Scramble Connector**.
  - To enable boards for new or forthcoming device/s.

Also, Layout "Un-used socket pins" to Scramble Connector.

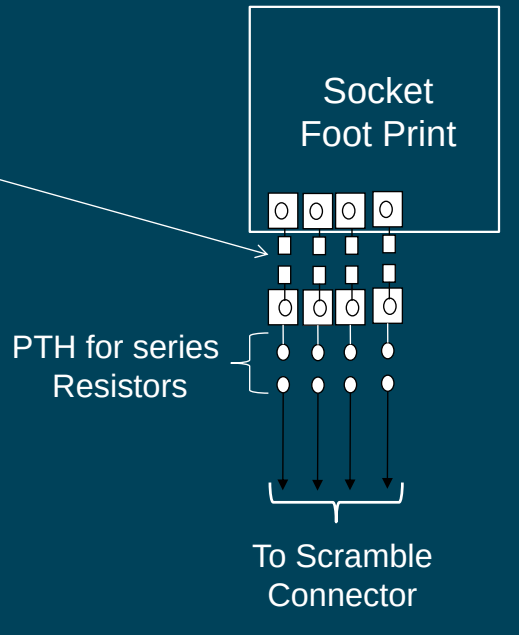
- To enable other or new device/s, to use those additional connections.
  - Changes can be made later using the Scramble Connector Option.



Socket Level Options

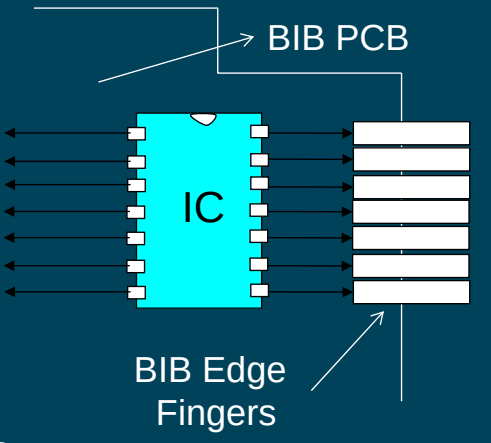
Socket Level Options:

- All socket pins to have **"Pad-to-Pad Connection".**
  - Normally shorted by soldering.
- Connect all "no connection" pins to "unused" channels.
  - To use boards for other devices later.
- Also enables UBIBs:
  - To connect or disconnect a pin
  - To change biasing condition of a pin
  - To connect unused channels to new device.



Other Advanced Options

- Include use of ICs on BIBs: Latches, MUX, PAL ICs.
  - Program ICs to select different channels to socket pins.
- BIB layout to implement:
  - Connecting IC Inputs to channels
  - IC output pins to device pins.
- For use of new device, the ICs to be programmed.
- **Pre-caution:** On board ICs to be of high temp. use.
- **Disadvantage: O**n Board IC's reduce socket density/BIB.



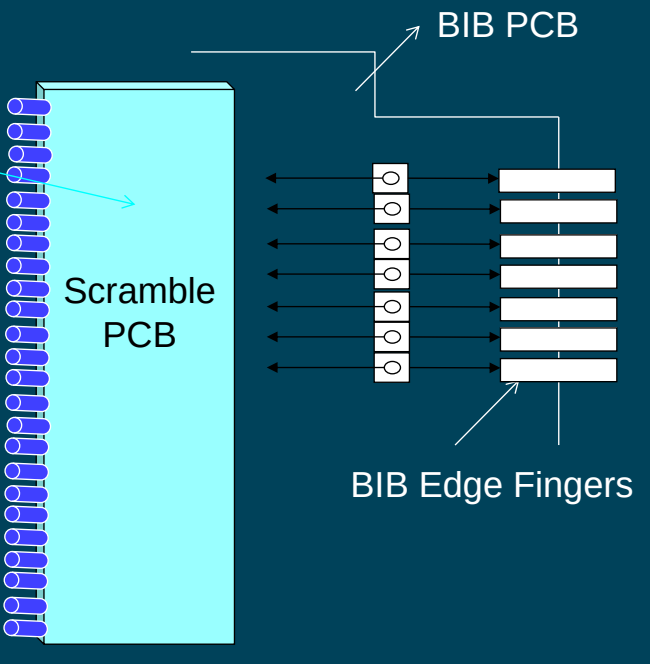
Scramble PCB Method

Uses a PCB with all options for new device.

- All the changes will be on a plug in PCB.

- Advantageous when:
  - Large number of BIBs need to modify same way.
  - BIBs to be changed between devices too frequently.
  - Changes for different devices are too cumbersome.

- Each device might have unique Scramble PCB.



System Compatible BIBs & Techniques

- For boards to use on two BI Systems, from same OEM:
  - Number of channels of one Oven is a subset of other.
  - Channel assignments of Edge Connector are same.

- Example Ver-1 (Old) & Ver-2 (New) Systems:
  a) BIB Edge Connector: 144 Gold Fingers.
  b) 72 on top, followed by 72 on bottom.

System Compatible BIBs - 2

Case-1: For Ver-1 boards to use on Ver-2 system:

- Ver-1 with 48 channels, top & bottom fingers shorted.
- Ver-2 with 96 channels, top & bottom fingers open

Above opposing needs are resolved by:

- Channel patterns (PnP) to be modified.
- All channels assigned to bottom 72 fingers to be tri-stated
- A new PnP program to generate per Ver-2 requirements.

Note: Ver-1 board on Ver-2 system can only use for a device with 48 channels.

System Compatible BIBs - 3

Case-2: For Ver-2 board to use on Ver-1 System:

- Ver-2 BIBs designed with 96 channels, top & bottom fingers Open.
  - Devices with 48 channels only can be used on Ver-1 System.
  - New PnP to redevelop per Ver-1 Channel assignments.
  - Edge fingers to short on top & bottom (Option: Scramble PCB)
- Modify test program to use “strobe” and “monitoring” signals.

Note: If short is not detected, system may false trigger stimuli fault.

System Compatible BIBs - 4

Options on Ver-2 BIBs to be compatible (backward) to Ver-1:

- To have shorting Option for top and bottom edge fingers of the BIB

The board design to include:

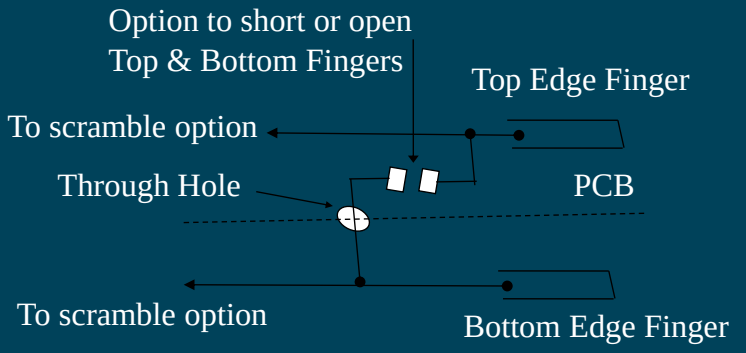
- A track from each of bottom fingers to a pads next to top fingers.
- All top edge fingers will also be pulled to another set of pads.
- To short the pads to convert BIB back to Ver-1 system compatible.

System Compatible BIBs - 5

Converse option to design on Ver-1 (old) boards:

- With normally short between top and bottom edge connectors,
- to make them forward compatible to Ver-2 system:

- Removing the short and using a new BI program with Ver-2 requirements.



Implementation & Cost Savings

Implementation Done: Concept used in GF for 3 technology nodes.

- Done by planning, follow up and design coordination with:
  - Design Engineering during Device definition phase
  - To plan same package type and Pin assignments etc.,
  - To ensure new devices match to existing UBIBs to use.
- Subsequently same boards were also used for PRMs.

Estimated Cost Savings:

- For 3 Devices and subsequent tech. nodes Qualifications
- Use UBIBs for PRMs Vs new set of BIBs every time.
- Cost savings are significantly high: **$0.75~1M** over 3years.

Cycle Time Savings

Cycle Time Savings: Below table shows cycle time savings achieved using UBIBs.

Item	Pre-Project Cycle Time Required	Post-Project Cycle Time Achieved	Cycle Time Saved	Remarks
Boards Re-Fabrication Time	10 wks	1 wk	9 wks	Re-configuration/Minor modifications on the boards.
Boards Re-design & Layout Verification Time	3 wks	0	3 wks	As the redesign and layout verification is eliminated.
Screening Test Program Redevelopment Time	2 wks	0	2 wk	As the redevelopment is eliminated.
Boards Screening Time	1 wk	0	1 wk	Screening time saved for subsequent device Quals.
BIP development and verification time	3 wks	1 wk	2 wks	Program modification instead of complete redevelopment.
Total Cycle Time Saved/Qualification			17 Wks	

UBIBs: Advantages - 1

Faster Turn-around Times

- Eliminates Re-fabrication
- Eliminates Redesign
- Eliminates Re-development
- Provides Faster BIP Development
- Provides Faster Verification Time

UBIBs: Advantages - 2

Better Utilization of Burn-In Ovens:

- **Flexibility on different systems**: Different versions from same OEM
- **More Availability of Ovens:** Early stress start on either of systems.
- **Lesser Waiting Time:** for the lot to stress and complete.
- **Faster Qual.** cycle time ➔ Faster feedback to Process/Customers.

Operational Advantages

Operational Advantages: As only one set of boards in operation:

- **Easier Operation**: no confusion to operators, on which boards to use.
- **Less Errors**: in using boards for each device.
- **Better Control** and monitoring of boards.
- **Easier to Manage** Boards, lesser storage space etc.,
- **Lesser Maintenance:** Only one set of boards to upkeep.
- **Lower Operational Costs ➔ More savings.**

Conclusion

- Cost of dedicated BIBs is significantly high.
- Common / UBIBs can be designed for >2 devices.
  - After meeting pre-requisites and with early design planning.
- UBIB design techniques & methods provide flexibility.
- UBIBs have several advantages when implemented.
- Implementation done: $0.5~0.75M savings achieved.

References

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2) JESD-47: Stress-Test-Driven Qualification of Integrated Circuits by JEDEC, Solid State Technology Association.

3) JP-001: Foundry Process Qualification Guidelines for Wafer Fabrication Manufacturing Sites, by JEDEC.

4) JESD659: Failure-Mechanism-Driven Reliability Monitoring, Electronics Industries Alliance, JEDEC, Solid State Technology Association.