COPYRIGHT NOTICE

www.bitsworkshop.org

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Sandeep Sankararaman - R&D Altanova
Noel Del Rio - NXP

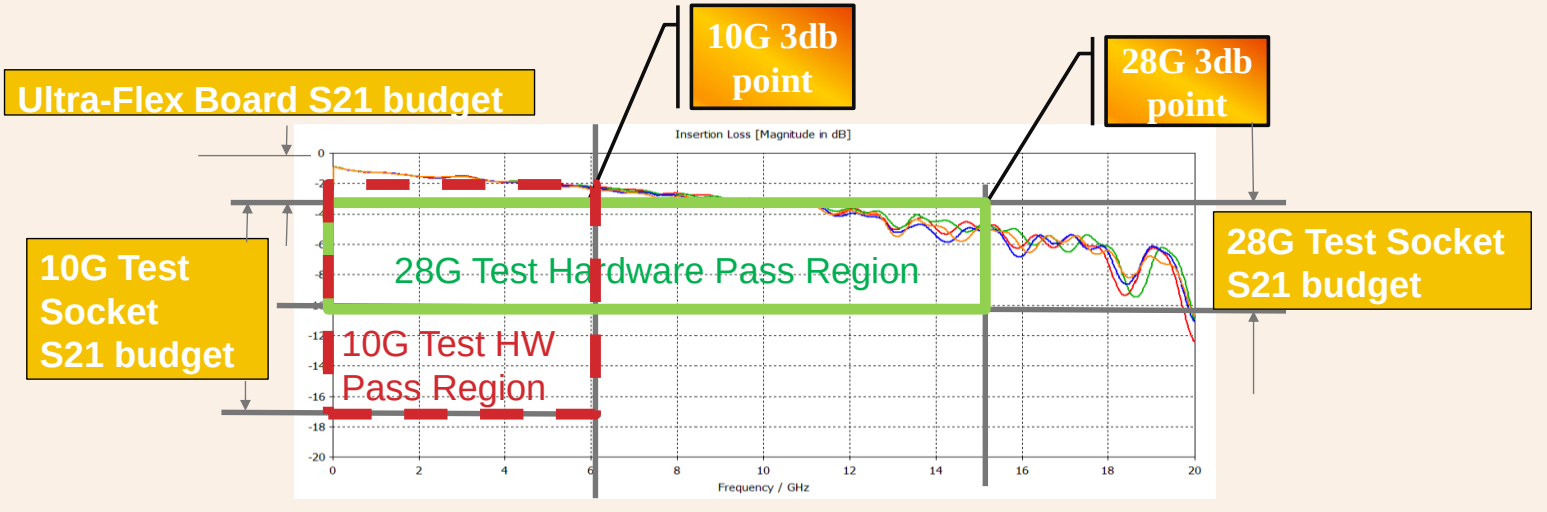
BiTS Workshop
March 4 - 7, 2018

Agenda

- Socket performance impact
- Designing a socket and it's load board transition for 28G
- Measurement fixtures and process to verify socket performance individually and in system
- NXPs experience with different 28G sockets

Socket Performance Impact

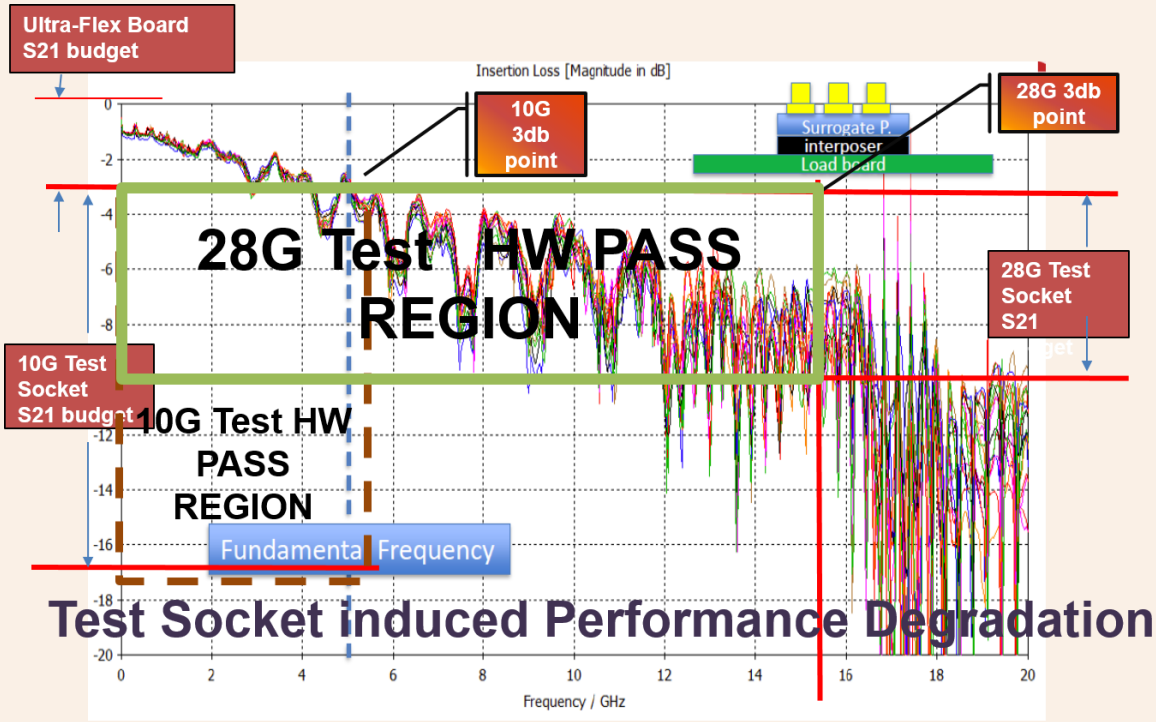
The socket performance factor



NXP Test Setup S21 (Insertion loss) plot.

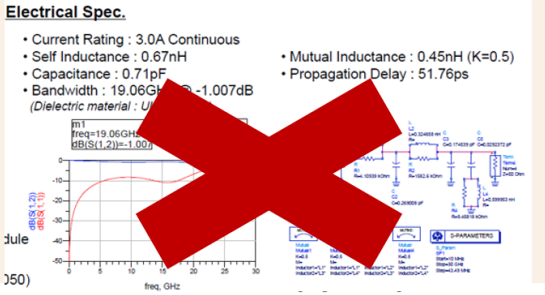
- Loadboard and support circuit only
- No Test Socket

The socket performance factor



Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

It's a socket, not just a pin



Wrong Model!

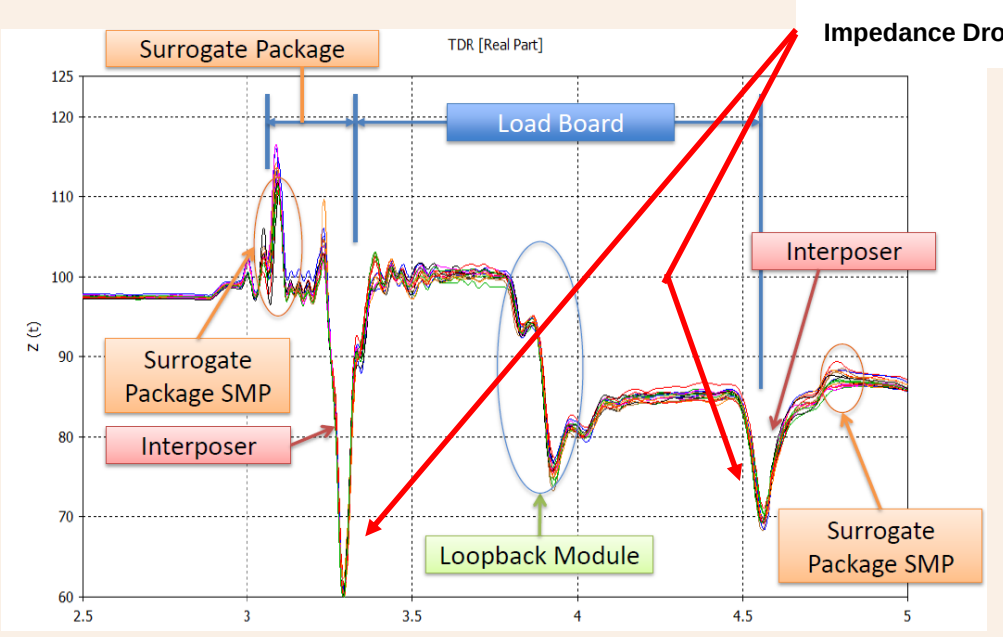
Pin performance insufficient

6.000 Ghz

15.000 Ghz

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

It's a socket, not just a pin

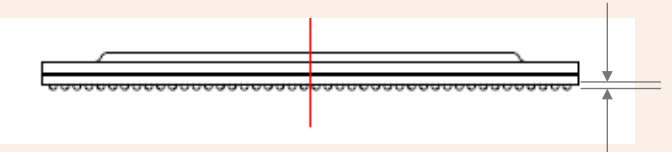


Blind built test socket

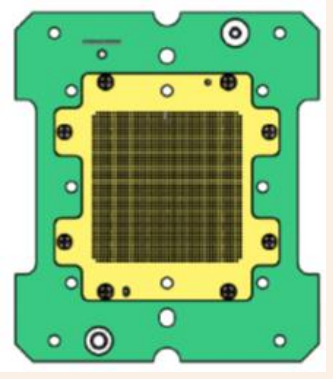
- Selected pin from datasheet
- Signal path not modelled
- Traditional practice of focusing on the pin

Analytical approach to test socket design

Define Socket Mechanical Model



Co-planarity



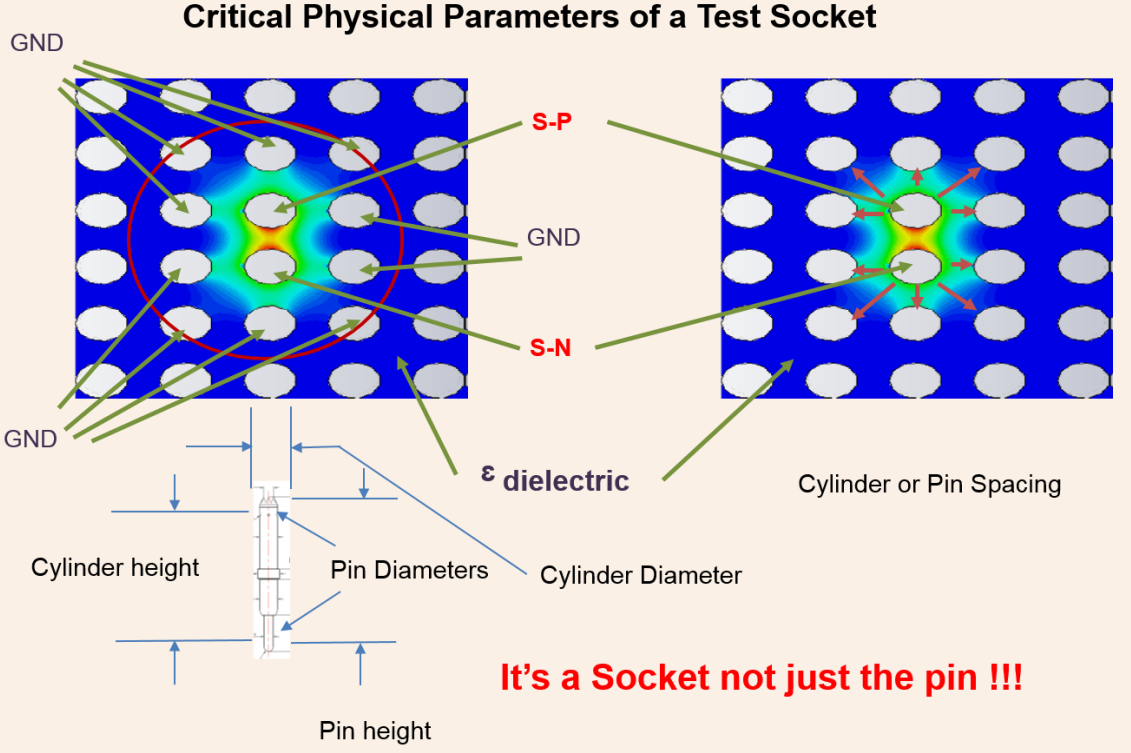
Test Socket Model to address key issues

- Handler capable of 28G data rate?
- Shortest pin the handler can accommodate?
- Co-planarity for 45x45 BGA package
- Define a range of specifications (mechanical) to allow socket vendor to design a 28G capable test socket
- Mechanical consideration is as important as electrical performance

BiTS 2018 Burn-in & Test Strategies Workshop

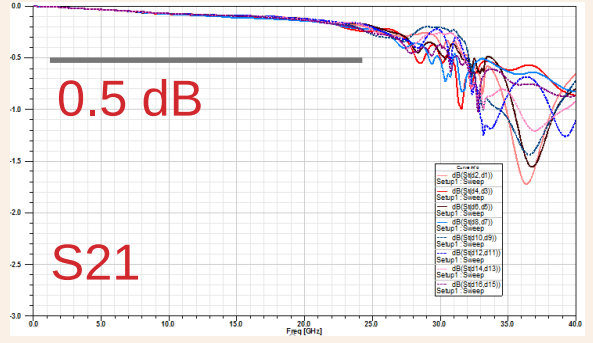
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

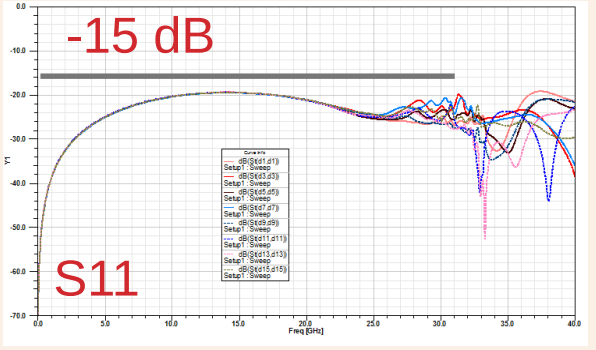
It's a test socket, not a just a pin



Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Define Socket Performance Budget, AC and DC





15 Ghz

28G Test Socket Target Performance

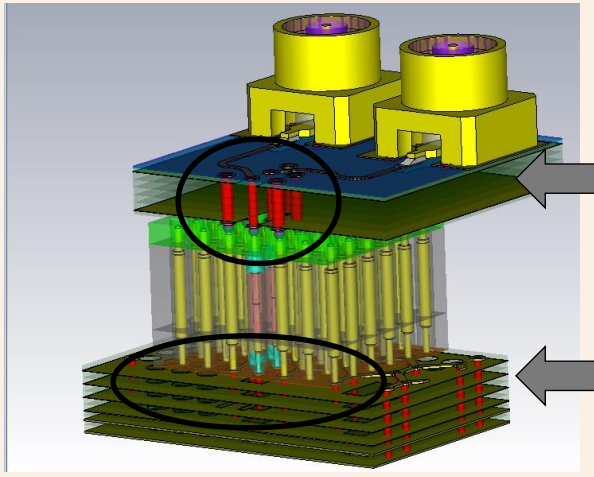
- S21 = 0.5 dB @ 15 GHz
- S11 ~ (-15db) @ 0.5 dB point
- Serdes Lane to Lane Correlation <0.5 db.
- Diff Z_0 = 100 Ohms + / - 10%
- After n-K cycles
  - S21 = -5db @ 15Ghz
  - S11 > (-15db) @ 15 Ghz
  - Differential Impedance is above 90Ω
- All parameters are to be measured by VNA (Vector Network Analyzer)

BiTS 2018 Burn-in & Test Strategies Workshop

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

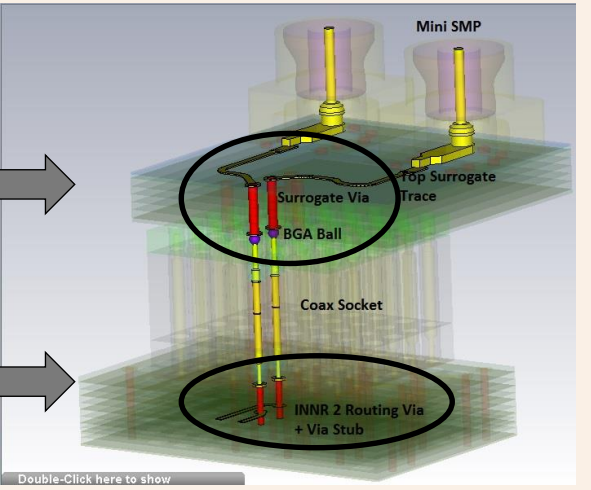
Optimizing the socket and its transitions

The Socket + Transitions



DUT to Socket transition

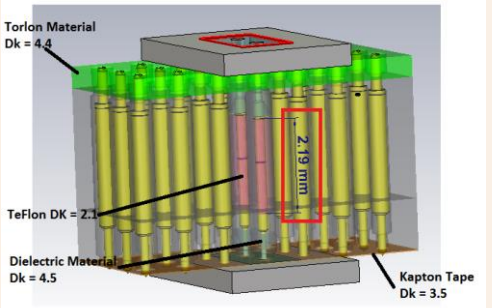
Socket to PCB transition



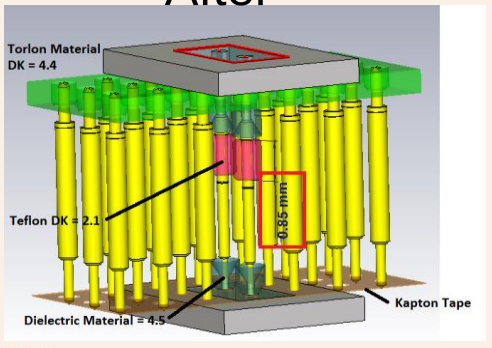
At 28+ Gbps, transition to/from socket as important as socket!!!

Socket Design Optimization

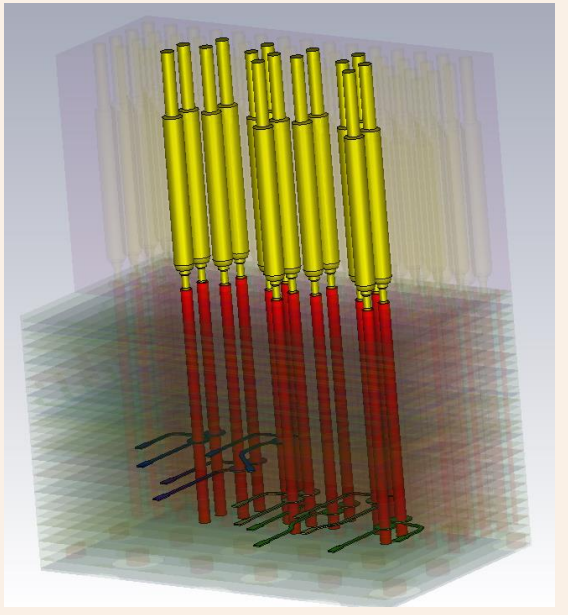
Before



After



DUT Escape Crosstalk



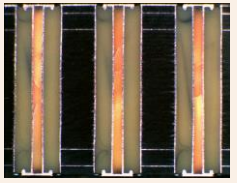
BiTS 2018 Burn-in & Test Strategies Workshop

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

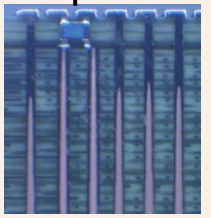
PCB, Socket Models & Design Consideration

Design → **Fab/Assy** → **Validation**

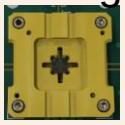
True coax vias



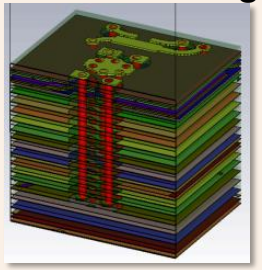
Embedded components

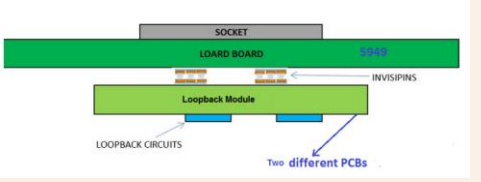


Socket technologies



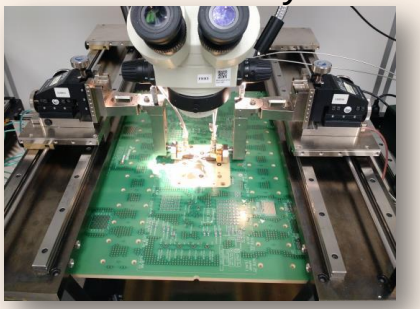
EM Modelling



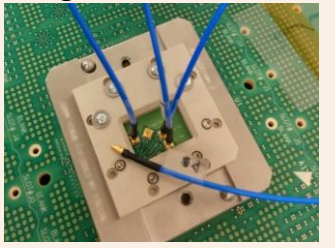


Material selection, Component selection, Backdrill control

PCB Only



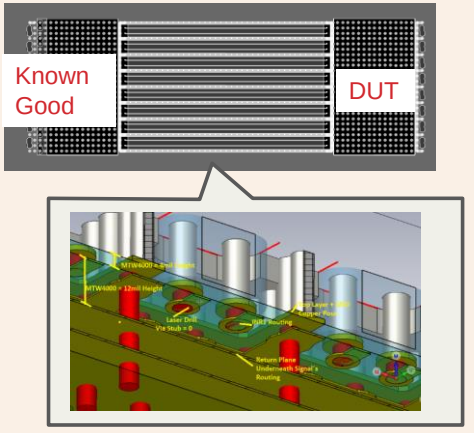
DUT Surrogate + Socket + PCB

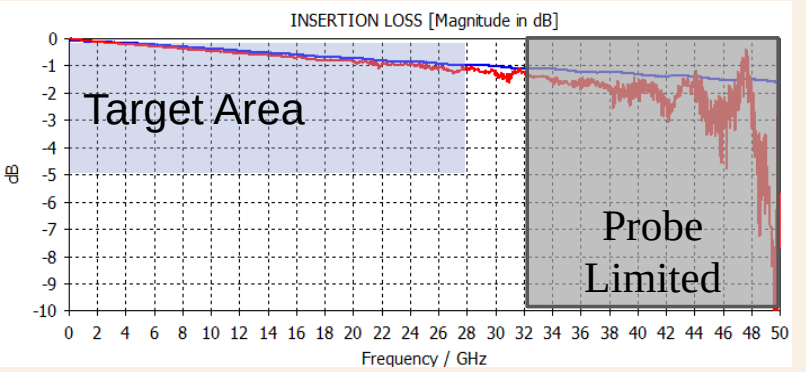


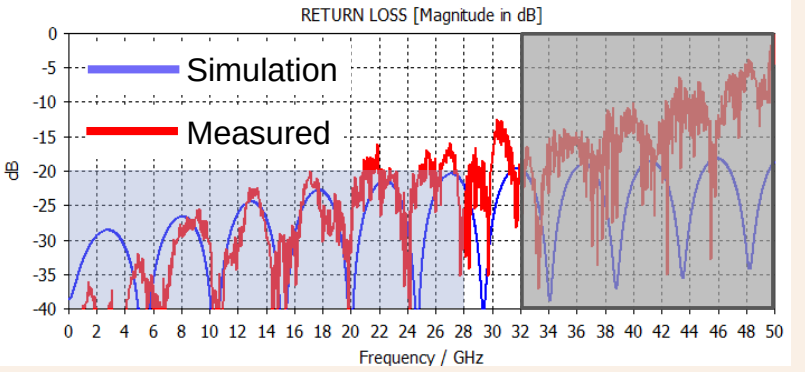
BiTS 2018 Burn-in & Test Strategies Workshop

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

PCB Optimization and Simulation – 56 Gbps NRZ







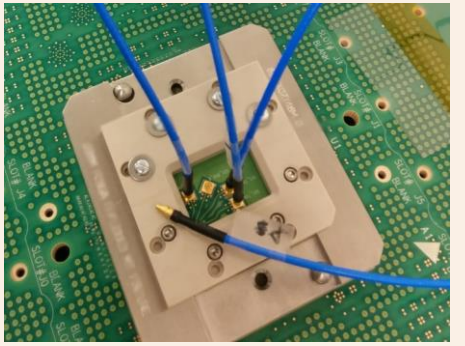
First pass success requires:

- Modelling every transition in 3D EM with sufficient BW.
- Understanding fabrication limits, tolerances and how to use them to your advantage

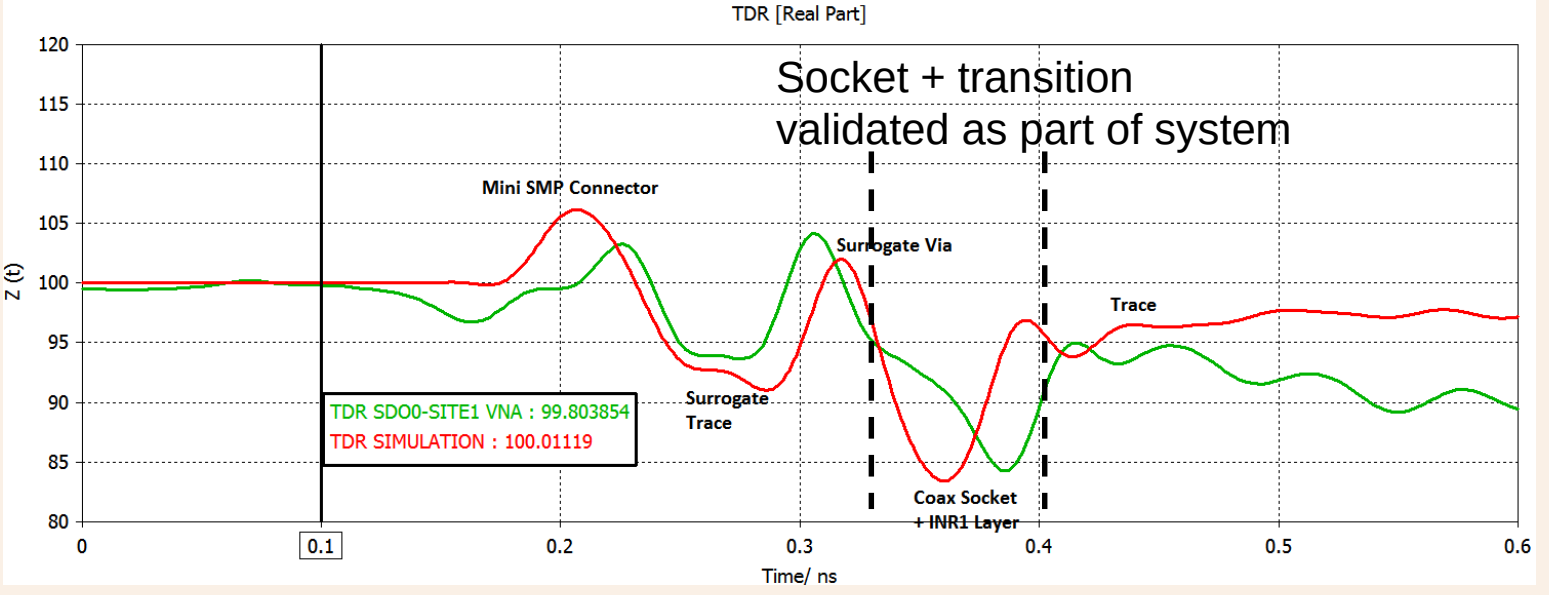
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Measuring Socket Performance

- Requires a DUT surrogate PCB
- PCB needs to be same thickness as DUT
- Needs a socket lid with open top access
- Uses coaxial connectors to connect to test equipment
- Surrogates with calibration structures are used to remove the surrogates from the measurement
- Due to the size of the coaxial connectors, multiple surrogates are usually needed to treat multiple channels



RDA Socket Performance Validation

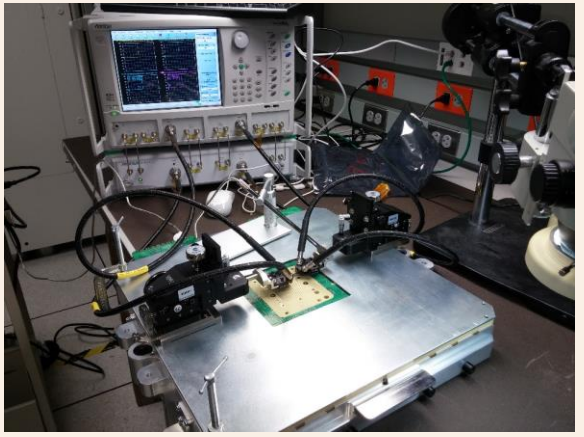


Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Design instrumentation fixtures to facilitate accurate measurements

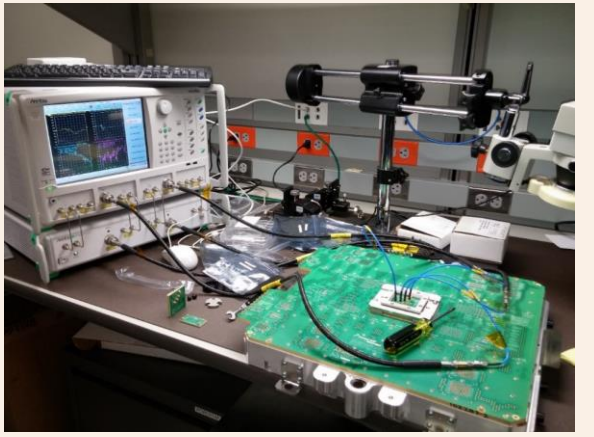
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

NXP's, S-Parameter Measurements, and TDR Plots Setup, Loadboard & Test Socket



Loadboard Probe Measurement Setup

Surrogate based Measurement



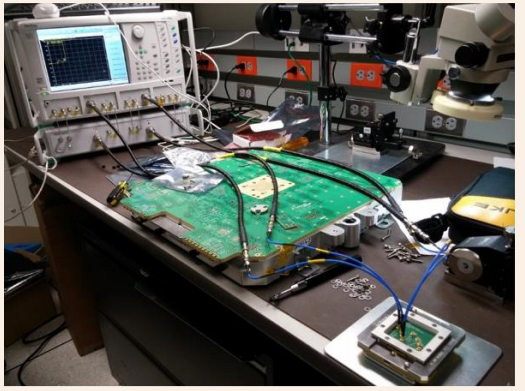
Surrogate and Cables are de-embedded

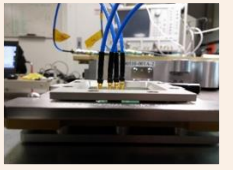
Loadboard and Test Socket Measurement Setup

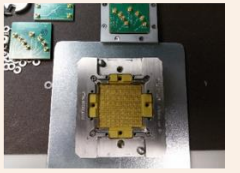
BiTS 2018 Burn-in & Test Strategies Workshop

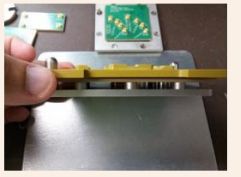
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

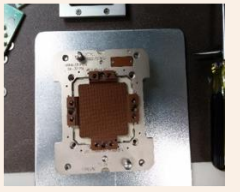
S-parameter and TDR Measurement Setup

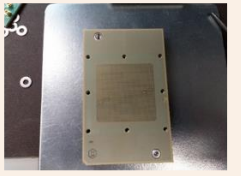












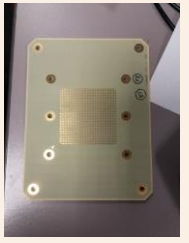
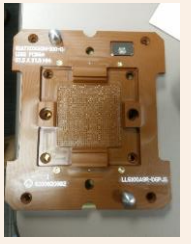
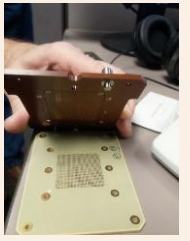
Test Socket/Pin Isolated
Compressed VNA measurement setup

Performance measurement of the test socket independent of the loadboard.

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

NXP Socket isolation Setup

1 2 3 4 5 6 7

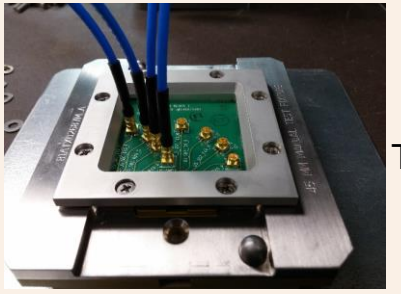

Support Block

Isolation PCB

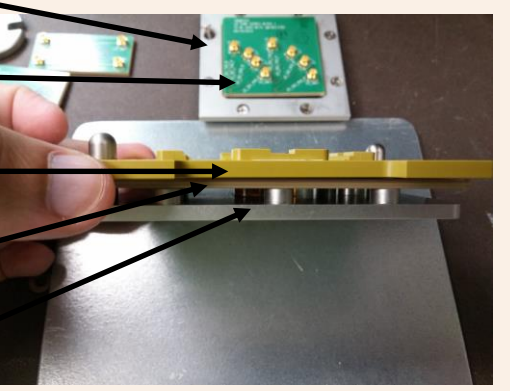
Test Socket

Surrogate & Lid

28G Specifications:
- S21 3dB point at 20Ghz
- S11 -11dB to -15dB at 3dB point
- Differential Impedance 100 +/- 5 Ohms

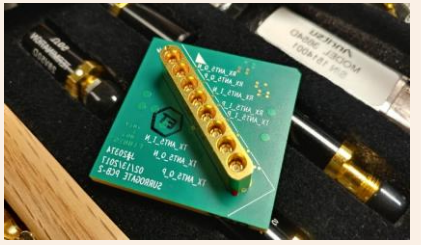


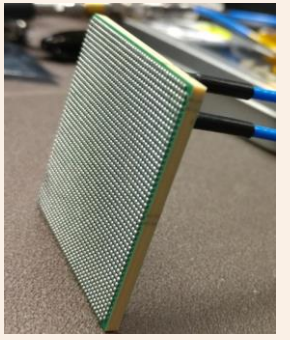
Socket Isolation Setup

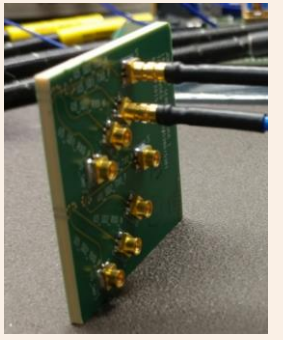


Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Test socket interface





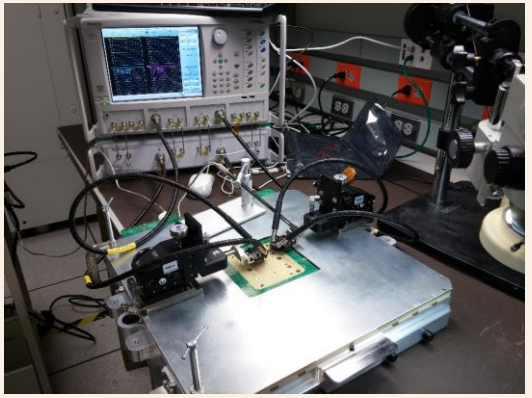


DUT Package Surrogate

- Precision electrical interface to enable access at the Pogo-pin top
- It is modeled, simulated, and validated with VNA (Vector Network Analyzer)
- Performance Specifications for 28G
  - S21 3dB point at 20Ghz
  - S11 -11dB to -15dB at 3dB point
  - Differential Impedance 100 +/- 5 Ohms
- De-embed point up to surrogate balls

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Loadboard Measurement Setup



Measuring the loadboard with probes

Measuring loadboard performance with SMP connectors

Design of experiments

NXP 28G Test Socket DoE (~ 1.5 years)

- 6 Test Socket Vendors
- Two 28G Serdes devices with identical package design used as characterization test vehicle
- NXP Mechanical Model created as reference design
- Electrical Performance requirements defined in frequency domain(S-Parameters) and time domain (TDR Impedance)
- Full functional test & Characterization program applied
- Test Sockets mechanical cycle range, 20k, 30k, 50k
- Temperature 25C, -40C, -110C

BiTS 2018 Burn-in & Test Strategies Workshop

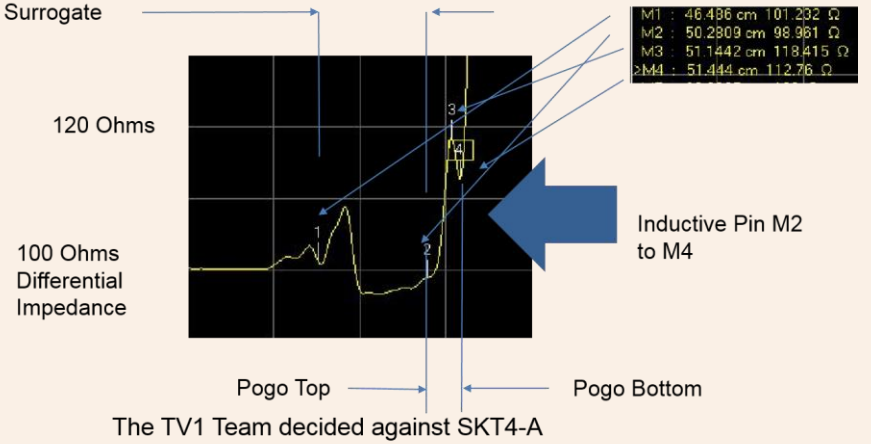
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

DoE Summary

- Analytical approach to test socket design enables objective assessment of its performance and impact to device testing
- Zero Failures on all test sockets, 100% first pass yield
- Pogo pins used in the study are at very close performance from time-0 to 20K and 50K cycles. Devices are still functionally passing electrical test.
- Test socket vendors modeling, simulation, and validation capability is an area for growth and opportunities.
  - Accuracy of design models to actual product performance is an area for improvement
- The cost of test socket validation is an area the industry has to deal with for short wavelength and high speed testing.

Measurement results and observations

(#1) Test socket that is not compliant at time-0, cycle 0

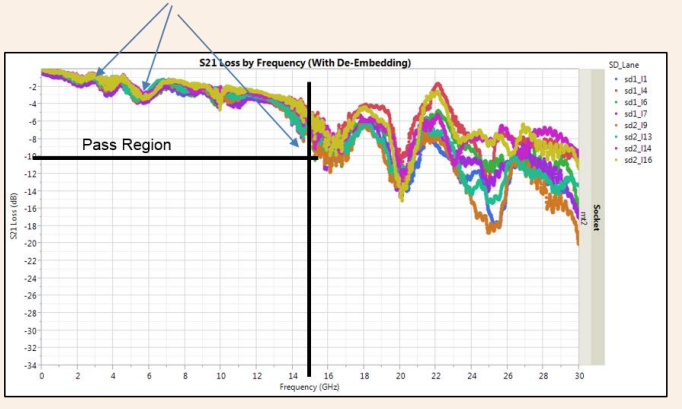


The TV1 Team decided against SKT4-A

1. High discontinuity (> 120 ohms impedance)
2. S21 failed to clear the -10db limit at 15 Ghz @ cycle=0

Time domain profile of a pogo pin socket

High level of rippling for inductive Test Socket SKT4-A



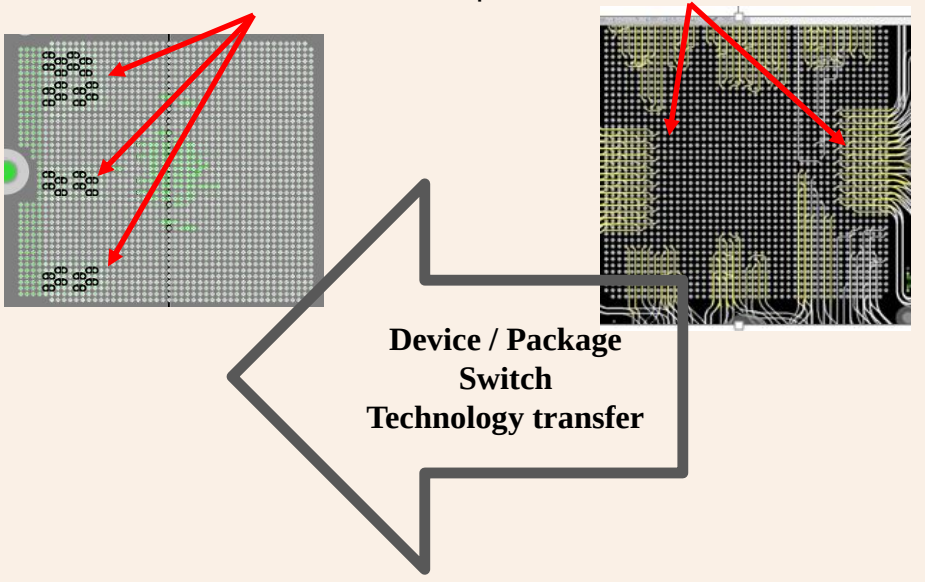
The TV1 Team decided against SKT4-A

1. High discontinuity (> 120 ohms impedance)
2. S21 failed to clear the -10db limit at 15 Ghz @ cycle=0

Frequency domain profile. The effect of inductive pin/socket on test hardware setup

(#2) Application of the same models on the same package but different profile

DUT field or Ball Map, and SERDES PAD location



TV1 28G SERDES 16 I/O Layout

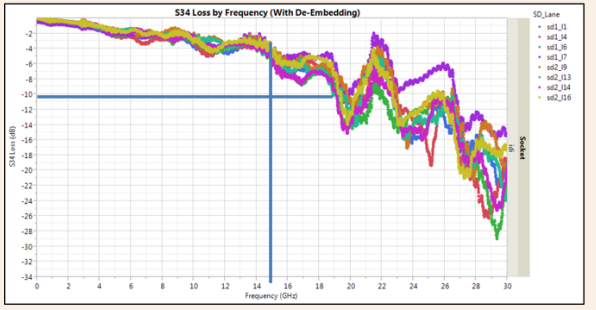
T4 SERDES 32 I/O Layout

(#2) Socket manufacturing challenges

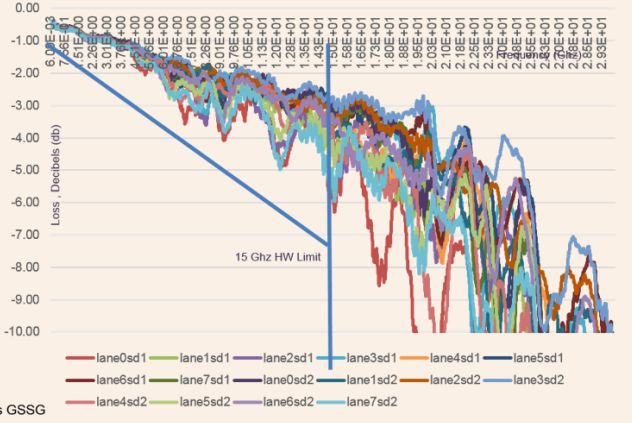
Correlation problem between models and fabrication

Same model different performance from T4 to TV1

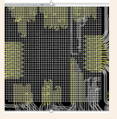
SKT4-B 28G S21 Insertion Loss Plot



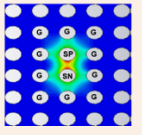
SCKT4-B, TV1 LB#3 S21 Insertion Loss

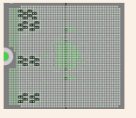


Differential Signal Pads GSSG



T4 Package

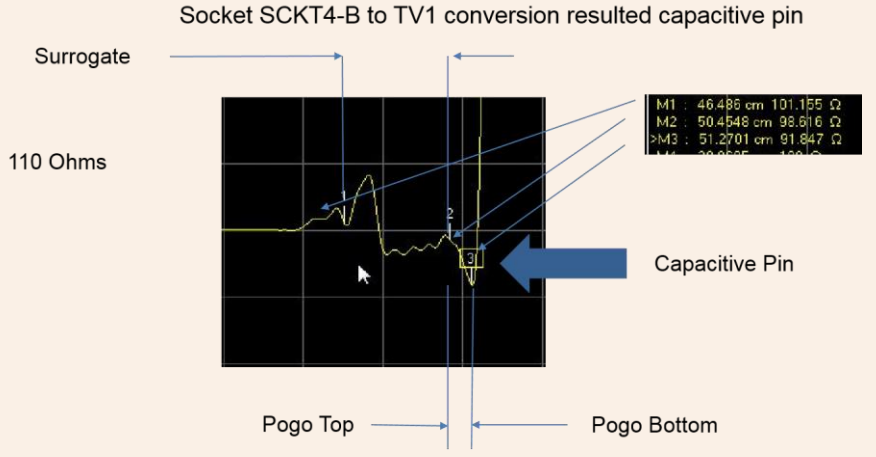


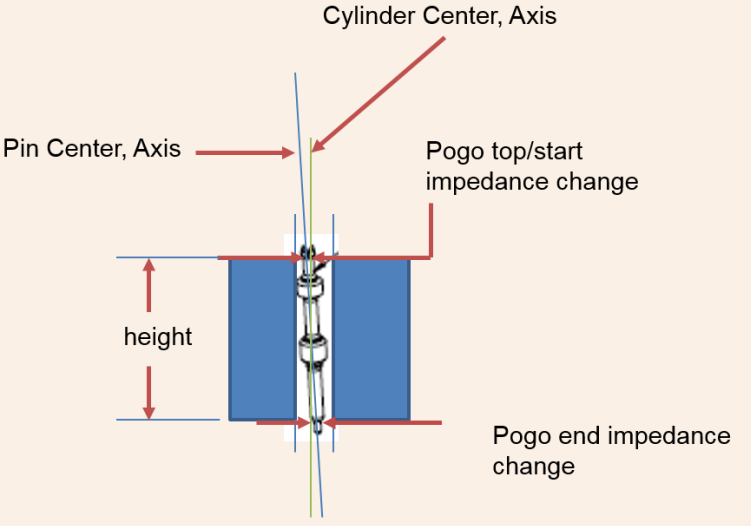


TV1 Package

Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

(#2) Socket manufacturing challenges





Socket SKT4-B to TV1 28G Conversion challenges

- Models and Simulation results use on T4-Package did not translate to the same performance to TV1Package

Pin wobble within the cylinder a source of discontinuity

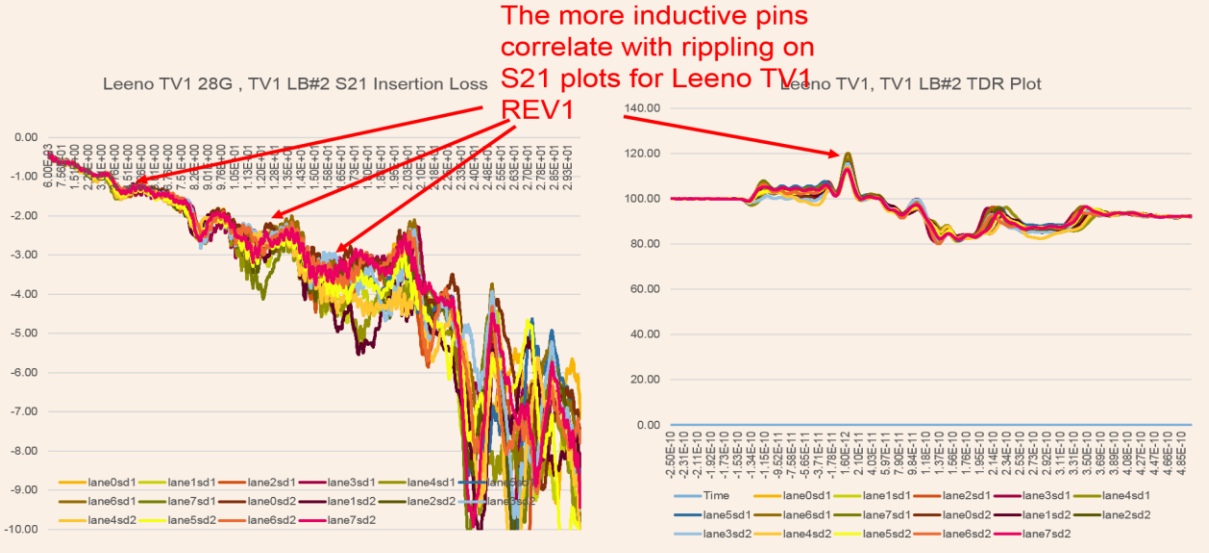
Pin Wobble: Illustration

Leeno Socket

 # 3, Leeno T4 to TV1 28G Conversion challenges..

We had a case of validation and instrumentation correlation question

- TV1 R1 Models resulted to inductive pin/socket
- TV1 R2
  - Change pin diameter
  - Change package material with better dielectric constant

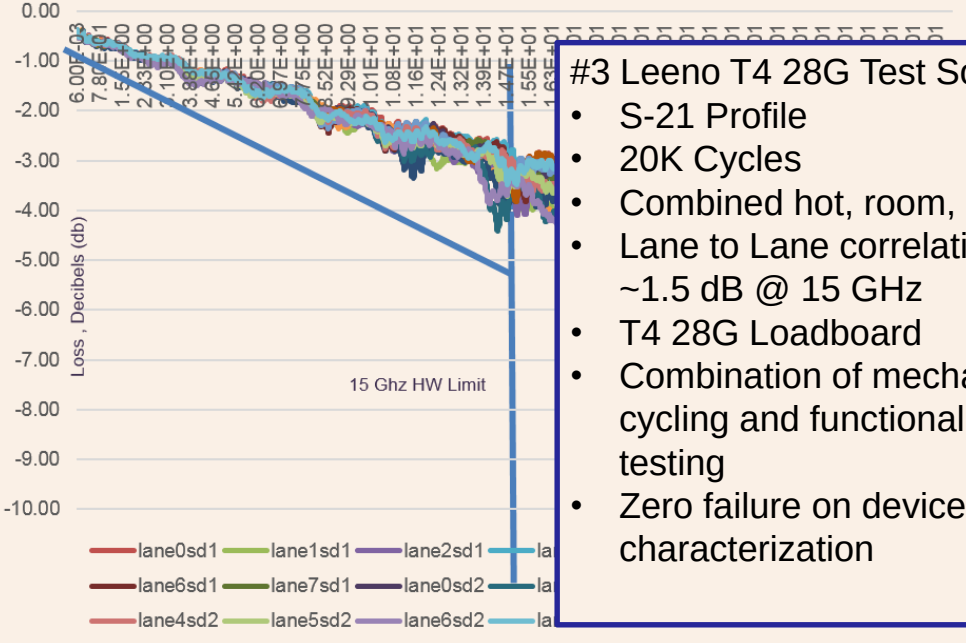


Leeno R1 TV1 Test Socket

Leeno Socket S21

IL (dB) TV1 LB#3

1. Cycle count ~ 20K
2. Mechanical Cycling performed on FSL ATC Handler



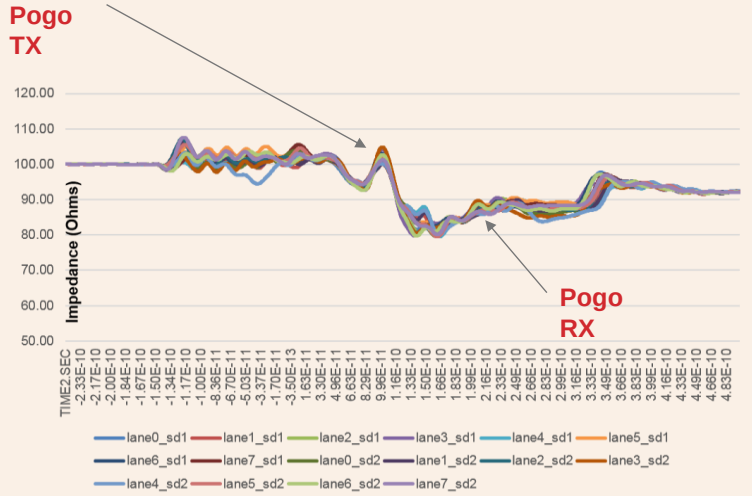
#3 Leeno T4 28G Test Socket

- S-21 Profile
- 20K Cycles
- Combined hot, room, cold
- Lane to Lane correlation ~1.5 dB @ 15 GHz
- T4 28G Loadboard
- Combination of mechanical cycling and functional testing
- Zero failure on device characterization

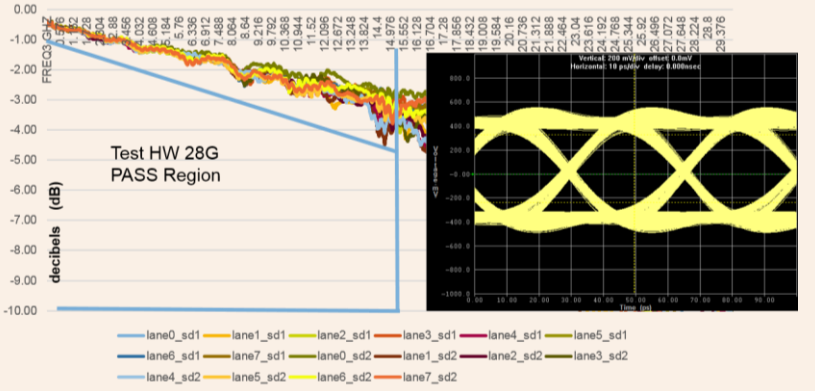
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Leeno Socket TDR Plots

TDR TV1 LB#3 Skt2 Rev2 0 Cycles



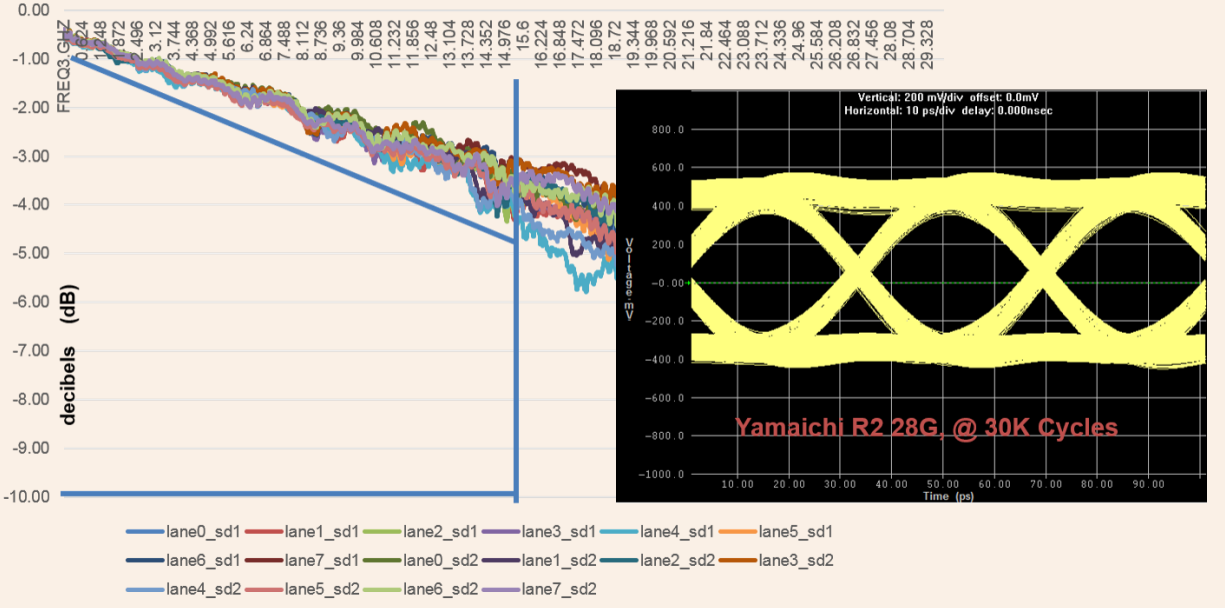
IL (dB) TV1 LB#3 Skt2 Rev2 0 Cycles



Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Yamaichi TV1 28G mechanical cycle test

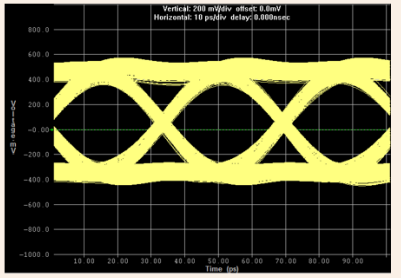
IL (dB) TV1 LB#3 Rev2 30K Cycles



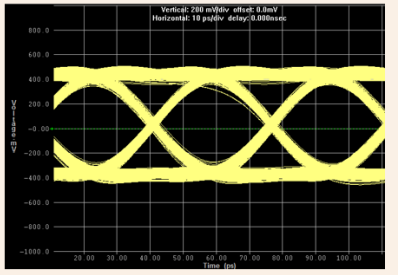
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Yamaichi TV1 28G mechanical cycle test

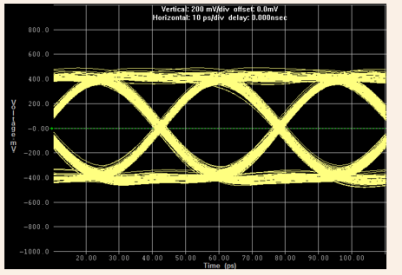
Yamaichi T4 Rev-2 Data Eye from 10K to 30K cycles



Yamaichi R2 28G, @ 30K Cycles



Yamaichi R2 28G, @ 20K Cycles



Yamaichi R2 28G, @ 10K Cycles

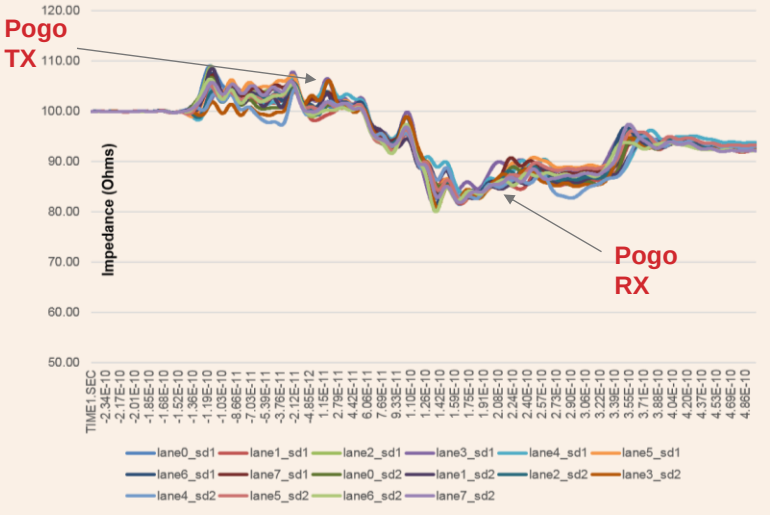
- Yamaichi R2 use a socket material with better dielectric
- Data eye remained in excellent condition at ~ 30K cycles
- Date eye height is affected by cycle count
- Device pass TV1 Electrical Test
- Socket, pin has not been cleaned to date

BiTS 2018 Burn-in & Test Strategies Workshop

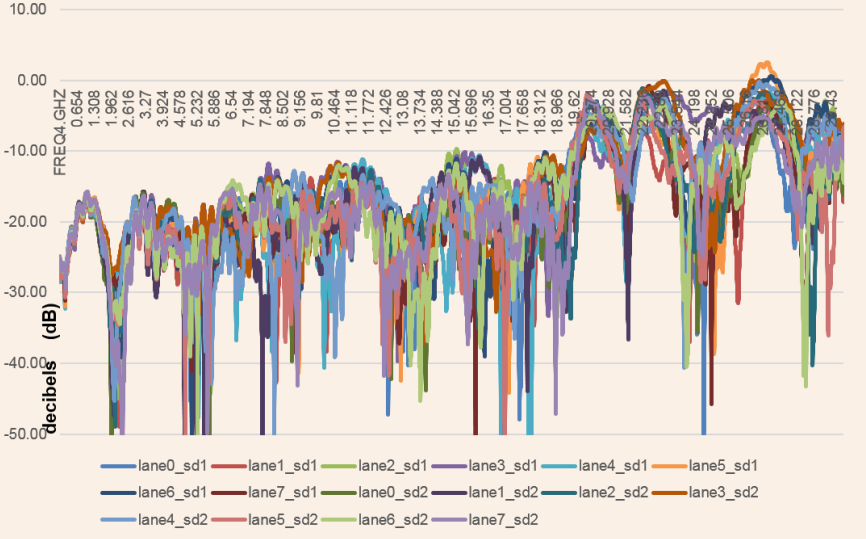
Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Yamaichi TV1 28G mechanical cycle test

TDR TV1 LB#3 Rev2 30K Cycles



RL (dB) TV1 LB#3 Rev2 30K Cycles



Methodology for Measuring and Characterizing 28Gbps+ SERDES Sockets

Conclusions

- It's a Test Socket. A matrix of conductors inside a cylinder with specific dielectric.
- For >10G, specify Test Socket performance, not datasheet based pin
  - S-Parameters (S21, S11) in frequency domain
  - TDR for time domain profile of the pin inside the cylinder
- Performance validation to establish compliance i.e. VNA, and TDR needed
- Mechanical design specification is very important & strongly impacts electrical performance of the Test Socket.
- Signal Integrity Design of probes, interface, and signal access is a must. Objective definition of its performance requirement is key to ensure compliance to device specification
  - S-Parameters (S21, S11) in frequency domain
  - TDR Impedance