## NINETEENTH ANNUAL

**Burn-in & Test Strategies Workshop** 

March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel Mesa, Arizona

Archive

## **COPYRIGHT NOTICE**

The presentation(s)/poster(s) in this publication comprise the Proceedings of the 2018 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2018 BiTS Workshop. This version of the presentation or poster may differ from the version that was distributed in hardcopy & softcopy form at the 2018 BiTS Workshop. The inclusion of the presentations/posters in this publication does not constitute an endorsement by BiTS Workshop or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by BiTS Workshop. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop. All rights reserved.

## www.bitsworkshop.org

## **Poster Session**





# **Zero Keep Out Zone Socketing Techniques: The advantages and the Limitations**

Emad Al-Momani, Ayman Abdo Intel Corporation

#### **BACKGROUND**

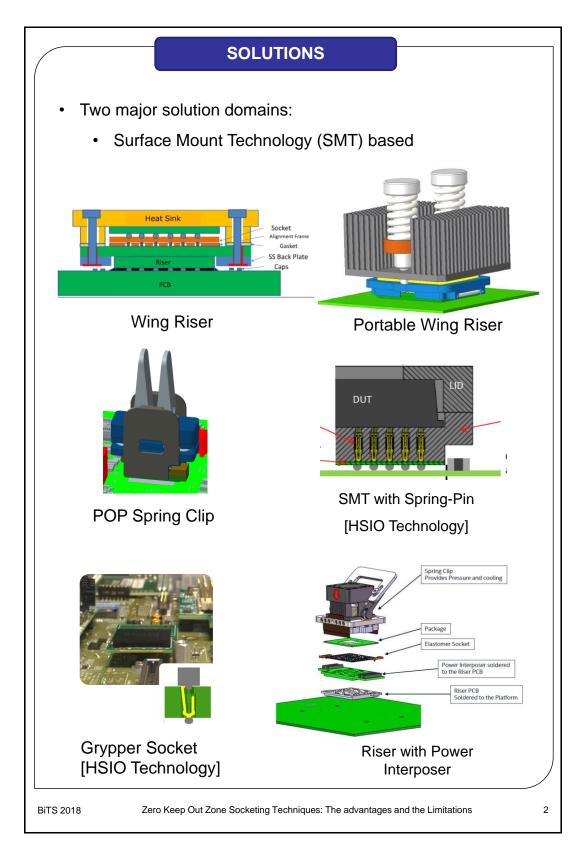
- We are seeing more demand for socketing BGA/LGA packages to OEM/ODM platforms.
- Validation is moving to be on OEM like validation platforms.
- Traditional socketing techniques require keep-out-zone on the platform.
- Most of OEMs/ODMs platforms are designed with no socketing hooks as part of the original design.
- We have worked on several technologies internally and in cooperation with industry partners to enable these type of Zero KOZ socketing solutions.

### **CHALLENGES**

- Reliability Validation HW are expected to sustain large number of usage cycles >300.
- Heatsink and Thermal Tools enabling
- Interposers Zero KOZ solutions need to work with N-1, coax, Power and other types of interposers
- Usability Validation engineers saw large number of packages over the program life cycle, time to swap packages and the ergonomics aspects of it need to be considered.
- Signal and Power Integrity: solution impact on signal and power integrity need to be as small as possible
- Cost

## **BiTS 2018**

## **Poster Session**

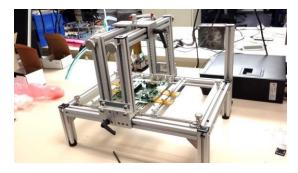


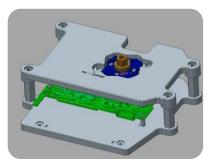
## **Poster Session**

### **SOLUTIONS**

- · Two major solution domains:
  - Chassis based







### **SUMMARY**

- Several ZKO technologies were explored at Intel side in the last two years. Each technology has its advantages and limitations
- ➤ One big challenge is to get the technology to work with minimum failure rate possible. This is more challenging for debug work needed on customers platforms.
- Solder joint quality and reliability is a concern for SMT type approaches
- ➤ Some SMT approaches depends on other technologies such as coax-riser. This increase the challenge as the maturity of these technology is progressing.
- Several approaches were used to aligning socket to platform for non-SMT type sockets.
- Chassis based approaches were found more reliable in getting the system to work with no issues the first time.

Acknowledgment: Hayley Klug, Jack Mumbo, Amy Xia, Stuart Burman, HSIO

BiTS 2018

Zero Keep Out Zone Socketing Techniques: The advantages and the Limitations

3