NINETEENTH ANNUAL

BiTS™
Burn-in & Test Strategies Workshop

March 4 - 7, 2018

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Mesa, Arizona

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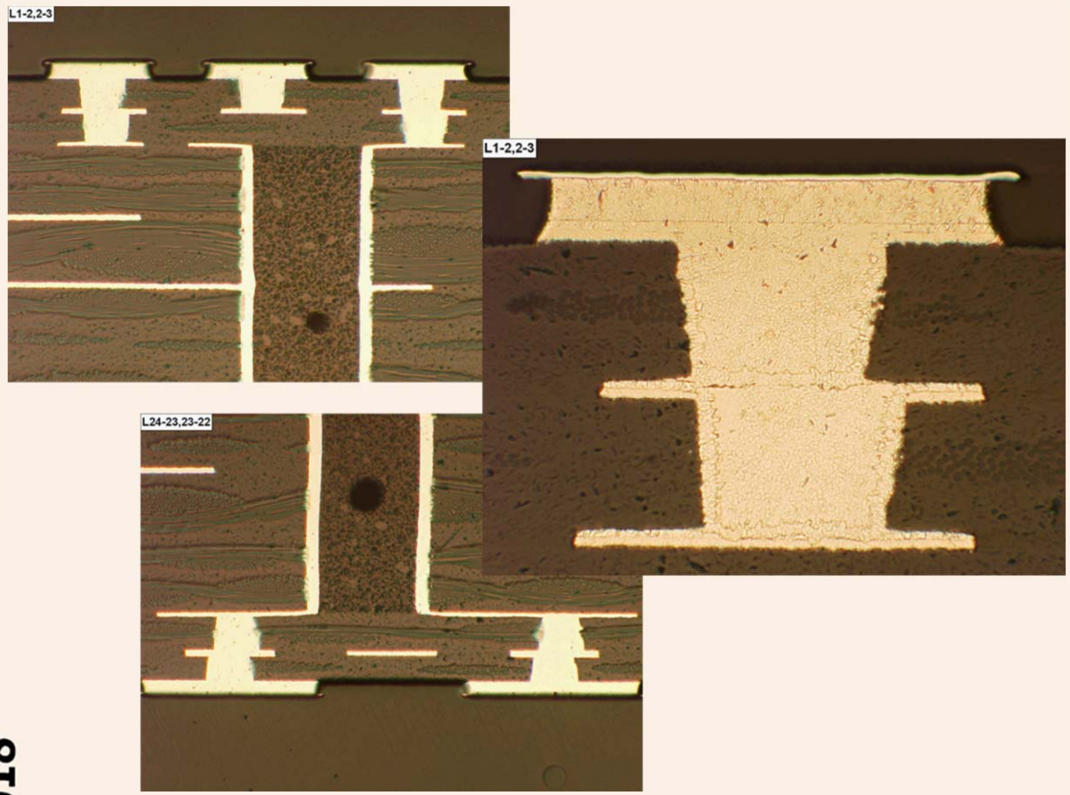
"Connecting Your DUT To Your Tester"

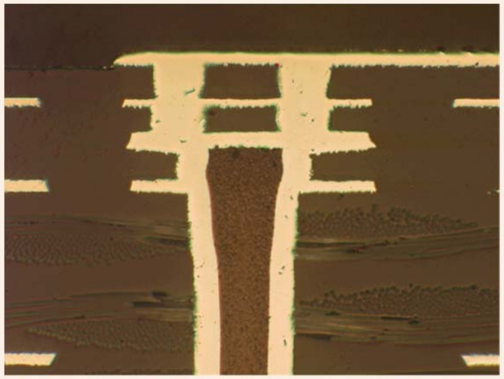
Tom Bresnan
R&D Altanova

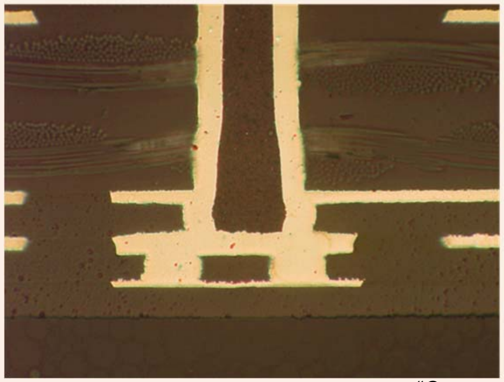
BiTS Workshop
March 4 - 7, 2018

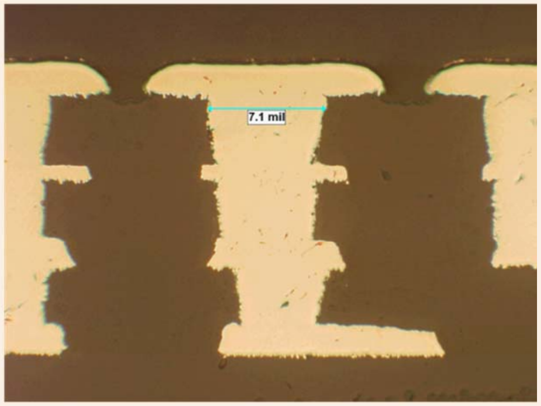
It's all about making connections

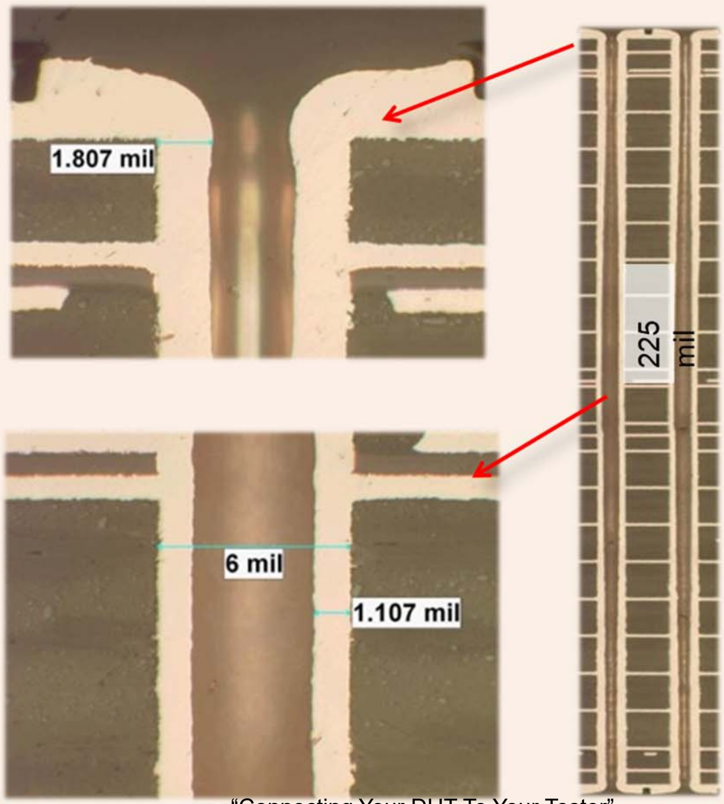


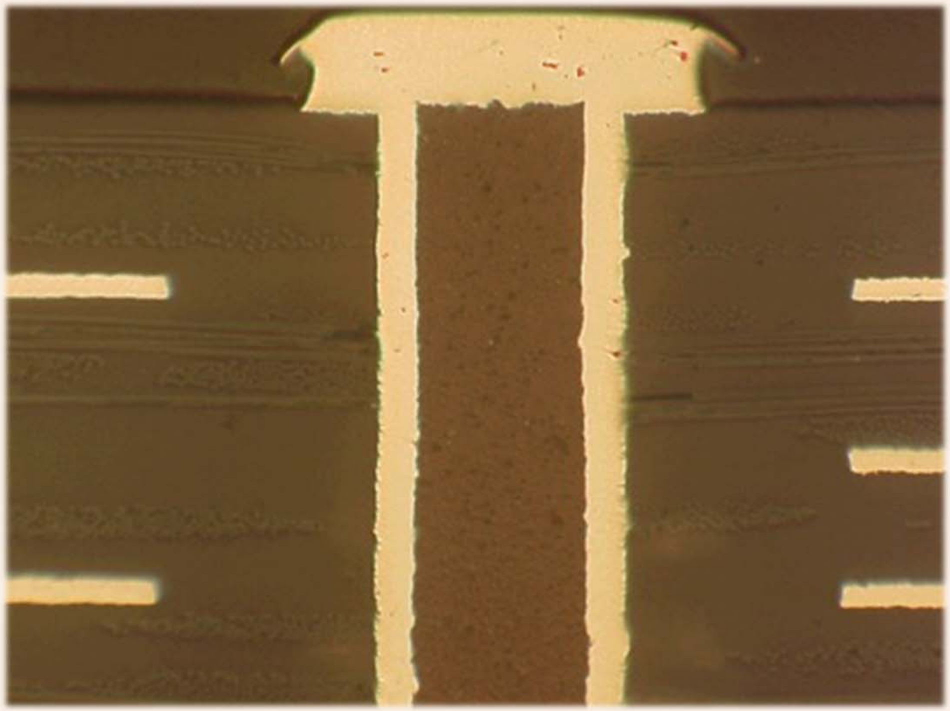
It's all about making (good) connections








1.807 mil
6 mil
1.107 mil
225 mil

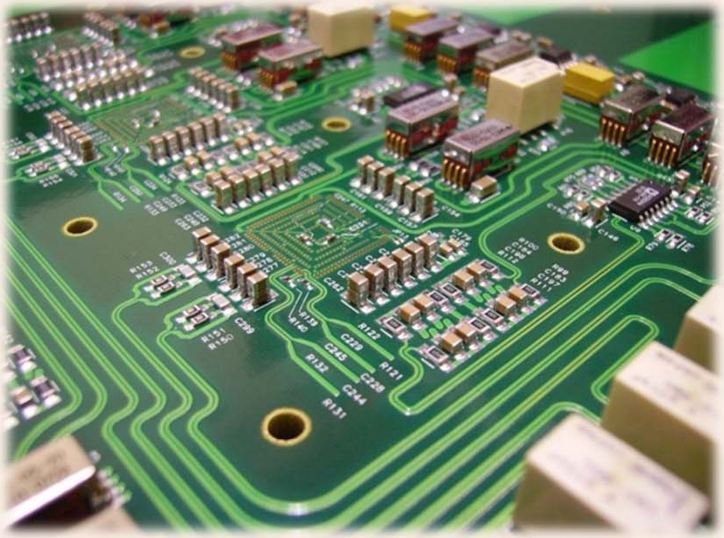


Why Are We Here?

- What is it?
  - How PWB's relate to ATE
    - Printed Wiring Boards – Automated Test Environment
  - Some Attributes
- Materials
- Let's take a break!
- Process flow and "How's it made?"
  - Including some videos of major processes
  - Hands-on display

What's in a Name?

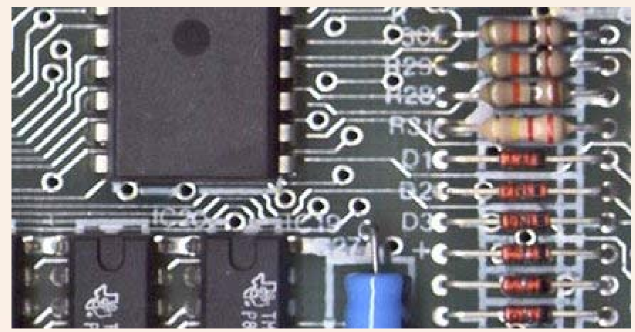
- PWB's
- PCB's
  - Printed Circuits Board
- DUT board, DIB, PIB, load board, or ATE board
  - Device Interface Board, Probe Interface Board



- Interface Board
  - Between Device Under Test and the Tester

What Is It?

- Wikipedia
  - A printed wiring board (PWB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate. PWBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer (outer and inner layers). Multi-layer PWBs allow for much higher component density. Conductors on different layers are connected with plated-through holes called vias. Advanced PWBs may contain components - capacitors, resistors or active devices - embedded in the substrate..



1980's PWB technology

"PCB Spectrum" by Bill Bertram - Bill Bertram. Licensed under CC BY-SA 3.0 via Commons -

What Is It?

- Simultaneously, a PWB is:
  - Mechanical Device
  - Electrical Device
  - Thermal Device

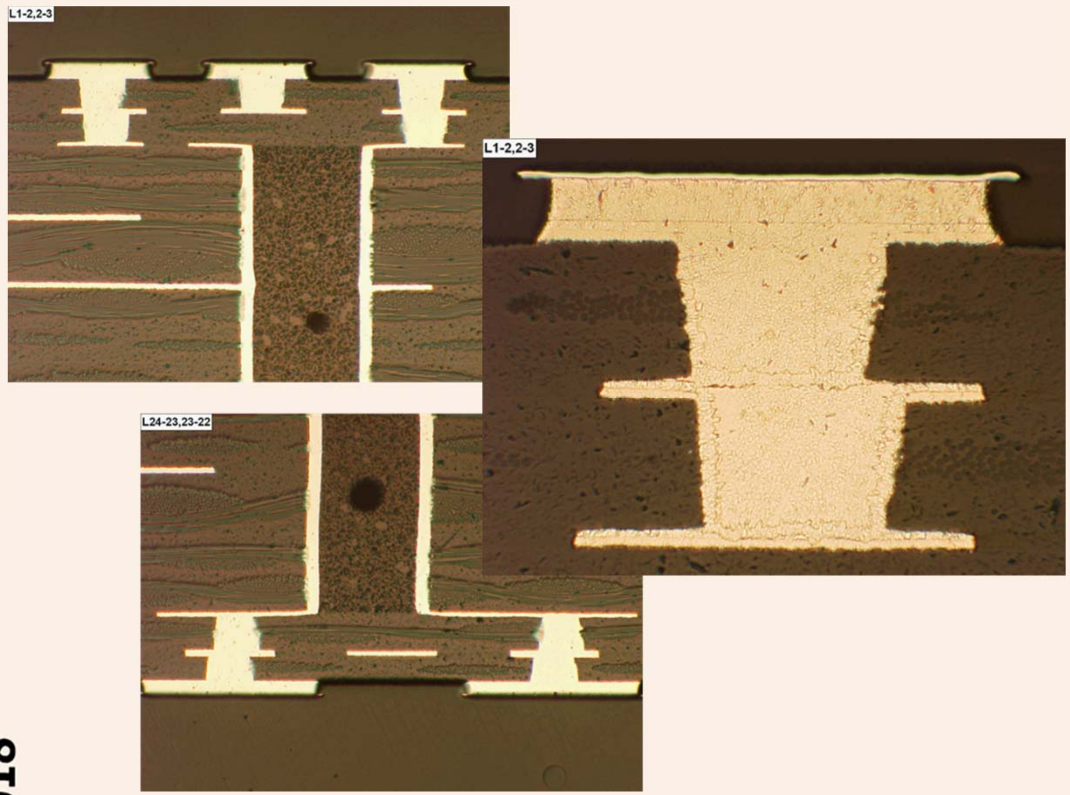
PWB Classifications

- There are two basic ways to form circuits on a PWB
- *Additive*
  - Formation is accomplished by adding copper to a bare PWB in the pattern and places desired
- *Subtractive*
  - The unwanted portion of the copper foil on the base substrate is etched away, leaving the desired pattern
- Our discussion today will focus on processes related to the latter method

PWB Classifications

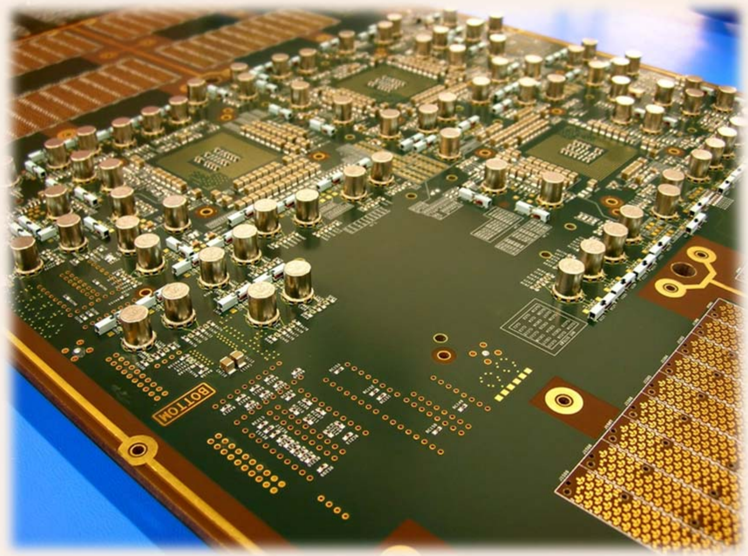
- Single-sided
  - Circuitry on one side only, components installed on back side
- Double-sided
  - Circuitry on both sides, plated thru holes, components on one or both sides
- Multilayer
  - To increase area for routing, multiple layers may be inside
    - Through holes, buried via’s or blind via’s may be employed to further increase circuit layout density

It’s all about making connections



The Marketplace

- Worldwide Market – 2007
  - $50B
- Worldwide Market – 2016
  - $62B
- North American Market – 2016
  - ~$3.2B
- ATE
  - $0.5B to $1.0B
    - Difficult to estimate



Today's Modern Load Board

Measuring Units Used in PWB Industry

Units	Micro Inches	Microns	Mils	MM	Inches	Angstroms
Micro Inch	1	0.025	0.001	0.000025	0.000001	250
Micron	40	1	0.04	0.001	0.00004	10,000
Mil	1000	25	1	.025	0.001	250,000
MM	40,000	1,000	40	1	0.04	100,000,000

Attributes of A PWB

Attribute	Type				ATE
Layer Count		2-40	40 to 60	60+	68+
Board Thickness		3.2mm	5.1mm	6.35mm	7.6mm+
Aspect Ratio	Plated Thru Hole	12:1	15:1	20:1	30+:1
	Blind Via	2:1	1:1	0.75:1	n/a
Line & Space	Inner Layer	100µ/100µ	75µ/75µ	50µ/50µ	50µ/50µ
	Outer Layer	125µ/125µ	75µ/75µ	50µ/75µ	50µ/50µ
Minimum Drill		200µ	150µ	<150µ?	100µ
Solder Mask Registration		100µ	75µ	50µ	<50µ

Attributes of A PWB (in inches)

Attribute	Type				ATE
Layer Count		2-40	40 to 60	60+	68+
Board Thickness		0.126	0.200	0.250	0.300+
Aspect Ratio	Plated Thru Hole	12:1	15:1	20:1	30+:1
	Blind Via	2:1	1:1	0.75:1	n/a
Line & Space	Inner Layer	0.004/0.004	0.003/0.003	0.002/0.002	0.002/0.002
	Outer Layer	0.005/0.005	0.003/0.003	0.002/0.003	0.002/0.002
Minimum Drill		0.008	0.006	<0.006	0.004
Solder Mask Registration		0.004	0.003	0.002	<0.002

Attributes of a Device

- Pitch
  - Device, trace, space, hole to copper
- Layers
  - Rows on a BGA device
- Hole Diameter
  - Function of device pitch
- Aspect Ratio
  - Ratio of thickness to hole diameter (think soda straw)

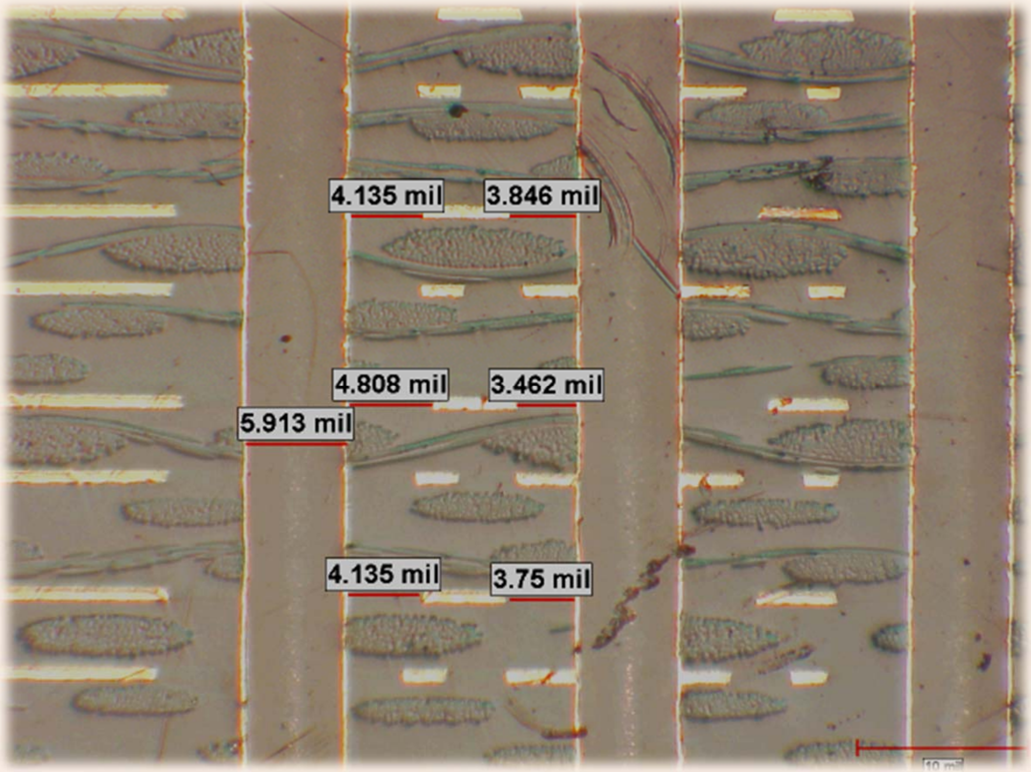
Attributes – By Device Pitch

- 1.0mm, 0.8mm, 0.5mm, 0.4mm ….
- Translates to other attributes
  - Line width
  - Spacing
  - Dielectric spacing
  - Hole to copper feature dimensions

Attributes by Device Pitch

	1.0mm (0.0394)	0.8mm (0.0315)	0.5mm (0.0197)	0.4mm (0.0157)
Pad	0.76mm (0.0299)	0.66mm (0.026)	0.35mm (0.0138)	0.3mm (0.0118)
Hole	0.37mm (0.0146)	0.3mm (0.0118)	0.15mm (0.0059)	0.1mm (0.0039)
Line	200µ (0.008)	200µ/125µ (0.008/0.005)	200µ/75µ (0.008/0.003)	200µ/50µ 0.008/0.002)
Hole 2 Copper	0.25mm (0.010)	0.18mm (0.007)	0.12mm (0.005)	0.1mm (0.004)
Aspect Ratio	Low	Medium	High	Extreme

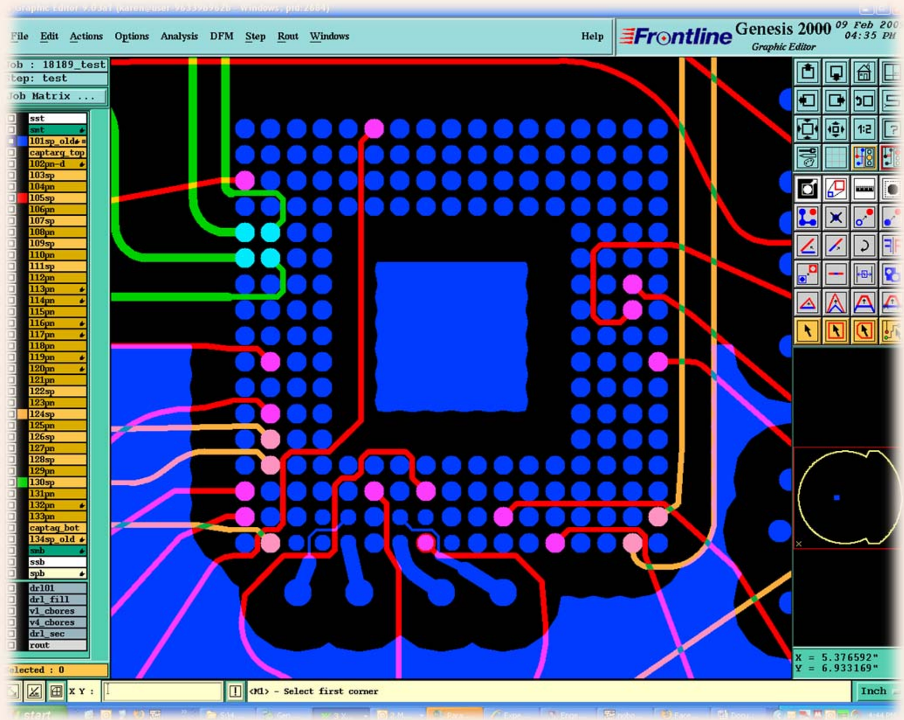
Hole to Copper Dimensions



Attributes - Layers

- Each row of a BGA device = one signal layer
- Signal layers need corresponding ground planes
  - Impedance control
- May need additional routing layers

Rows = Layers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Frontline
Genesis 2000
Graphic Editor
Inch

Attributes – Hole Diameter

- Drilled or finished hole diameter
- Human Hair
  - 40µ to 250µ (0.0015” to 0.010”)
  - 100µ is pretty average (0.004”)
- Today’s interface boards are drilled with a 100µ to 150µ drill bit (0.004” to 0.006”)
  - And smaller

Attributes – Aspect Ratio

- Ratio of the board thickness relative to drilled hole diameter
- 1.0mm device, 13:1
- 0.8mm device, 16:1
- 0.5mm device, 31:1
- 0.4mm device, 38:1
- 0.35mm device, >40:1

Let's Talk About Materials

- Wikipedia…A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, on a non-conductive substrate.

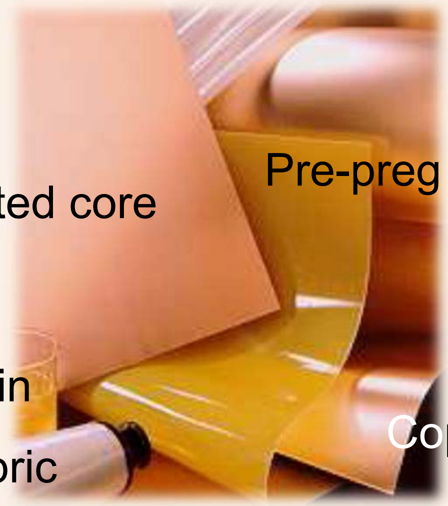
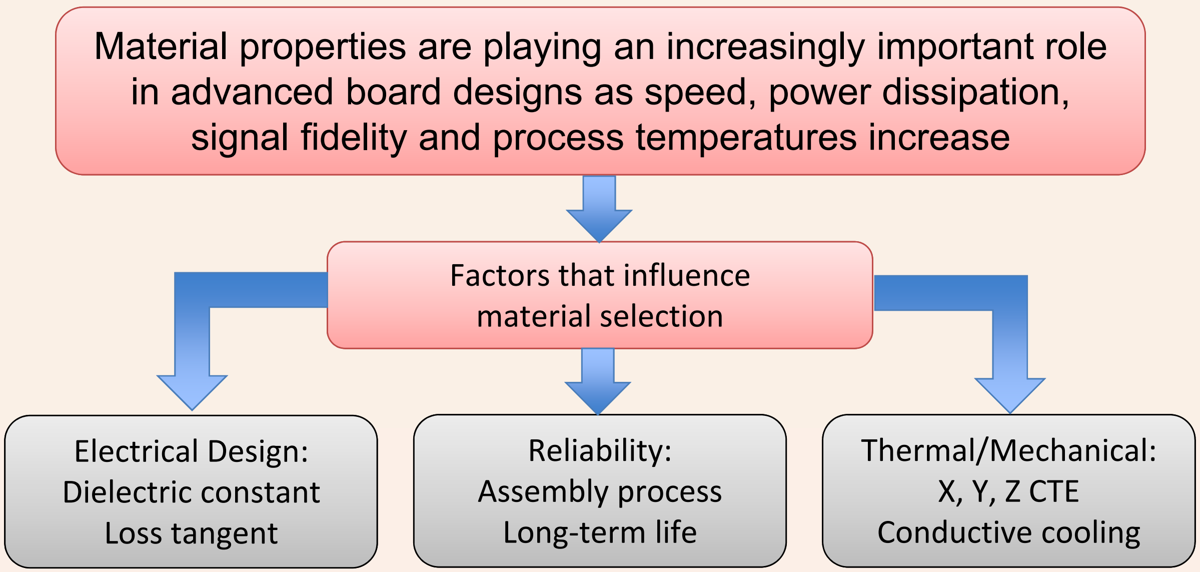


Photo courtesy of Isola

Materials & More



Laminates

- Pre-preg
  - Fiberglass cloth (woven)
  - Resin
- Copper foil
  - Electrodeposited (ED)

Photo courtesy of Isola

Why Copper?

- Copper is an excellent electrical conductor
- Low electrical resistivity
- Inexpensive metal
- Soft and easily workable
- Easily processed
- Patternable by photolithography
  – Using relatively benign chemistry

Copper Foil

- Copper is the dominant metal for interconnection use
- Specified by weight
  - ½ ounce per square foot
  - 1 ounce per square foot
- Corresponding thicknesses
  - 17u and 35u respectively
- Usually produced by electrolytic deposition on a mandril
  - 99.8% purity common
  - Thickness tolerance is approx. 10%

Materials – 'Pre-Preg'

<u>Glass Style 106</u>
Plain Weave
Count 56x56
Thickness: 40µ

<u>Glass Style 1080</u>
Plain Weave
Count 60x47
Thickness: 64µ

Photos courtesy of Isola

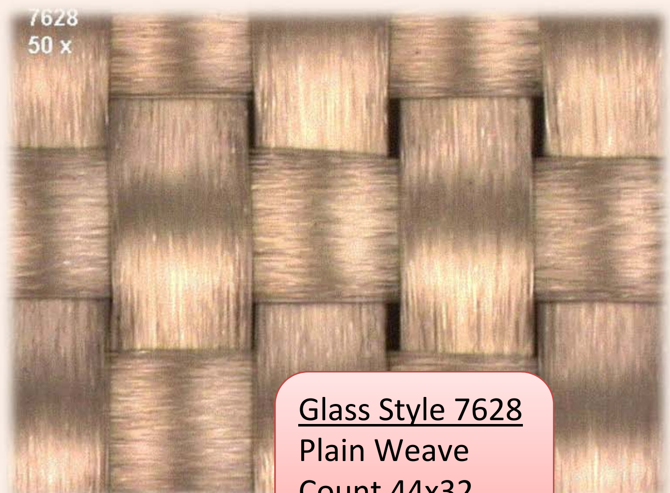
Materials – 'Pre-Preg'

Glass Style 2113
Plain Weave
Count 60x56
Thickness: 75µ

Glass Style 2116
Plain Weave
Count 60x58
Thickness: 100µ

Photos courtesy of Isola

Materials – ‘Pre-Preg’



<u>Glass Style 1652</u>
Plain Weave
Count 52x52
Thickness: 100µ

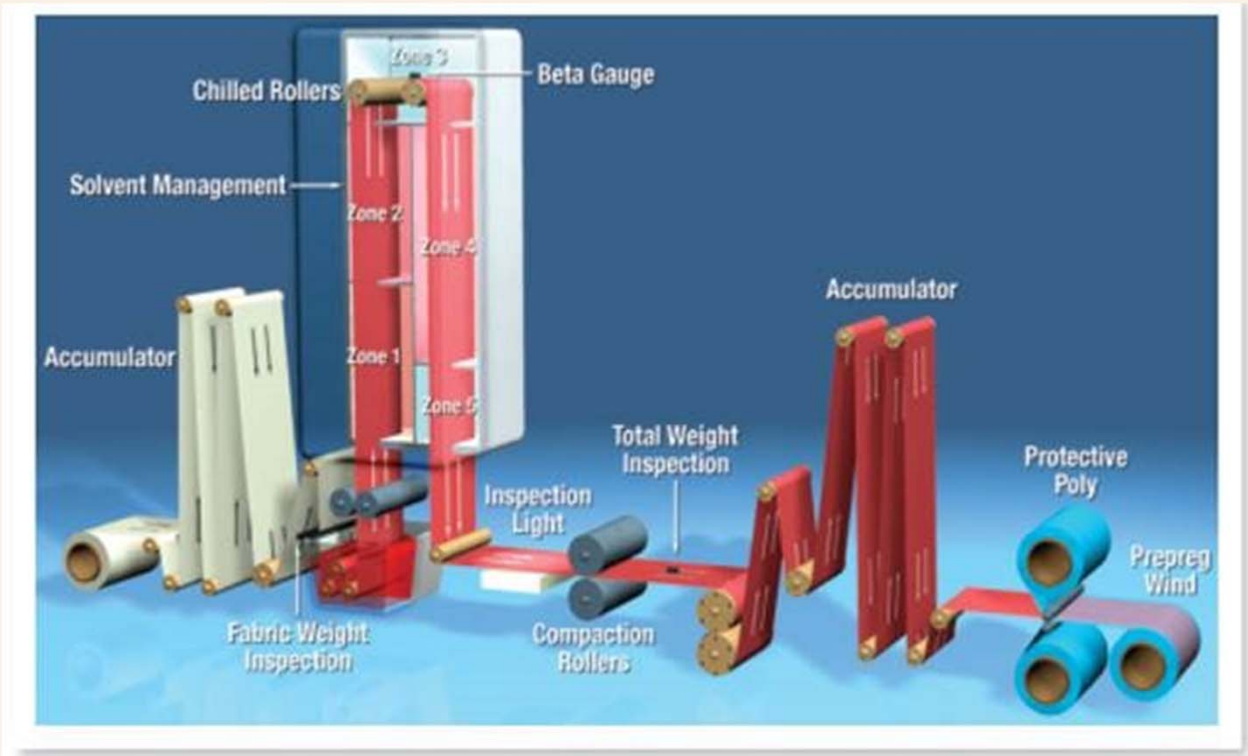
<u>Glass Style 7628</u>
Plain Weave
Count 44x32
Thickness: 170µ

Photos courtesy of Isola

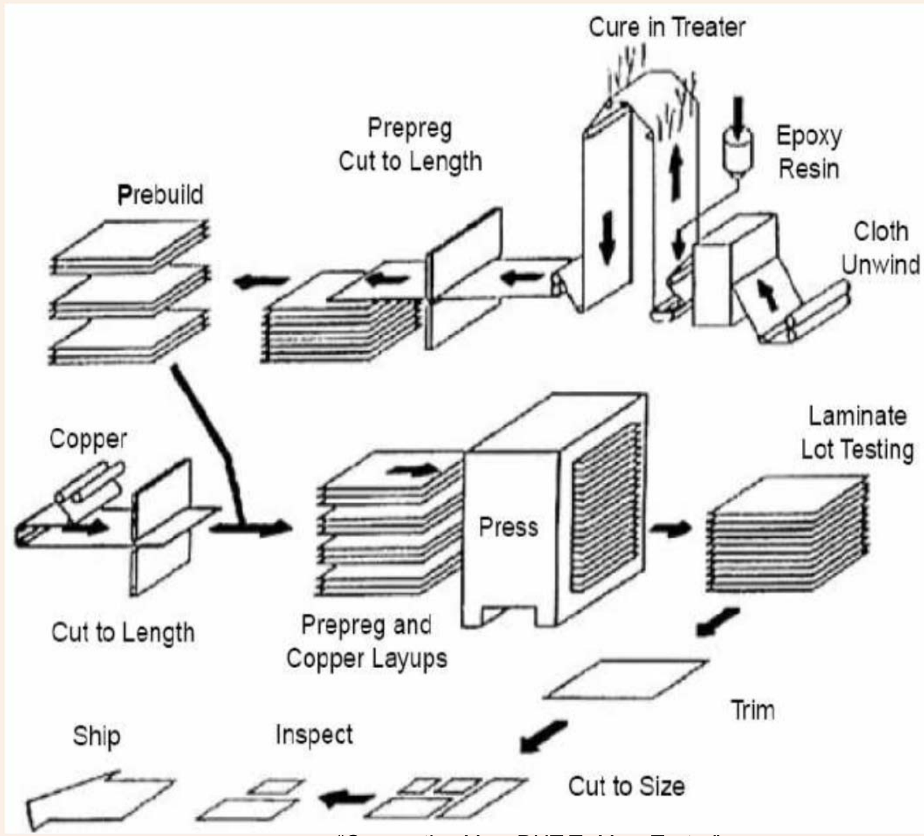
Laminate

- Enhanced FR-4's
- Modified Epoxies
- Teflon
- BT
- Polyimide
- Hybrid
- Too many to do justice to each supplier

Pre-Preg - how it's made

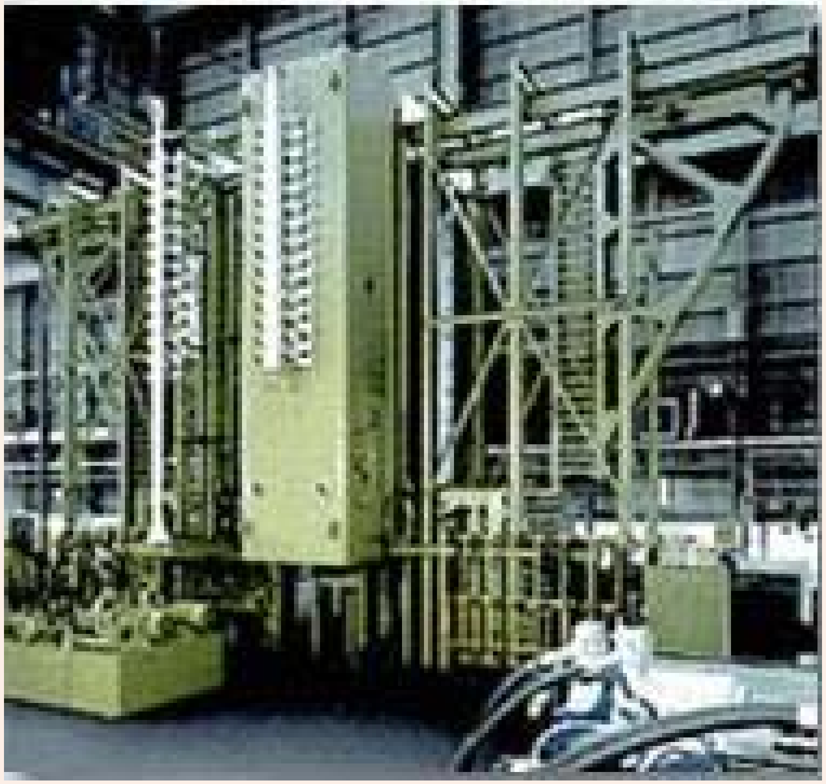


Laminate Process Flow



Laminate – How It's Made

Laminate – How It's Made



Laminate Construction (caveat emptor)

Thickness	Tolerance	Construction	Resin Content	E_r @ 1 MHz	E_r @ 10 GHz
0.008	0.001	1x 7628	44.4%	4.55	4.12
0.008	0.001	2x 2116	43.0%	4.54	4.11
0.008	0.001	1x 2116 1x 2113	48.6%	4.36	4.02
0.008	0.001	1x 7629	42.6%	4.38	4.12

Laminate Construction

- Know what you’re getting
- Understand the implications
- Electrically significant or not
- Mechanically significant!

Revision Date: March 2006

SPECIFICATION SHEET

SPECIFICATION SHEET #: IPC-4101/129
REINFORCEMENT: *1:* Woven E-glass *2:* N/A
RESIN SYSTEM: *Primary:* Epoxy
Secondary 1: Multifunctional epoxy *Secondary 2:* Modified Epoxy or Non-epoxy (max. wt. 5%)
FLAME RETARDANT MECHANISM: Bromine, RoHS Compliant *Minimum UL94 Requirement:* V-0
FILLERS (≥5%): N/A
ID REFERENCE: *UL/ANSI:* FR-4/129
GLASS TRANSITION (T_g): 170°C minimum
UL MAX. OPERATING TEMP: 130°C

Keywords: (For Search Only)
NOT Grade Requirement
See Section 7
Lead-Free FR-4
Low Z-axis CTE
High Decomposition Temperature
CAF Resistant

LAMINATE REQUIREMENTS

Laminate Requirement	Specification <0.50 mm [0.0197 in]	Specification ≥0.50 mm [0.0197 in]	Units	Test Method	Ref. Para.
1. Peel Strength, minimum A. Low profile copper foil and very low profile copper foil – all copper weights >17 µm [0.669 mil]. B. Standard profile copper foil 1. After thermal stress 2. At 125°C [257°F] 3. After process solutions C. All other foil – composite	AABUS 0.80 [4.57] 0.70 [4.00] 0.55 [3.14] AABUS	AABUS 1.05 [6.00] 0.70 [4.00] 0.80 [4.57] AABUS	N/mm [lb/in]	2.4.8 2.4.8.2 2.4.8.3	3.9.1.1 3.9.1.1.1 3.9.1.1.2 3.9.1.1.3
2. Volume Resistivity, minimum A. C-96/35/90 B. After moisture resistance C. At elevated temperature E-24/125	10^6 – 10^3	– 10^4 10^3	MΩ–cm	2.5.17.1	3.11.1.3
3. Surface Resistivity, minimum A. C-96/35/90 B. After moisture resistance C. At elevated temperature E-24/125	10^4 – 10^3	– 10^4 10^3	MΩ	2.5.17.1	3.11.1.4
4. Moisture Absorption, maximum	–	0.5	%	2.6.2.1	3.12.1.1
5. Dielectric Breakdown, minimum	–	40	kV	2.5.6	3.11.1.6
6. Permittivity at 1 MHz, maximum (Laminate & prepreg as laminated)* 1 MHz 1 GHz 10 GHz	5.4 5.2 AABUS	5.4 5.2 AABUS	–	2.5.5.2 2.5.5.3 2.5.5.9	3.11.1.1 3.11.2.1
7. Loss Tangent at 1 MHz, maximum (Laminate & prepreg as laminated)* 1 MHz 1 GHz 10 GHz	0.035	0.035	–	2.5.5.2 2.5.5.3 2.5.5.9	3.11.1.2 3.11.2.2
8. Flexural Strength, minimum A. Length direction B. Cross direction	– –	415 [60,190] 345 [50,040]	N/mm² [lb/in²]	2.4.4	3.9.1.3
9. Flexural Strength at Elevated Temperature, length direction, minimum	–	–	N/mm² [lb/in²]	2.4.4.1	3.9.1.4
10. Arc Resistance, minimum	60	60	s	2.5.1	3.11.1.5
11. Thermal Stress 10 s at 288°C [550.4°F], minimum A. Unetched B. Etched	Pass Visual Pass Visual	Pass Visual Pass Visual	rating	2.4.13.1	3.10.1.2
12. Electric Strength, minimum (Laminate & prepreg as laminated)	30	–	kV/mm	2.5.6.2	3.11.1.7 3.11.2.3
13. Flammability (Laminate & prepreg as laminated)	V-0 minimum	V-0 minimum	rating	UL94	3.10.2.1 3.10.1.1
14. Glass Transition Temperature	–	170 minimum	°C	2.4.24 2.4.25	3.10.1.6
15. Decomposition Temperature	–	340 minimum	°C	ASTM D3850 (5% wt loss)	3.10.1.10

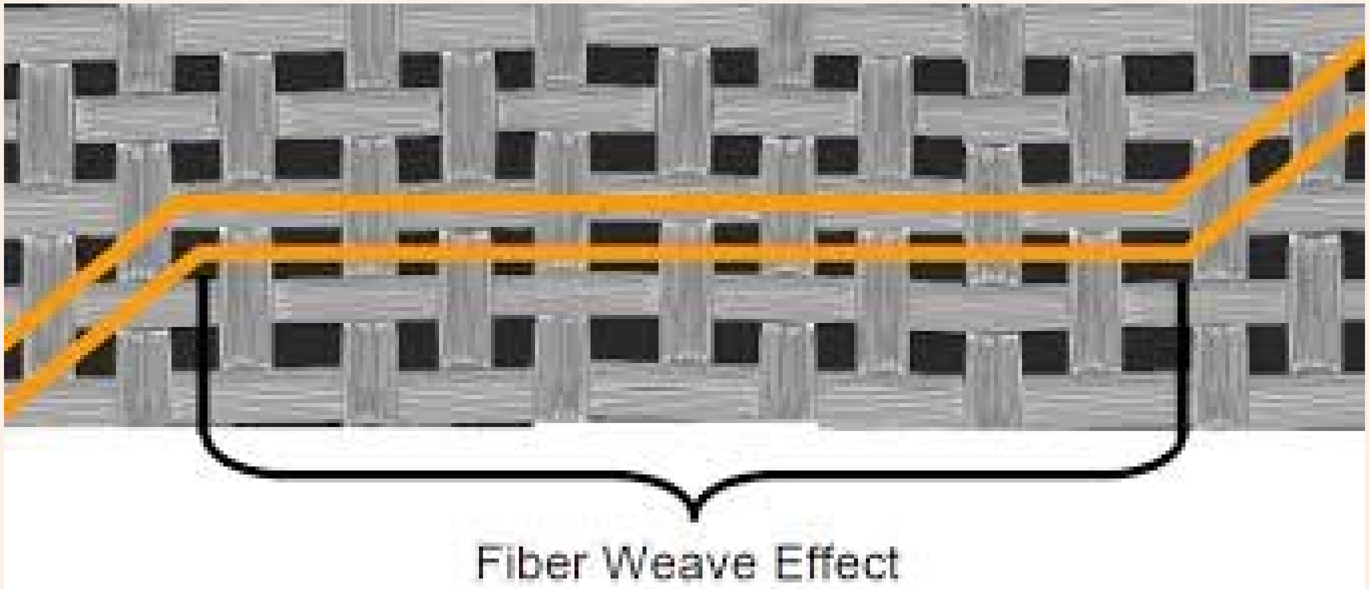
Material Properties

- Mechanical and Thermal
  - Peel strength
  - X-Y CTE
  - Z CTE
- Tg
  - DSC
  - TMA
  - DMA

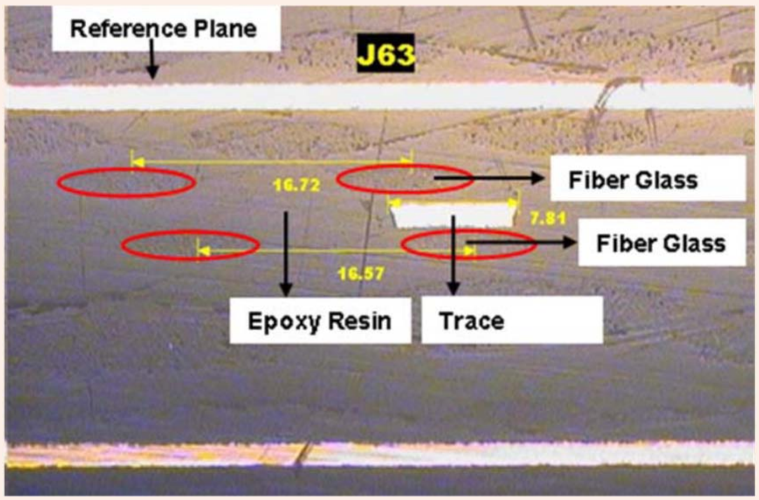
Material Properties

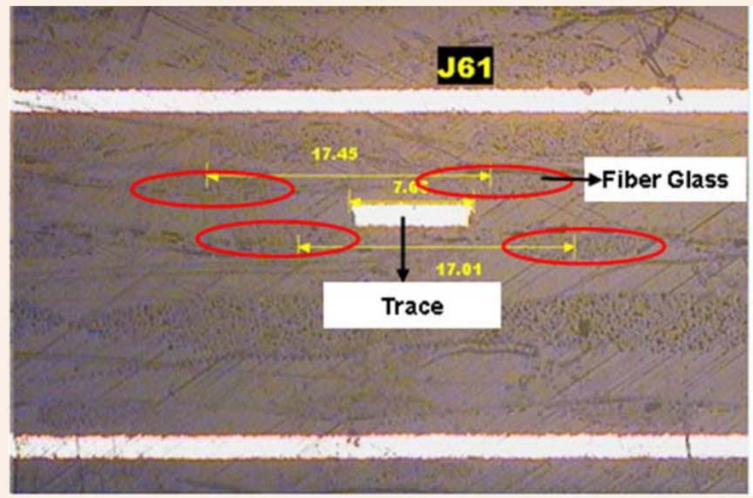
- Electrical
  - Dielectric Constant or
- ε_r Epsilon-sub-r (or relative permittivity)
  - The dielectric constant is a ratio of the capacitance of a capacitor in which a particular insulating material is the dielectric, to the capacitance of the capacitor in which a vacuum is the dielectric.
  - Also known as E-sub-r
- Effective Permittivity

Material Properties – Weave Effect

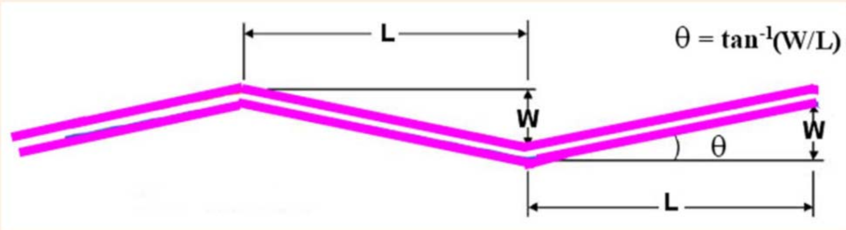


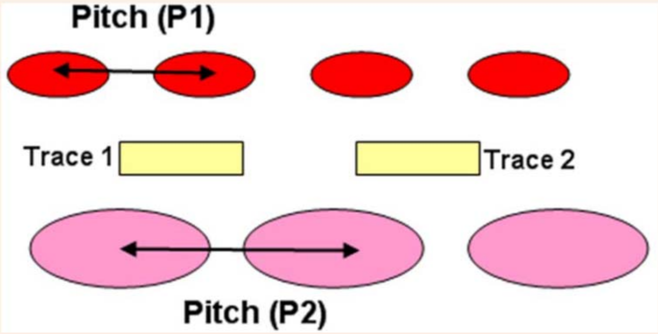
Material Properties – Weave Effect

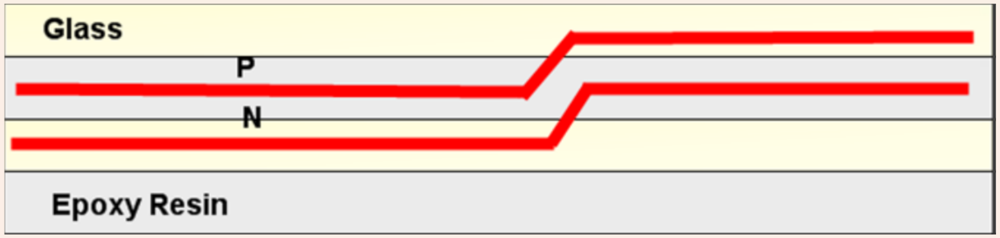




Combating Weave Effect

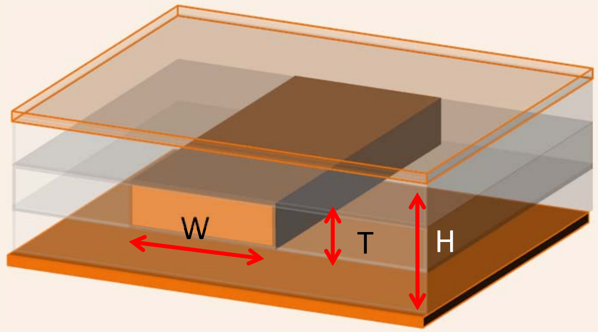






Material Properties – Trace Variabilities

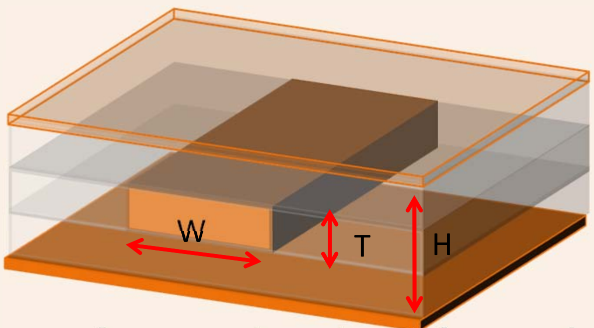
- Dry film etch tolerance is +/-12μ; therefore as W decreases Z0 error increases.
- As H decreases, tolerance changes from +/- 10% to ~+/-15μ. H also varies within a sheet +/- 10μ.
- T does not vary significantly, but a 'tall' T results in higher resin flow around the trace and makes the final thickness H somewhat less predictable.
- A 'tall' T is also prone to under etch, which influences Z0.



- Fiberglass reinforced materials are not homogenous, and εr *is not* constant in the material.

*Z0 or Z naught = impedance

Material Properties – Trace Variabilities



- Important: driven by etch variation and by heterogeneous materials Z0 varies as a function of distance.

100um example in 1/2 Oz copper:

Trace Etch Width

	min	nominal	max
	88 um	100 um	112 um
	53.2 Ω	50.1 Ω	47.4 Ω

Height

	min	nominal	max
	201 um	223 um	245 um
	47.0 Ω	50.1 Ω	53.0 Ω

Combined Error

	min	nominal	max
	44.3 Ω	50.1 Ω	56.1 Ω

Materials Chart

	Mwave 1000	Mwave 2000	Mwave 3000	Mwave 4000	Meg 6	Rogers 4350	N4000 -13	N4000 -13SI	N4800 -20	N4800 -20SI	Astra MT7	Tachyon 100
Mech												
Peel strength												
After float	6.6	6.6	5.5	5.5	.8kN/m	5	7.5	7.5	7	7	5.7	
At elev. temp	5.6	5.6	4.4	4.4	n.a.	n.a.	8.1	8.1	6.5	6.5	n.a.	5.5
After exp./proc	5.3	5.3	5	5	n.a.	n.a.	9	9	7	7	n.a.	5.5
X-Y CTE	10-14	10-14	10-14	10-14	14-16	10-12	10-14	10-14	10-14	10-14	12	15
Z CTE α1	55	55	55	55	45	32	70	70	27	31	60	45
Z CTE α2	260	260	260	260	260	n.a.	280	280	205	210	300	250

α1, 50C to Tg; α2, Tg to 260C

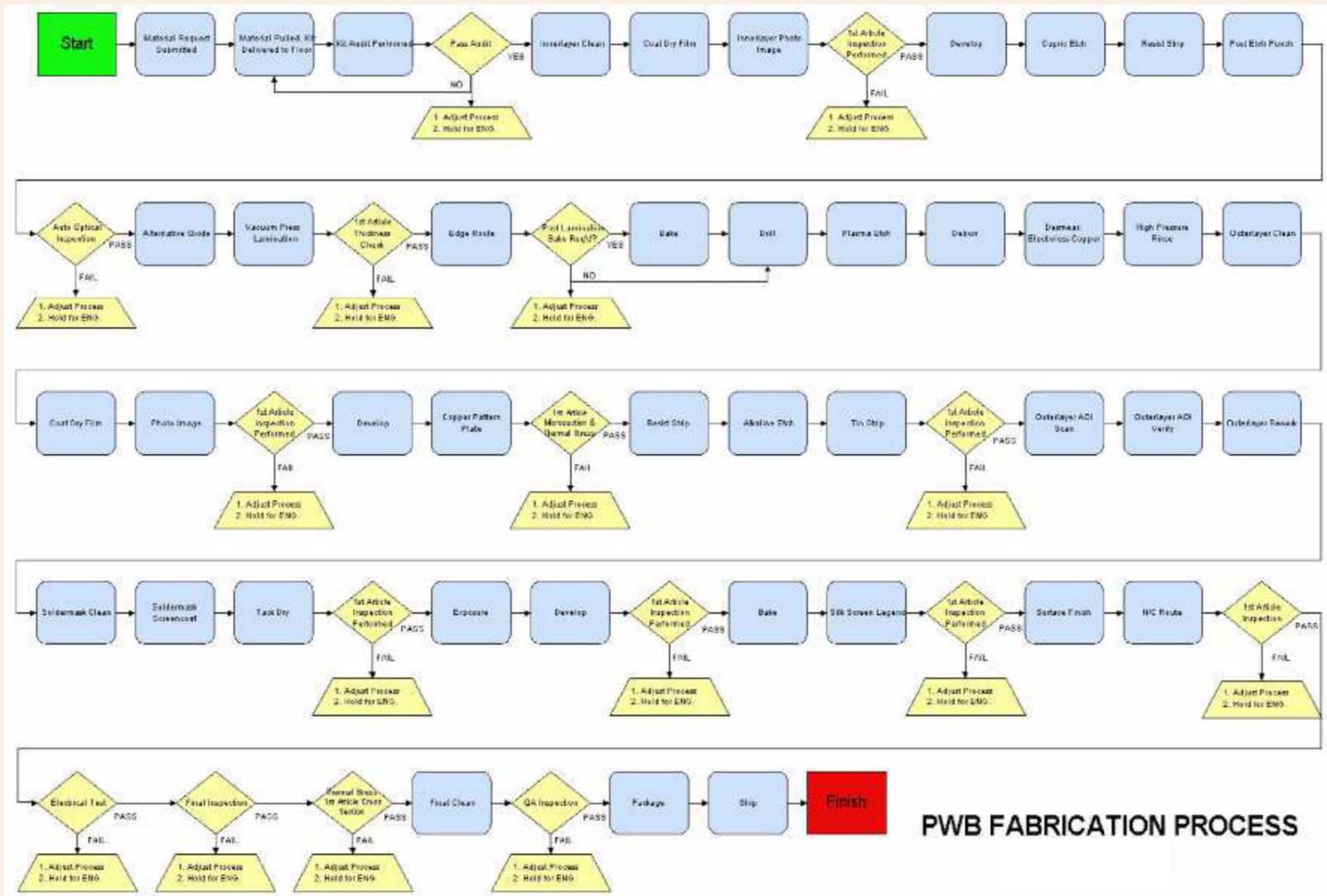
Materials Chart

	Mwave 1000	Mwave 2000	Mwave 3000	Mwave 4000	Meg 6	Rogers 4350	N4000 -13	N4000 -13SI	N4800 -20	N4800 -20SI	Astra MT7	Tachyon 100
Electrical												
Dk												
2 Ghz	3.7	3.4	3.8	3.5	3.71	n.a.	3.7	3.2	3.7	3.55	3	3.04
10 Ghz	3.7	3.4	3.8	3.5	3.61	3.48	3.7	3.3	3.8	3.4	3	3.02
Df												
2 Ghz	0.004	0.003	0.0032	0.002	0.002	0.0031	0.009	0.008	0.007	0.0055	0.0017	0.0021
10 Ghz	0.0055	0.004	0.0048	0.0028	0.004	0.0037	0.008	0.007	0.0075	0.006	0.0017	0.0021
Thermal (Tg)												
TMA	215	215	170	170	n.a.	280	200	200	180	180	n.a.	180
DMA	240	240	200	200	210	n.a.	240	240	210	210	n.a.	220
DSC	n.a.	n.a.	n.a.	n.a.	185	n.a.	210	210	200	200	200	185

DSC, Differential Scanning Calorimetry; TMA, Thermomechanical Analysis; DMA, Dynamic Mechanical Analysis.

Before We Continue to The Process

http://www.doggonedelightfulstampin.com/.a/6a01a511621c4d970c01b7c7e33543970b-popup

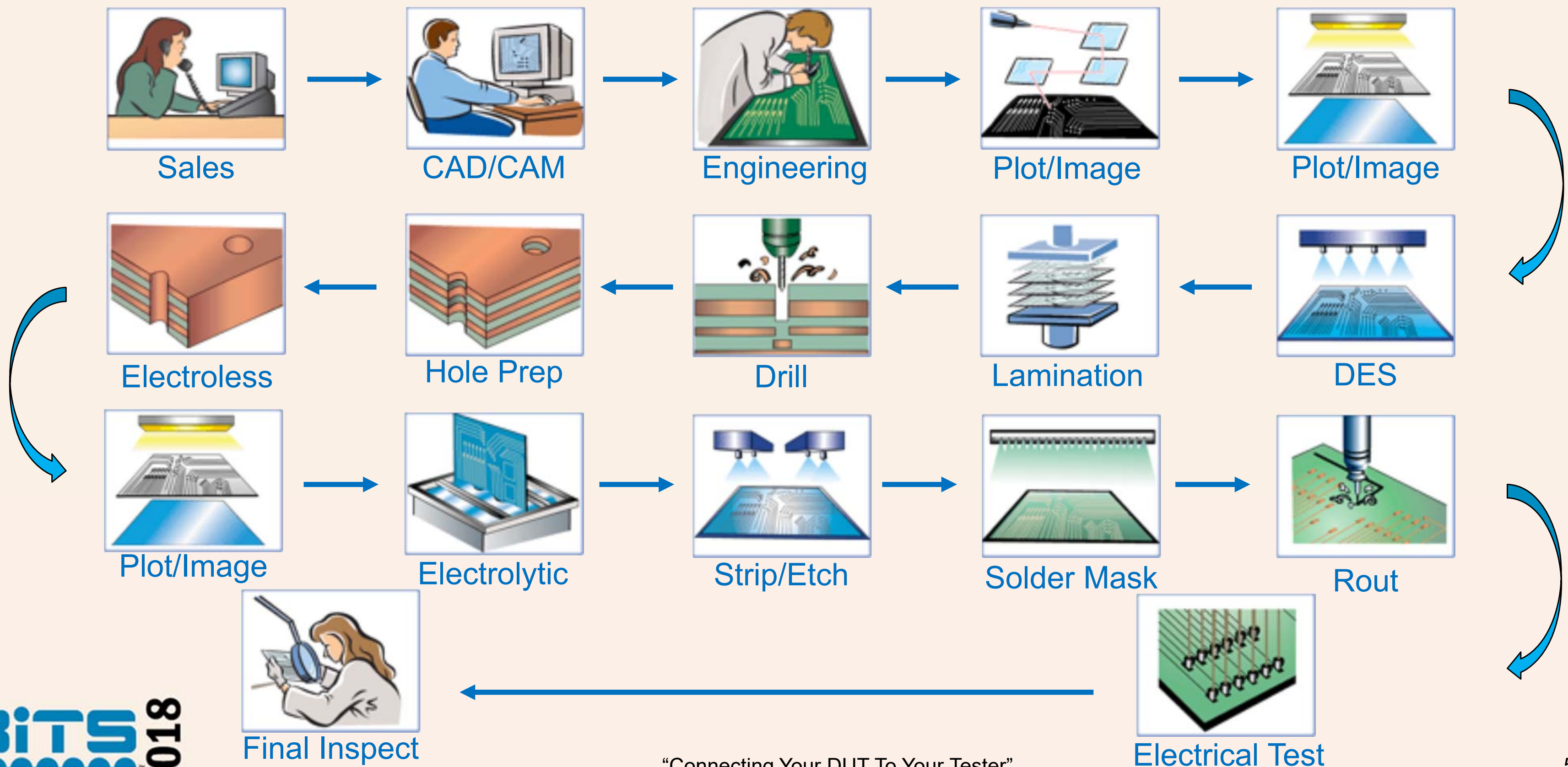


Start
Material Request Submitted
Kit Audit Performed
Pass Audit
YES
NO
1. Adjust Process
2. Hold for ENG
Innerlayer Clean
Coat Dry Film
Innerlayer Photo Image
1st Article Inspection Performed
PASS
FAIL
Develop
Cupric Etch
Resist Strip
Post Etch Punch
Auto Optical Inspection
Alternative Oxide
Vacuum Press Lamination
1st Article Thickness Check
Edge Route
Bake
Drill
Plasma Etch
Deburr
Desmear Electroless Copper
High Pressure Rinse
Outerlayer Clean
Coat Dry Film
Photo Image
Copper Pattern Plate
Resist Strip
Alkaline Etch
Tin Strip
Outerlayer AOI Scan
Outerlayer AOI Verify
Soldermask Clean
Soldermask Screencoat
Tack Dry
Exposure
Silk Screen Legend
Surface Finish
NC Route
1st Article Inspection
Electrical Test
Final Inspection
Final Clean
QA Inspection
Package
Ship
Finish
PWB FABRICATION PROCESS

Confused?

Flickr: Bex Ross

Not to Worry, a Simpler Way



“Connecting Your DUT To Your Tester”

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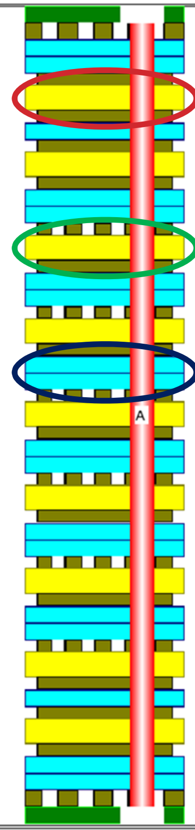

Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type DK / DF
SM-1	0.0005		SM	Spray LPI	3.20 / 0.0000
L-1, TOP	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-2, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-3, PWR1	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-4, PWR2	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-5, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-6, SIG1	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-7, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-8, SIG2	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-9, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-10, SIG3	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-11, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-12, SIG4	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-13, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-14, SIG5	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-15, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-16, SIG6	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-17, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-18, PWR3	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-19, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-20, BOT	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
SM-2	0.0005		SM	Spray LPI	3.20 / 0.0000
	0.1517	Total Calc. Thickness			
	0.1520	Incl.Plating After Lamination	+0.0152 +	-0.0152 -	

Drill/Rout Files: A: DR-1

BiTS Burn-in & Test Strategies Workshop 2018

"Connecting Your DUT To Your Tester"

The Process – Inner Layer Imaging

- Photo resist application
- UV Exposure
  - Laser Direct Imaging (LDI)
  - Collimated light & film
    - Polymerizes resist
- Develop
  - Removes non-polymerized resist

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The Process – Inner Layer Imaging

- Etch & Strip
- Removal of base copper
  - Non-polymerized area
- Various chemistries available
  - Ammonia based
  - Cupric chloride based
- Resist removal

The Process – Automatic Optical Inspection

- Post-Etch Punch
  - Registers all layers to common optical targets
  - Slots added for tooling purposes
- AOI
  - Data downloaded from CAM
  - Core layer scanned
  - Compared to CAM data
  - Verification

The Process – Oxide Treatment

- Copper Surface Preparation
  - Adhesion promotion
    - Added bonding strength
  - Reduced oxide
    - Pink ring elimination
  - Alternative oxide
    - Variety of materials
    - Multiple or sequential laminations

The Process – Layup & Lamination

- Registration and stacking of cores
  - Process combines cores, pre-preg and copper foil
    - Multiple times thru this process may be required
      - Simple thru-hole vs. sequential lamination
- Pin lamination
  - Registration or layer to layer alignment
- Vacuum chamber
- Heat, pressure, time
- Tightly controlled process window

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	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-6, SIG1	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-7, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-8, SIG2	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-9, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-10, SIG3	0.0006		Cu - Std	.5	SIGNAL
	0.0080	A	HTFR4	0.008	3.82 / 0.0000
L-11, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
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	0.1520	**Incl.Plating After Lamination**	**+0.0152** +	**-0.0152** -	

Drill/Rout Files: A: DR-1

Engenix® by Cimnet Systems, Inc. © 2002-2008

The Process - Drill

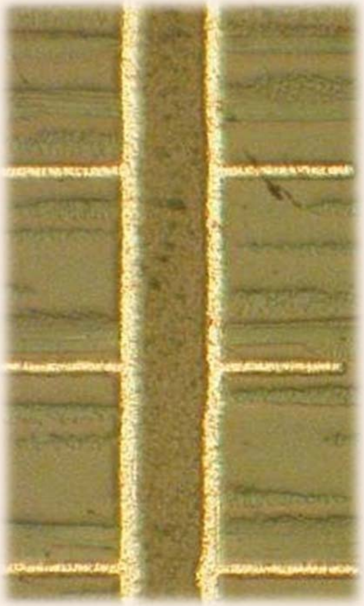
- Mechanical hole formation
  - 100µ – 150µ typical
- Opto-mechanical positioning
  - Glass scales
- Real-time drill bit analysis
  - Diameter
  - Run-out
  - Broken bit detection
- Stub drilling or back drilling

The Process - Drill

- Laser hole formation
  - Microvias down to 25µ
- Opto-mechanical positioning
  - Blind vias
  - Buried vias

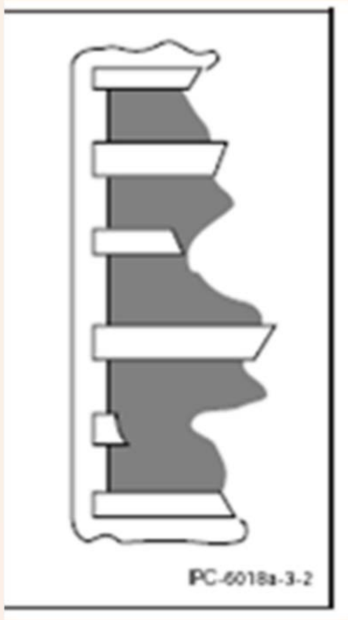
The Process – Hole Prep & Copper Plate

- Desmear
  - Removes epoxy smear from interconnects
    - Created during drill operations
  - Chemical removal



The Process – Hole Prep & Copper Plate

- Etchback
  - Different from desmear
  - Removes epoxy resin from dielectric space
  - May include a glass etch
  - Three point connection
    - Some materials resistant to previous chemical process



The Process – Hole Prep & Copper Plate

- Electroless copper deposition
- Seed layer
  - Prepares dielectric and interconnects for subsequent plating operations
  - 30 micro-inches – 40 micro-inches followed by copper plating
  - 75 micro-inches – 125 micro-inches to prep for imaging process
- Unfriendly chemistry
- Inherently unstable

The Process – Hole Prep & Copper Plate

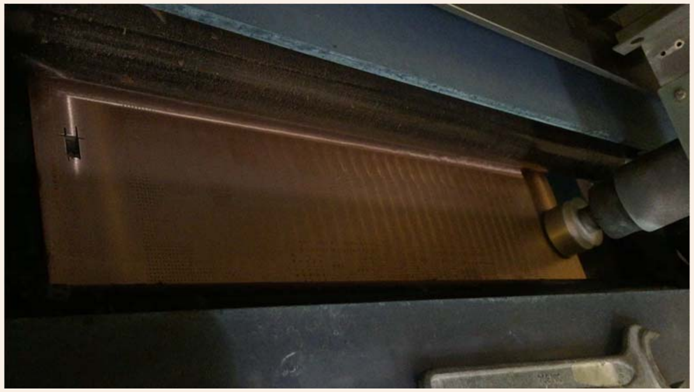
- Carbon
- Graphite
- Palladium
- Electroless Nickel
- Conductive Polymer
- Non-Formaldehyde-Based Electroless Copper

The Process – Hole Fill

- Fill to create flat surface
  - Needed for socket touchdown
- Vacuum assist
- High aspect ratio
- Blind vias

The Process - Planarization

- Fill to create flat surface
  - Needed for socket touchdown
- Vacuum assist
- High aspect ratio
- Blind vias
- Planarize the surface



The Process – Outer Layer Imaging

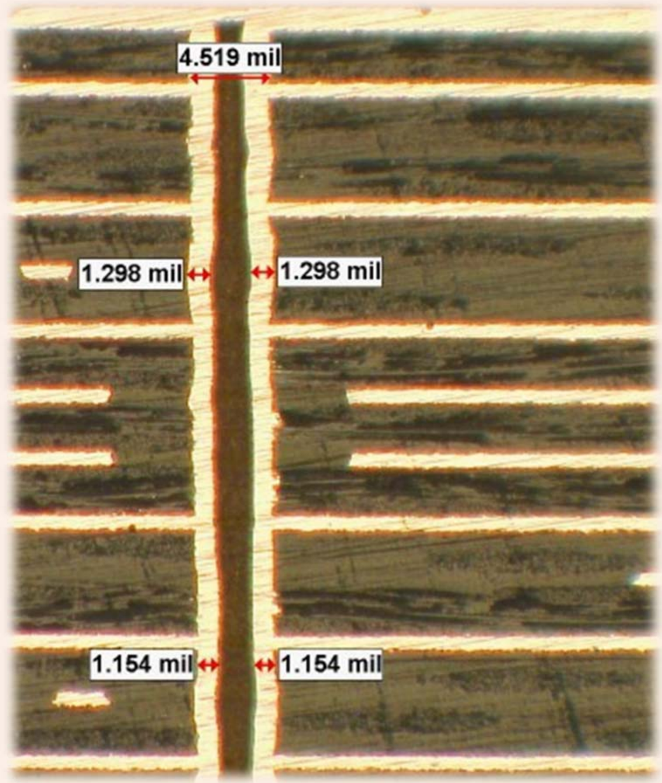
- Reversed from inner layer imaging
- Plating resist, not etch resist
- Photo-resist application
- UV Exposure
  - Film and collimated light
  - LDI or Laser Direct Imaging
    - Polymerizes photo-resist
- Develop
  - Removal of non-polymerized resist

The Process – Copper-Nickel-Gold Plating

- Electroplating
  - Chemistry (electrolyte solution)
  - Power rectifier
    - Rectifier converts AC to DC
  - Anode (copper)
  - Cathode (PWB panel)

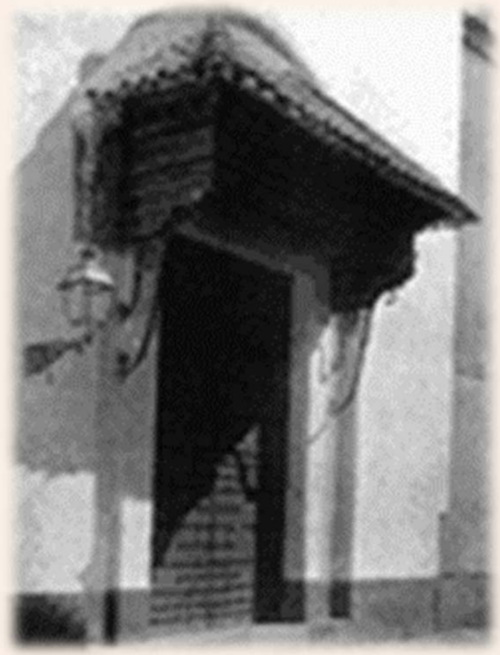
The Process – Copper-Nickel-Gold Plating

- 1 mil (25 micron) minimum copper thickness in holes
- Minimize surface buildup
- Aspect ratio
  - Through holes or microvias
- Robust and survivable
- Etch resist



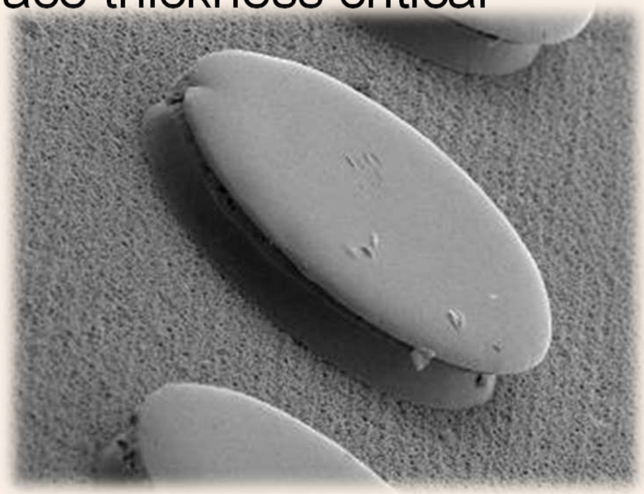
The Process – Outer Layer Etch

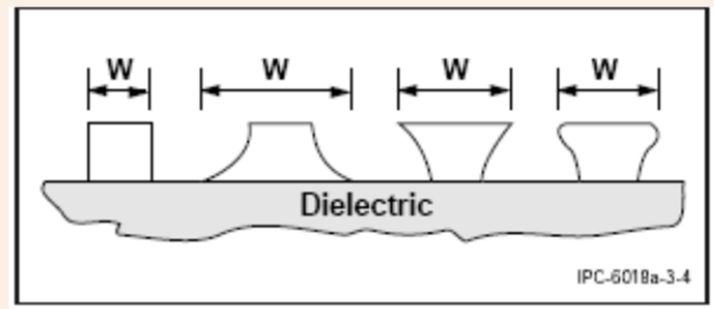
- Define the outer layer(s) pattern
  - Removal of base copper
  - Defines lines, pads, other features
  - Impedance control
- Nickel / Hard Gold typical ATE finish
- Etch factors and 'overhang'
- Other finishes available

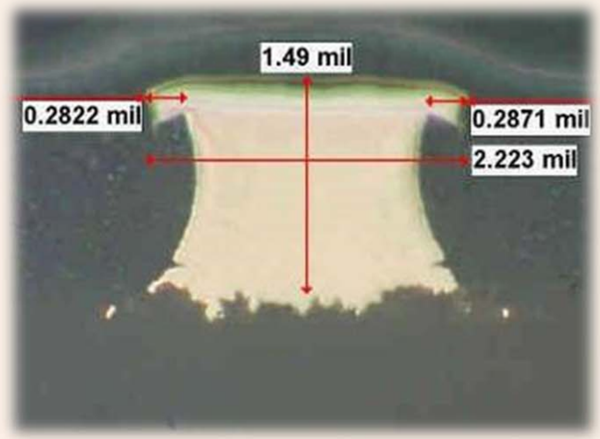


The Process – Outer Layer Etch

- Overhang
  - Depends on surface finish
  - 1:1 thickness
  - Surface thickness critical







"Connecting Your DUT To Your Tester"

The Process – Electrical Test

- Direct measurement for first board
  - Indirect measurement of subsequent boards
- Isolation and continuity
- Capacitive or electromagnetic coupling
  - Broken traces = reduced coupling
  - Shorted traces = increased coupling
- Trace to ground (increased degree of confidence
- Adjacency analysis

“Connecting Your DUT To Your Tester”

The Process – Solder Mask

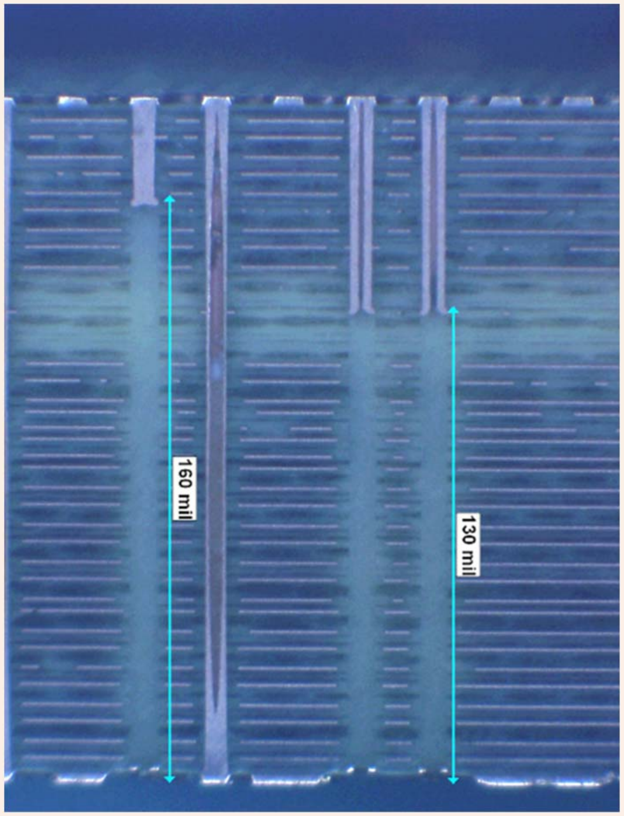
- Epoxy based coating
  - Available in colors and clear
- Surface protection
- Solder resist, as the name implies
- Product identification
- Liquid Photo-imageable
  - Spray coated or screen flood
- Dry film still in use

The Process – Silk Screen or Legend

- Assembly nomenclature or legend
- Available colors
- Product identification
- Screen print
- Inkjet

The Process - Depanelization

- Secondary Drill (non-plated holes)
- Back drill or stub drill
- Counterbores / countersinks
- Slots
- Routing



The Process – Final Inspection

- Visual and dimensional
- Cosmetic defects
- Impedance testing
- Cross sections
- Other measurements and certifications

May this information help you weather your PWB storms

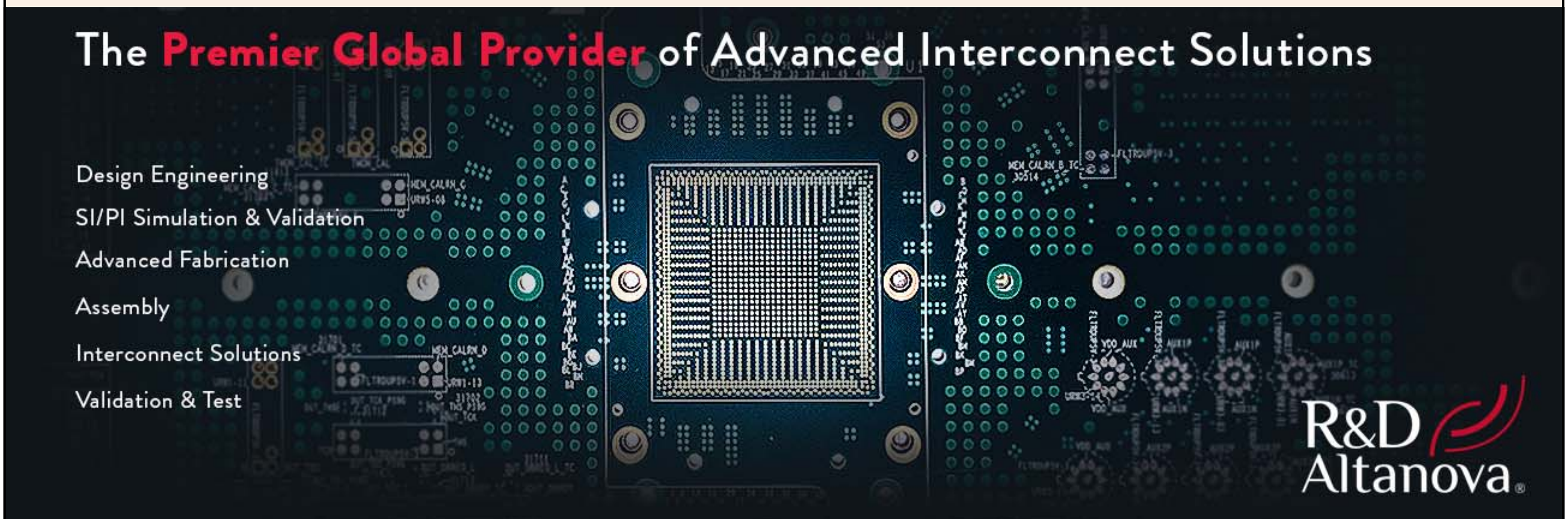
https://www.pinterest.com/source/anchorcharters.com.au/

About Us – R&D Altanova

- Founded in 1969
- Privately owned and operated
- Full Turn-Key Supplier
  - SI/PI Engineering
  - Design
  - Fabrication
  - Assembly
  - Sockets and Interconnects

Thank You!

- Tom Bresnan – tbresnan@rdaltanova.com – 732-549-4554 x3110



- Visit our website – www.rdaltanova.com