NINETEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop™

March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

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SAMSUNG ELECTRONICS

A new methodology to improve power integrity of high parallelism probe card

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Introduction

BACKGROUND

• Probe Card is a hardware that is connected physically and electrically between ATE (Automatic Test Equipment) and chips on the wafer test.

•Number of chips per probe card continues to increase. Limited channels in ATE are divided into several channels within the probe card.

•The power level of a divided channel would be dropped. That often makes problems when testing chips.

• In this paper, we suggest a new design to improve the power integrity of the divided channel.

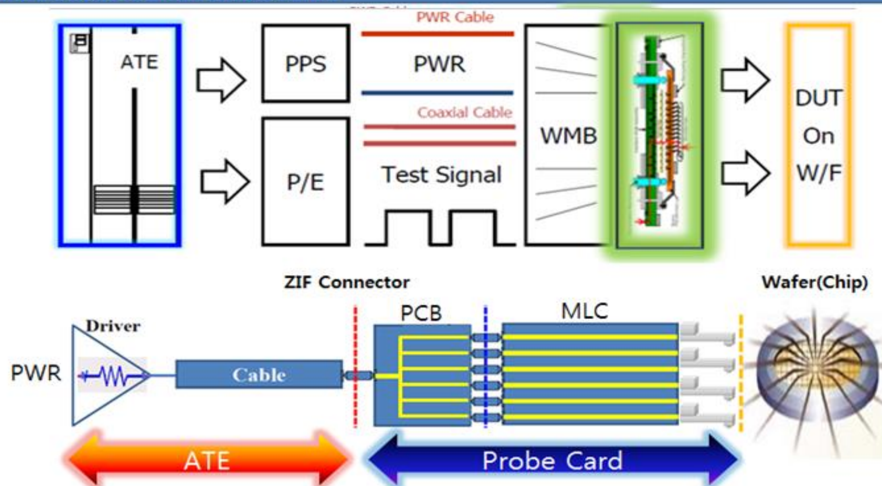

Fig1. Structure & Divided Channel of Probe Card

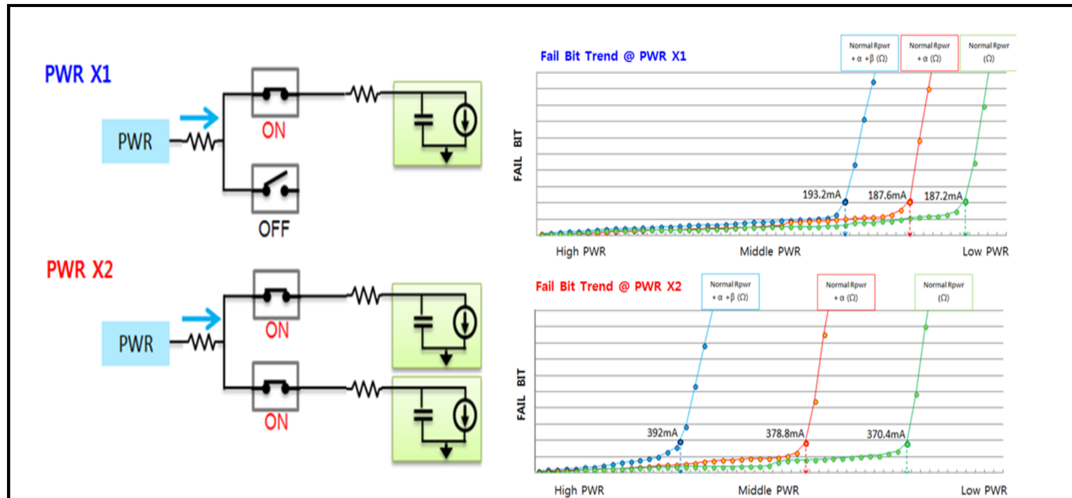

Fig2. Chip Test VDD Margin @ PWR Channel Branch

Solution

Change the sensing point of power channel.

• The sensing point of power channel is changed from ZIF to the power relay input terminal as shown Fig3. Because the sensing point is closer to the DUT than before, it enables the DUT to be given more precise power level.

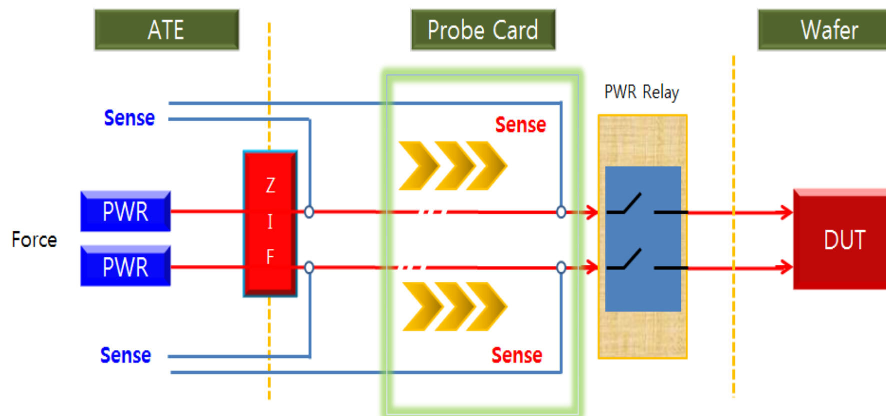

Fig3. Change the sensing point to be closer to the DUT

Change the placement of power relay.

• The power relay position is moved from the edge side on PCB top plane to the center side on PCB bottom plane as shown Fig4.
This method affects the improvement of power integrity by reducing the resistance of the power channel.

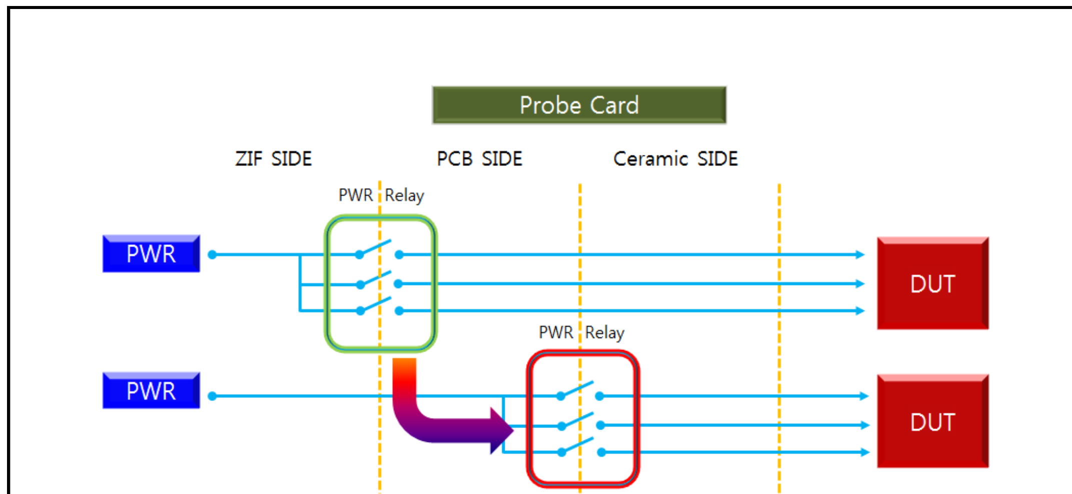

Fig4. Chip Test VDD Margin @ PWR Channel Branch

Result & Conclusion

• To improve power integrity of a divided channel, it was proposed to apply the sensing point and power relay to be closer to the DUT.
After these solutions was applied, the resistance of power channel was dramatically decreased as shown Fig5. It was confirmed that power integrity problem was improved when these methods were applied.

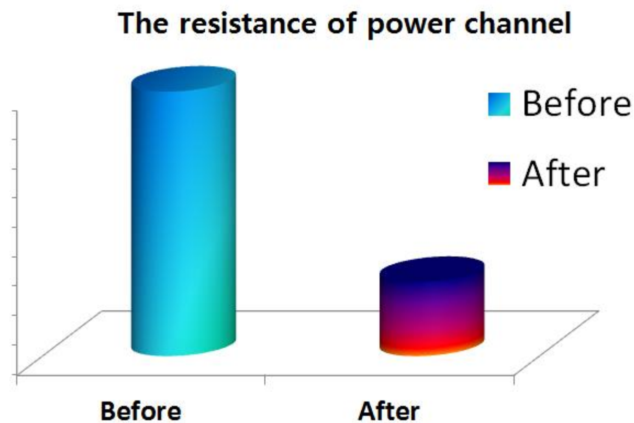

Fig5. Rpwr value of before and after improvement