# NINETEENTH ANNUAL Burn-in & Test Strategies Workshop

## March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel Mesa, Arizona

Archive



## **COPYRIGHT NOTICE**

The presentation(s)/poster(s) in this publication comprise the Proceedings of the 2018 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2018 BiTS Workshop. This version of the presentation or poster may differ from the version that was distributed in hardcopy & softcopy form at the 2018 BiTS Workshop. The inclusion of the presentations/posters in this publication does not constitute an endorsement by BiTS Workshop or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by BiTS Workshop. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop. All rights reserved.

## www.bitsworkshop.org

## **BiTS 2018**

## **Poster Session**



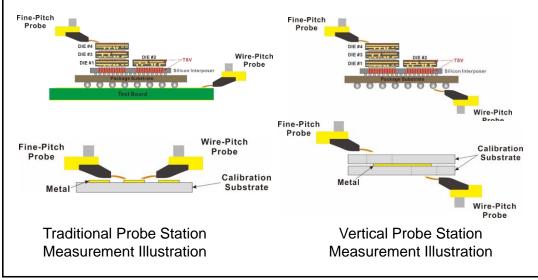


### An Innovative Vertical Probing System for High Speed/Frequency Applications

Oliver Chiu<sup>1</sup>, Duncan Huang<sup>1</sup> and Sung-Mao Wu<sup>2</sup> <sup>1</sup>Jthink Technology, Ltd 81148, Taiwan <sup>2</sup> Micro Electronic Packaging Laboratory, Department of Electrical Engineering, National University of Kaohsiung, 81148, Taiwan

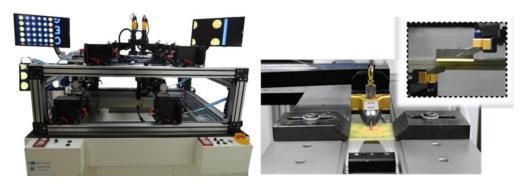
#### Abstract

The Moore's Laws is the most important rules in semiconductor industry. As we know the physical limitation of gate width may oncoming soon. Therefore, more than Moore solutions are developed in recent years, like 2.5D/3D IC, PoP(package on package), and SiP(system in package). The package design becomes more complicated in multi-layer substrate technology/process. Meanwhile the designer need to take care of the SI(signal integrity) and PI(power integrity) seriously by simulation and measurement on high speed and high frequency devices. The traditional probing system can't measure directly because of coplanar design base on wafer applications. We develop the vertical probing system and calibration kits for advance package design applications in order to solve measurement illustration.



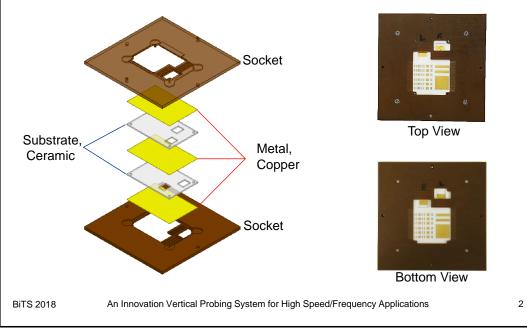
#### **Vertical Probing System**

Most importance of vertical probing system is making RF probes aim to opposite direction which rotate an arm to place the probe below DUT and make probe tip upward. When the DUT put on the probing system, the probes can contact single pad on the top layer and single pad on the bottom layer pad at same time.



#### Calibration Kit for Vertical Probing System

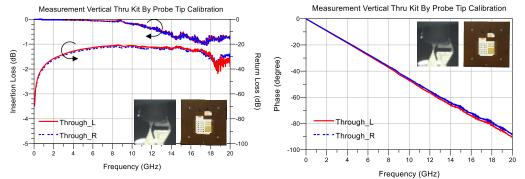
For the high speed/frequency applications, considering on measurement accuracy that use SOLT calibration method with open, short, load, through elements to have a standard definition table in vector network analyzer. The through element is a key parameter for multi-port measurement that design by metal non-exchanged layer structure to avoid the bandwidth limitation from the resonances of vias in vertical layer stack.



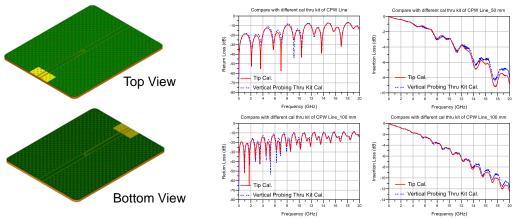
#### Burn-in & Test Strategies Workshop www.bitsworkshop.org

#### **Measurement and Verification**

First of all, the standard definition of through element is needed to extract of delay time that is given by phase delay. We used GS types of RF probe by Cascade to measure the through element. The phase delay is -4.625 degree at 1 GHz that is equal to 12.8 pico second.



After extraction, using the transmission line by CPWG type from top layer through to bottom layer for length of 50 mm and 100 mm to verify the phase delay extraction result.



#### Conclusion

The through element for vertical probe measurement system can be operated up to 20 GHz bandwidth and the probe tip pitch coverages ranges are 150 to 1600  $\mu$ m for GS type, 300 to 1250  $\mu$ m for GSG type. It can be used for chip size (fine-pitch) to load board size (wide pitch) and the application like TSV extraction, via extraction, and signal path extraction by top layer through to bottom layer, etc.

We also develop through element for the differential type of GSSG type used on vertical probing system.

BiTS 2018 An Innovation Vertical Probing System for High Speed/Frequency Applications

3