NINETEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

March 4 - 7, 2018

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive

© 2018 BiTS Workshop – Image: pilgrims49 / iStock

COPYRIGHT NOTICE

The presentation(s)/poster(s) in this publication comprise the Proceedings of the 2018 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2018 BiTS Workshop. This version of the presentation or poster may differ from the version that was distributed in hardcopy & softcopy form at the 2018 BiTS Workshop. The inclusion of the presentations/posters in this publication does not constitute an endorsement by BiTS Workshop or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by BiTS Workshop. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop. All rights reserved.

www.bitsworkshop.org

Printed Circuit Board Via Technology Limitations and Optimization

Estanislao Aguayo, Vothy Heang, Christopher Kinney,
Matthew Priolo, Adrian Rodriguez
Intel, Manufacturing Validation Solutions

- Balancing **fine pitch** device constraints and printed circuit board (PCB) **fabrication limitations** presents the test board designer a challenge implementing **optimal layer transitions or vias**.
- Layer transition structures, or vias, are a significant source of PCB signal integrity degradation. This paper focuses on two aspects of the PCB manufacturing and via impact in signal integrity, which are **manufacturing geometrical parameters and shielding.**
- The data presented in this poster has been acquired using state of the art simulation software (HFSS) and the goal of such a study is to gain insight into the shielding aspect in via design, also referred to as return path via or "adjacent" via. The paper's conclusion highlights each via technology limitations due to geometries and fabrication capabilities.

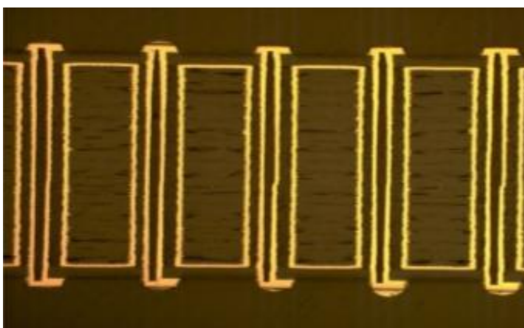


Fig 1: Coax via cross section I/II

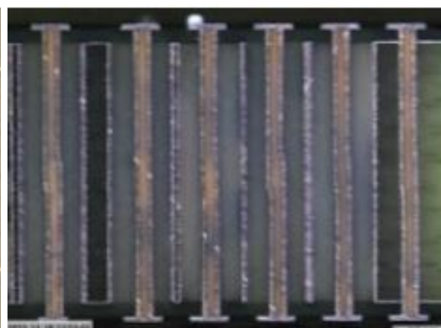


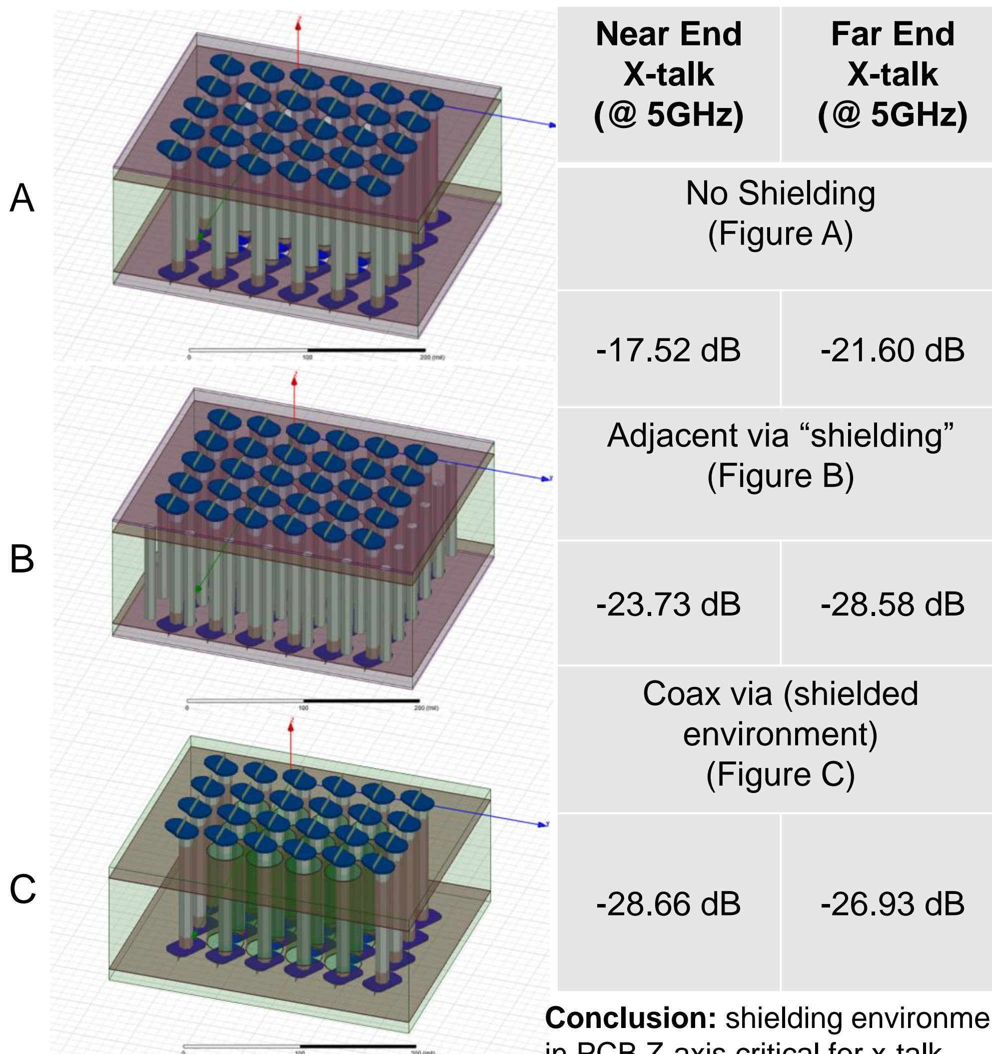
Fig 2: Coax via cross section II/II

Coax via, a via structure capable of improving cross talk up to 10dB @5Ghz

Via performance as a function of shielding environment

Optimization goal: To create a 50 Ohm layer transition, low x-talk,

- Using a 160 mils height riser
- Using 5 GHz as a comparison point for cross-talk
- Ball map is 1 mm pitch
- All assumptions are common where applicable
- Solutions are NOT optimized for best impedance, just minimum and maximum webbing where applicable



Near End X-talk (@ 5GHz)	Far End X-talk (@ 5GHz)
No Shielding (Figure A)	
-17.52 dB	-21.60 dB
Adjacent via “shielding” (Figure B)	
-23.73 dB	-28.58 dB
Coax via (shielded environment) (Figure C)	
-28.66 dB	-26.93 dB

Conclusion: shielding environment in PCB Z-axis critical for x-talk performance

Via manufacturing limitations as a function of via technology

Stacked lasers (µVia)

- Main risk: delamination increases with number of layers (Each layer requires a lamination cycle). Pads on every layer. Stacking vias adds reliability risk.
- Plating increases variation of the trace impedance within a layer which makes it more challenging for de- embedding
- Need to build thickness in the core may require mixing different via technologies

Through hole

- Main risk: Stubs can degrade signal and impede de-embedding of the channel.

Blind / Buried

- Sequential lamination design adds risk to delamination

Back Drilling

- Secondary operation on finished board
- Bandwidth improves due to removed stub.
- Capability to back drill with a drill size less than the antipad used for the via.

Coax via technology

- Main risk: low fabrication yields, due to bubbles in the filling material of the outer via.
- Aspect ratio: up to 15 (achieved 28.2:1)

Stacked µVia over buried

- Adjacent via shielding limited by the mechanical buried via
- Main risk: Delamination of laser via and core via, due to the use of materials and geometries that result in different thermal coefficients for each layer.

Conclusion: Via technology selection will have a major impact on yield of PCB

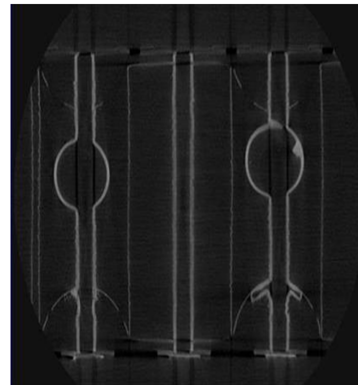
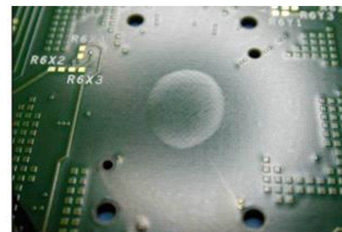


Fig 3: Failure mode in coax via

A



B

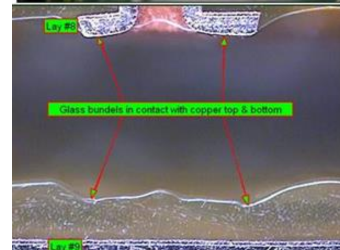


Fig 4: Failure mode in buried vias. A) Delamination on PCB B) Via delamination detail

Fig 5: Stacked µVia over buried failure