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## **“Symptoms of failures and solutions to complicated PCB stack ups”**

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### **Introduction**

- High Density Interconnect (HDI) or Type4 designs are becoming the design choice for most of the next generation premium client systems.
- Comes with added cost but help ODMs/OEMs to meet design complexities and achieve thinner, lighter systems.
- Available in different flavors like 1x1+, 2x2+, 3x3+ or via anywhere designs.
- This paper describes challenges faced in debugging a failing HDI (3x3+) board design and captures learnings which should be useful for similar future designs.

### **Problem Statement**

- During Mother Board Power-on, initial few boards booted successfully to OS, but soon most of the boards started showing MRC(Memory Reference Code) failure [post code – “DD80”].
- Post layout SI analysis on memory interface didn’t reveal any electrical issues on the channel.
- As validation progressed, more failures were reported and different boards showed different failing signatures. However, all boards got stuck at same MRC failure [post code – “DD80”].

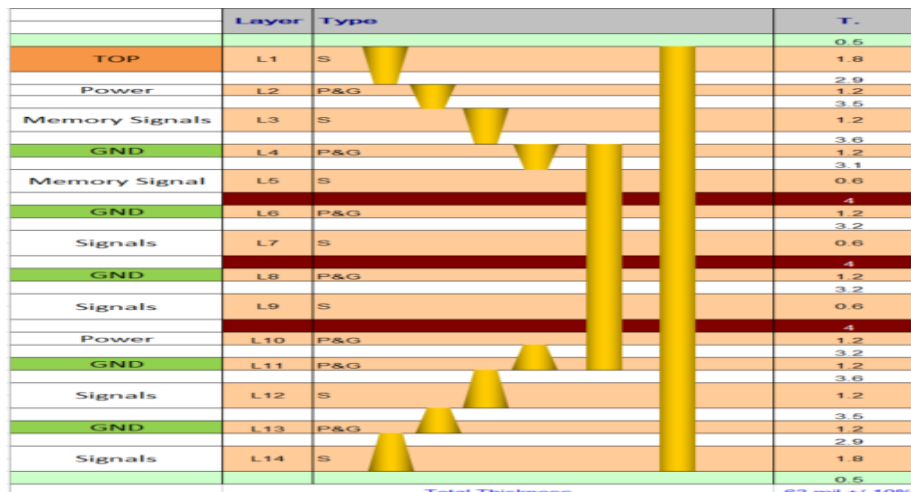
### **Multiple approaches tried to debug issue, in vain**

- Experimenting socketed v/s solder down memory (different memory parts/memory vendors.
- Lowering memory speed bin from 2133MT/s to 1600MT/s
- SOC swapping as the board was socketed.
- Checking PD/PI and tweaking DRAM voltages ...
- Electrical voltages check and power up sequencing measurements.

## HDI Stack-up details for Mother Board

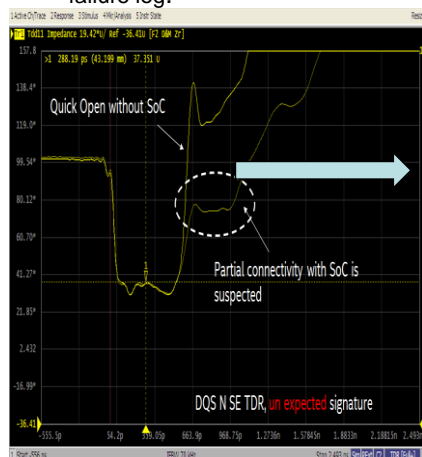
**Below is stack up details for Motherboard supporting Intel's latest Gen processor.**

- 14 layer HDI 3x3+ stack up
- DDR memory routing on L3, L5 as SOC and DRAM placed on top side and to minimize via stubs.



## MRC Failure Leveling Failure

- RC log for one failing system consistently showed failure in write leveling for Channel0 – Byte1.
- Design review of this byte lane on board did not show up any issue.
- Multi meter probing shows proper connections. **but TDR probing on DQS signal however shows high impedance on SOC side implying partial or no connectivity.**
- Below waveform is TDR measurement correlating with the failure log.



**Critical Inference made from TDR Measurement as below:**

- DQS signal for failing byte probed for TDR from DRAM side.
- SOC impedance on higher side (75 ohm v/s 40 ohm expected value for SE measurement). Also, missing C die impact (dip) in the end. → partial or weak DQS connectivity on board.

Series of TDR measurements are made on multiple failing boards and TDR results are correlating with MRC Log.

## Failure Analysis Techniques

Board subjected to various tests mentioned below to physically confirm discontinuity location:

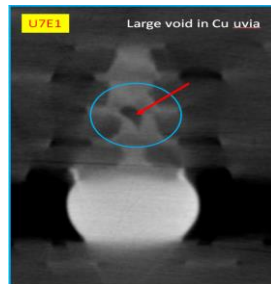
### Non-destructive techniques:

- **2D X-ray:** X-ray inspection uses the fact that X-ray penetration varies according to the type of material and thickness.
- **3D X-ray:** a combination of X-ray and Laser where all angles are covered.
- **Thermal imaging** - Very precise IR Images of current carrying path & identify where the resistance is building to locate the failure spot

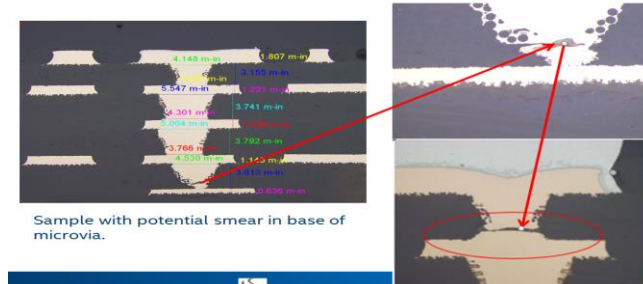
### Destructive techniques:

- **Dye & Pry:** to subject the DUT to Dying/Baking/Prying to identify failure points.
- **Cross-sectioning** of the board which can give exact nature of failure.

## Failure Analysis Results – 3D X-ray, Cross Sectioning



3D X-ray image of via discontinuity



Cross Section image showing hairline crack in u vias.

## Summary and Learnings

- ✓ Inconsistent failure signature can imply connectivity or manufacturing issues as potential cause of failure.
- ✓ TDR/TDT can be a handy tool to characterize boards and identify potential connectivity issues. Multi meter pass may not guarantee signal connectivity.
- ✓ Different fault analysis techniques – destructive and non-destructive can be employed to pin-point exact failure location on board.
- ✓ Careful examination of HDI stack up very important. Via connectivity failures can be eliminated by adherence to proper via **aspect ratio between each layer** in the stack up.
- ✓ Close interaction required with vendor to understand their capabilities and limitations.

## Acronyms

- |   |                               |
|---|-------------------------------|
| ➤ OEM : Original Equipment Manufacturer | ➤ MRC : Memory Reference Code |
| ➤ ODM : Original Design Manufacturer    | ➤ SOC : System on Chip        |
| ➤ HDI : High Density Interconnect       | ➤ DDR : Double Data Rate      |
| ➤ TDR : Time Domain Reflectometer       | ➤ PCB : Printed Circuit Board |