NINETEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

March 4 - 7, 2018

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Mesa, Arizona

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Marketplace Report Challenges of Today & Tomorrow

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BiTS Workshop
March 4 - 7, 2018

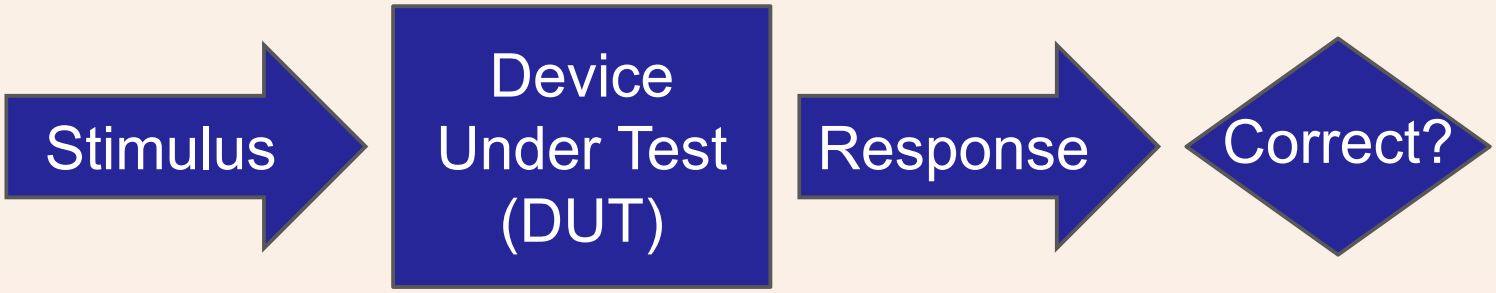
Overview

- Today's Challenges
  - Non-electrical
  - Final vs. Wafer Test
  - System Level Test
- Impending Challenges
  - Internet of Things (IoT)
  - Mobile Devices
- Tomorrow's Challenges
- Socket Market

TODAY'S CHALLENGES

How are electronics tested?

- Stimulus – Response used on Device Under Test (DUT)



Final & Wafer Test Cells

Teradyne Ultra Flex

Advantest V4400

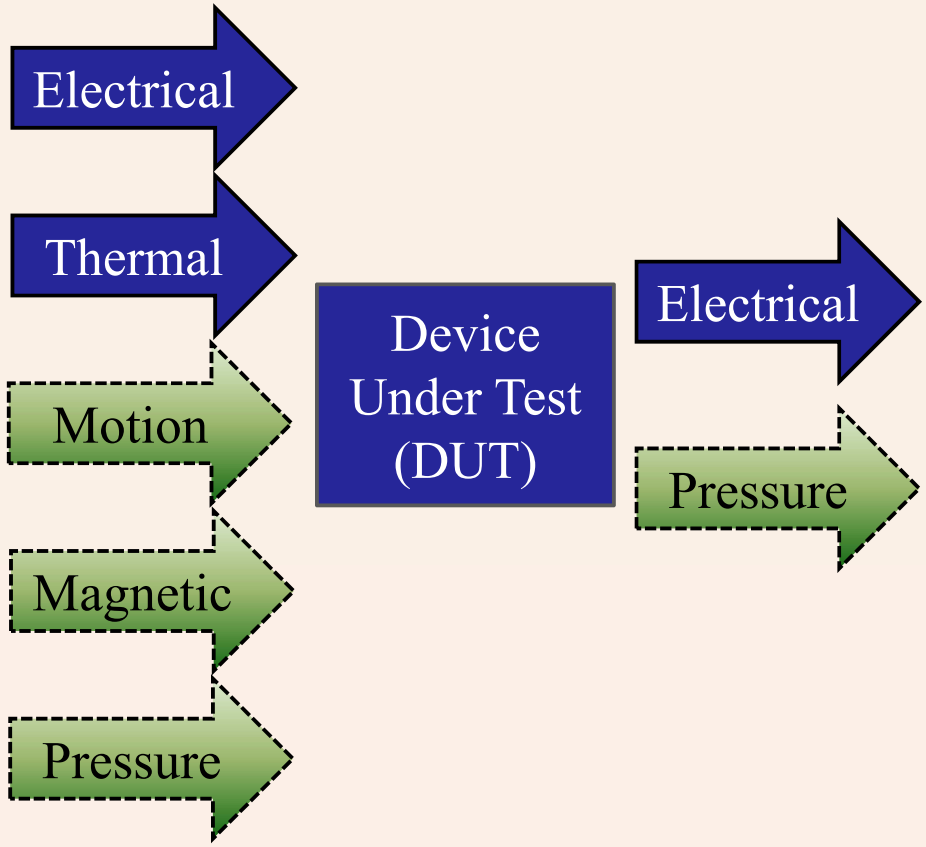
Marketplace Report - Challenges of Today & Tomorrow

Courtesy Teradyne & Advantest

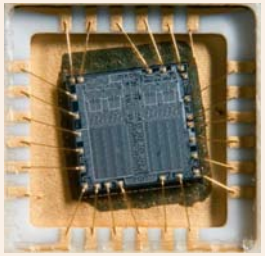
Stimulus & Response – MEMS Sensors

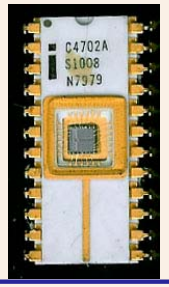
- Accelerometers
- Gyroscopes
- Magnetic Compass
- Microphones
- Speakers
- Pressure sensors

…



Historical - Wafer Sort vs. Final Test





Wafer Sort
- Is this die worth packaging?
- Fab feedback
- Packaging feed-forward

Reduced pin count
Less than at-speed
Single temperature

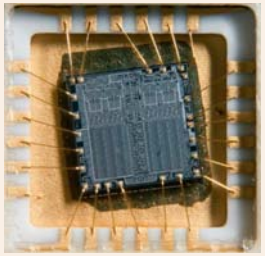
Singulate & Package

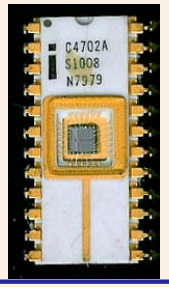
Final Test
- Does this packaged part meet specification?

All pins
Full speed (performance bin)
Multiple temperatures

Electroglas Prober – vortexcontrolsystems.com
UV EPROM circa 1974 - cpushack.com/EPROM.html

Wafer Test & Final Test





Wafer Test Wafer ~~Sort~~

- Is this ... worth ...

...ackaging feed-forward

Known Good Die (KGD) / Not Known Bad Die

Increasing Migration of Tests Earlier in Process

Final Test

...s this ...taged part ... meet specification?

Reduced or full pin count
~~Less than~~ at-speed
~~Single~~ multiple temperatures

All pins (*sometimes*)
Full speed (performance bin)
Multiple temperatures (*sometimes*)

Electroglas Prober – vortexcontrolsystems.com
UV EPROM circa 1974 - cpushack.com/EPROM.html

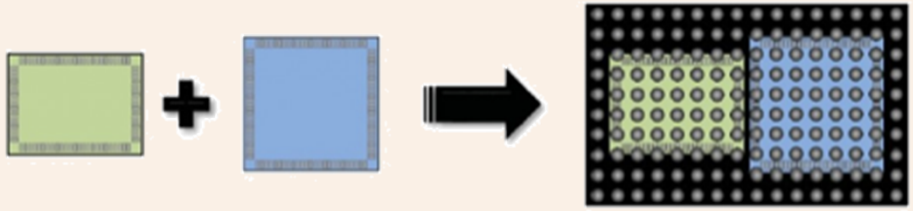
Advanced / Chip Scale Packaging

Wafer Level Chip Scale Packaging

(Chip Scale ≤ 1.2x Die Size)

Fan Out Wafer Level Packaging

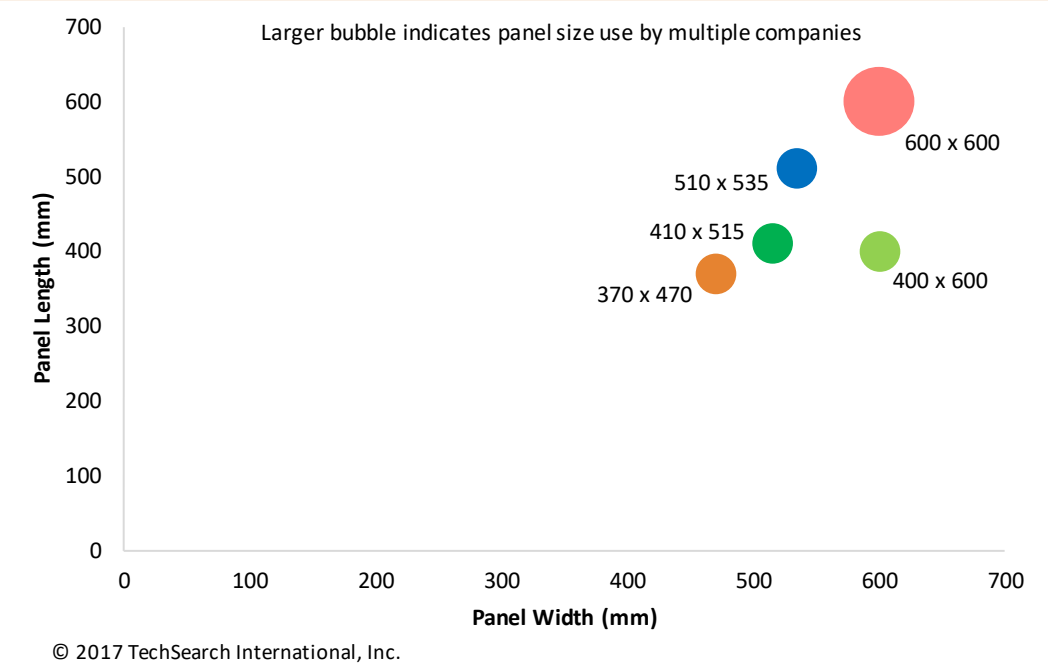
Heterogeneous Integration – System in Package (SiP)



➔ Disruptive to entire supply chain – including test

Panel Level Processing

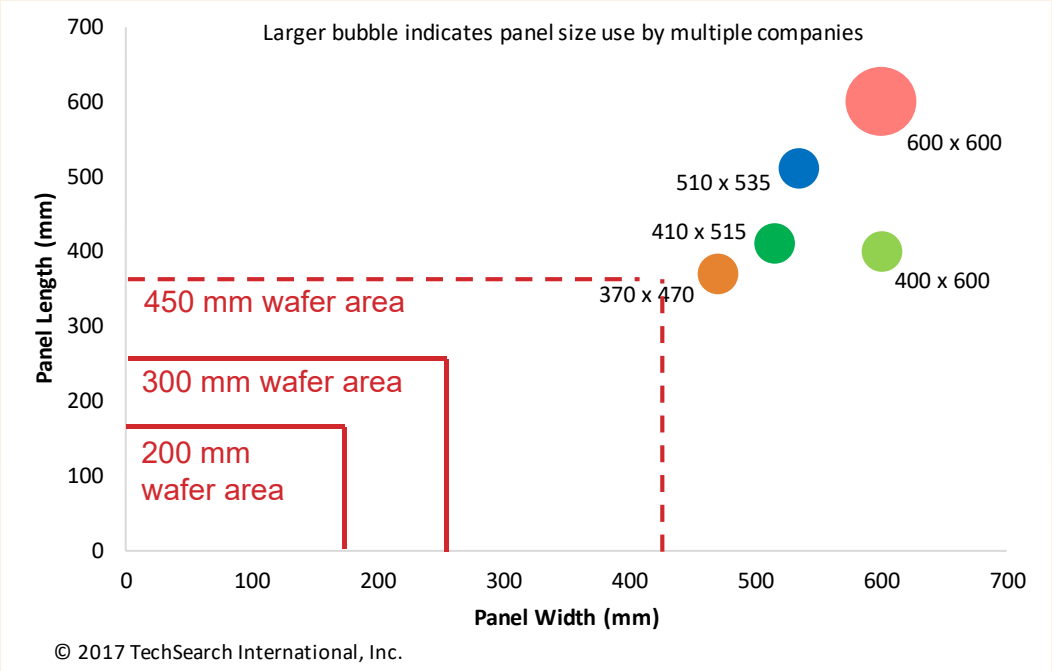
No Consistent Panel Size for Large Area FO-WLP



Courtesy Jan Vardaman / TechSearch International

Panel Level Processing

Each increase in wafer diameter results in 2.25x the area

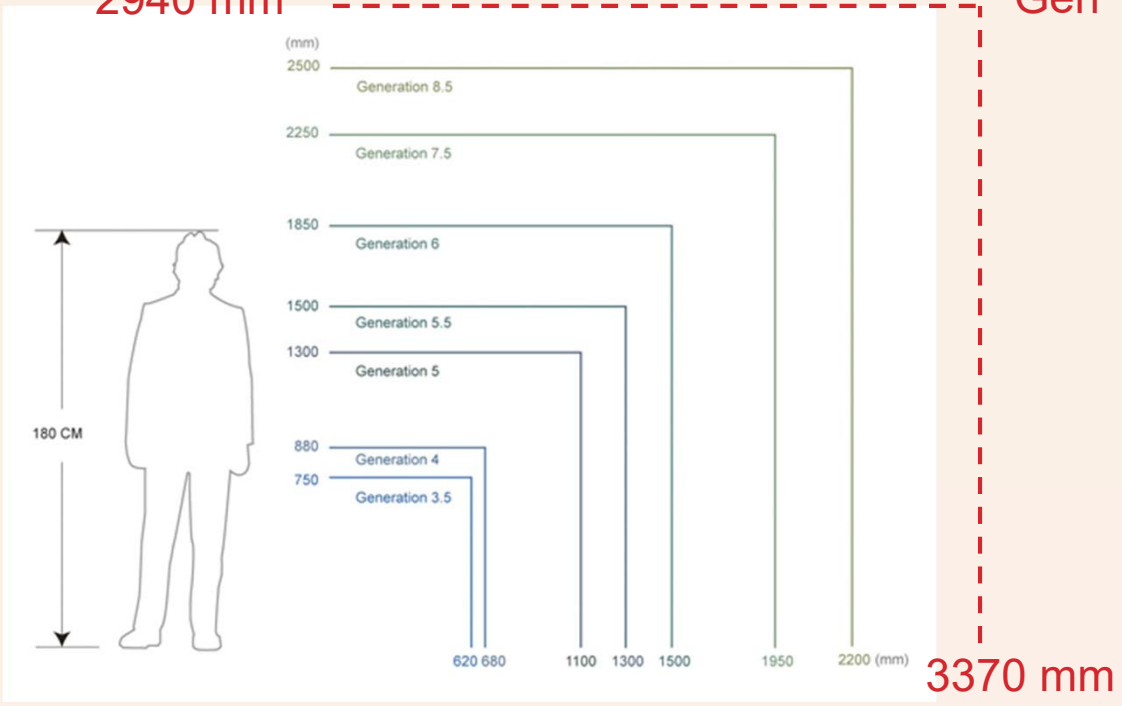


600 mm sq. panel is 5x area of 300 mm wafer

Courtesy Jan Vardaman / TechSearch International

Panel Evolution?

LCD Display
'Mother Glass'



Future Panel Test Handler?

Gallant Precision Machining
TFT Array Probe G4.5~G6

System Level Test – Wide Range of Solutions

Nvidia GPU
(AnandTech)

Chroma ATE

Astronics Test Systems

Why SLT?

- Lower cost of test
  - For some devices vs. automated test equipment (ATE)
  - Typically microprocessors (MPU) / application processors (SoC), graphical processors (GPU), and field programmable gate arrays (FPGA)
- Full ‘stress’ of device
  - Can uses ‘operating system’ or diagnostic code in ‘mission mode’
- Multi-Device interdependency
- Extended test times
  - Burn-in ‘lite’

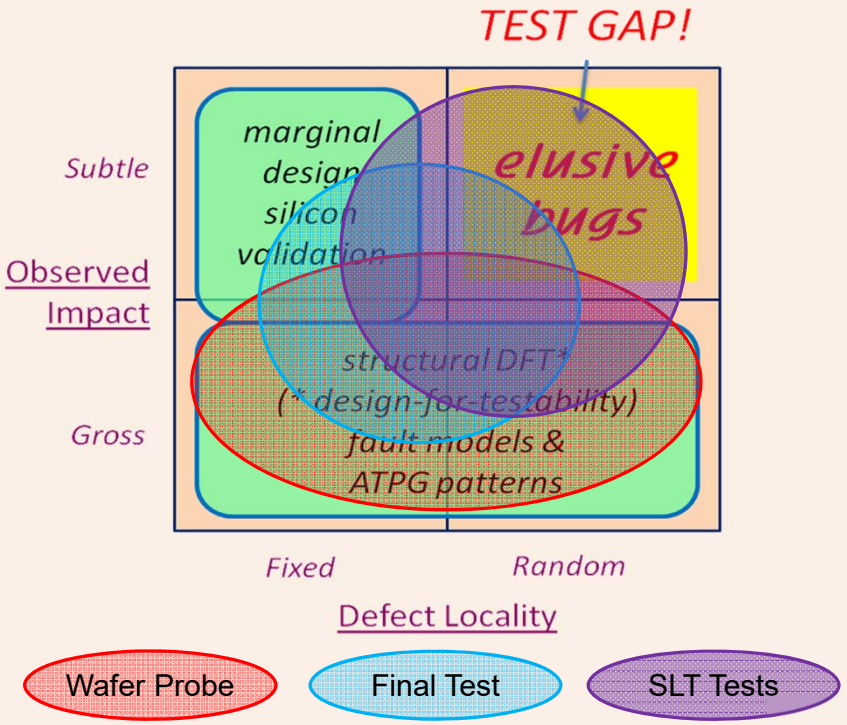
System Level Test (SLT)

Today . . .

- Structural test techniques find most silicon defects
- Rise in random/subtle defects defected by SLT
- Redundant testing for faults

Tomorrow . . .

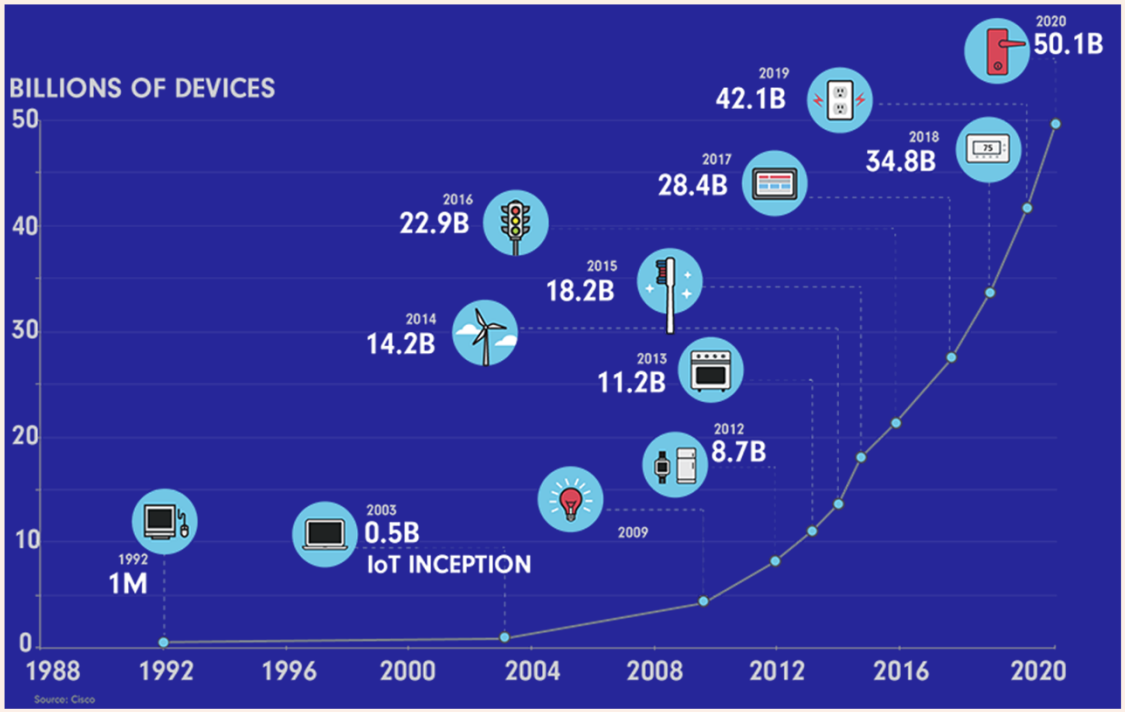
- Expanded fault dictionary to ensure faults are only tested once in manufacturing flow



Courtesy Dave Armstrong / Advantest & HIR Test TWG

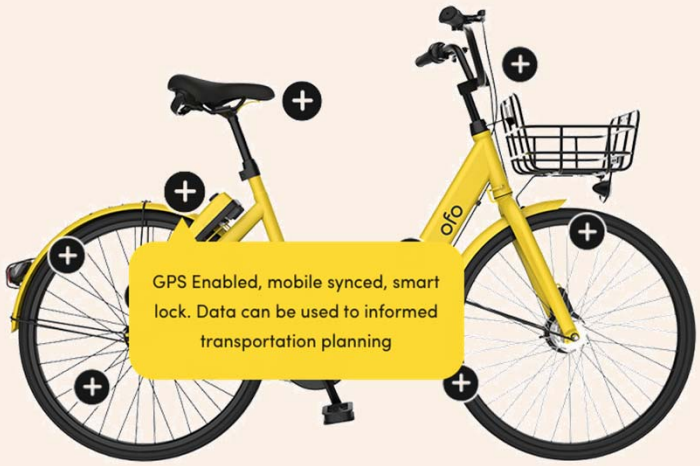
IMPENDING CHALLENGES

Internet of Things



- Billions of devices
- Exabytes/month data
- Typically wireless
- Cost sensitive

IoT – Bicycle Sharing

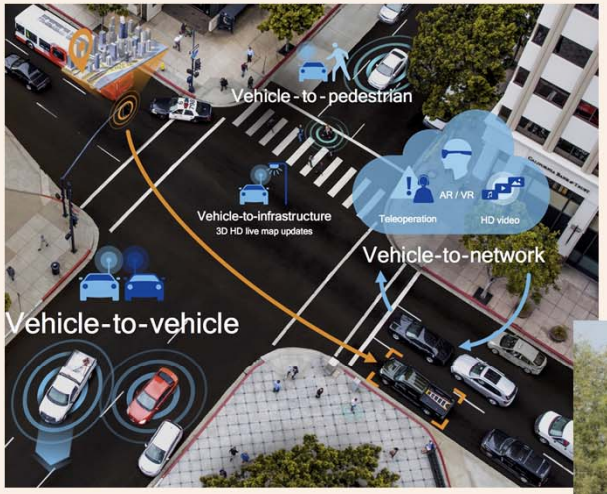


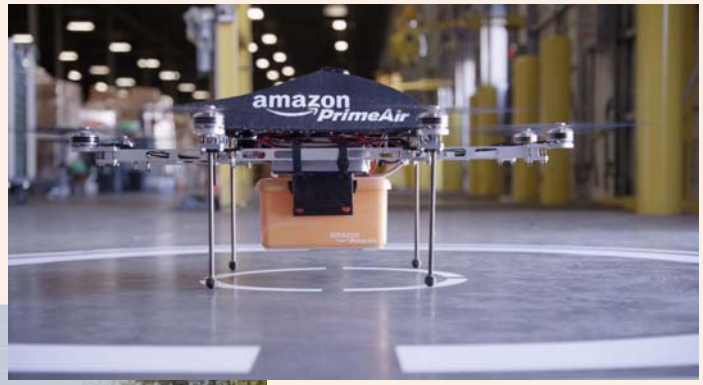
Outside Beijing Wangfujing Hilton Hotel

At the right price, IoT applications become ubiquitous.


bluegogo

Mobile Applications

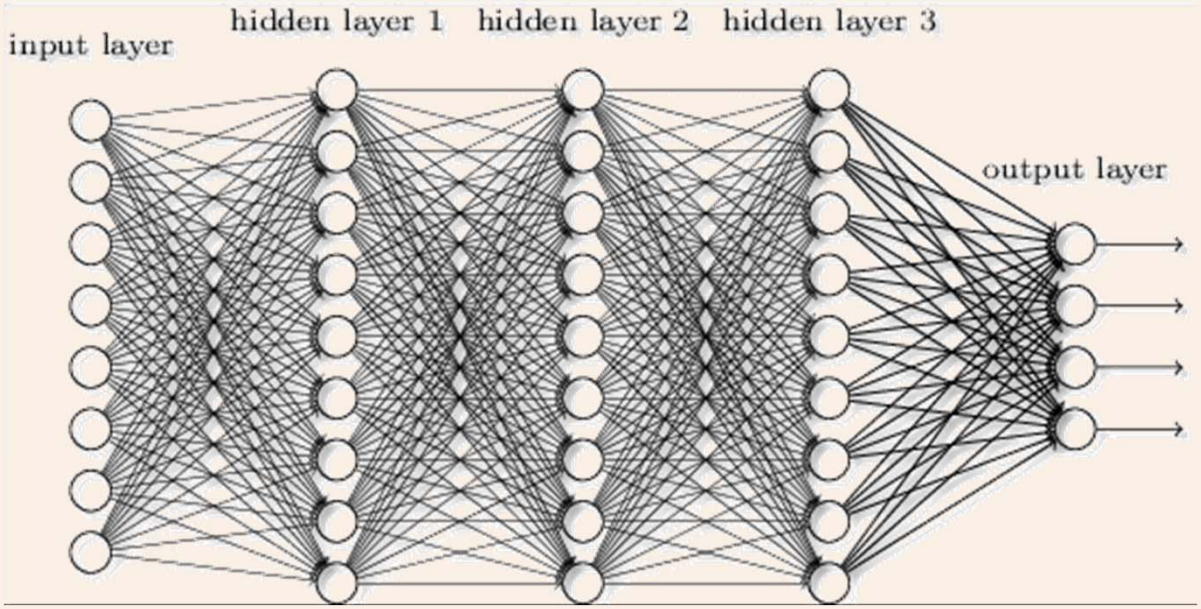




- Safety & Reliability
- Low Latency
- Power Management

TOMORROW'S CHALLENGES

Neural Networks



Right Answer via Distorted / Defective Process

Do we care? What if not consistent?

Input

Misrepresentation

Output

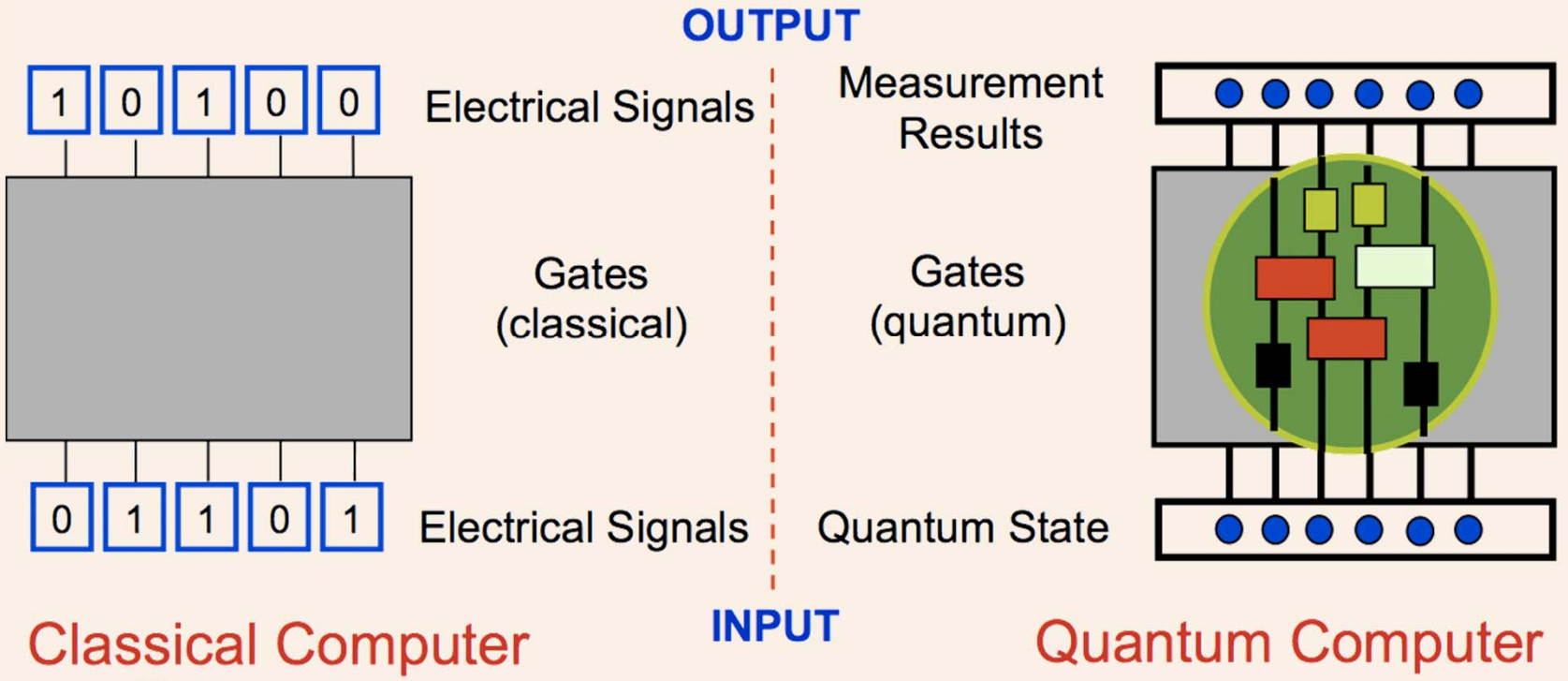
Red

Aqua

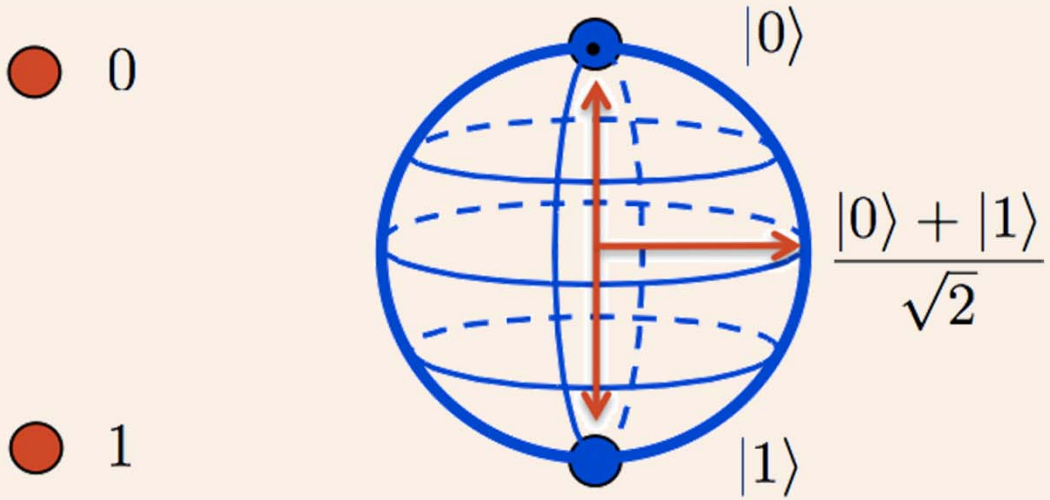
Dark Blue

Protanopia Color Blindness

Quantum Computing



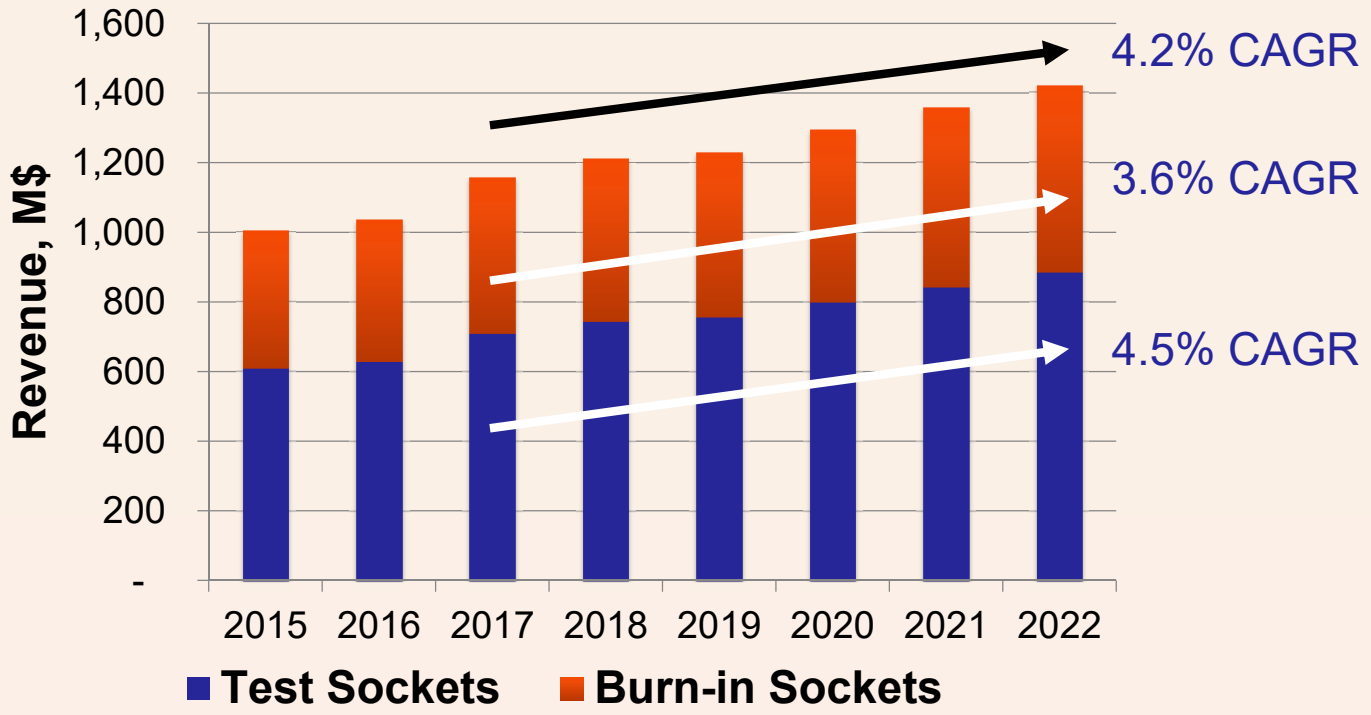
Quantum Computing



Classical Bit **Qubit**

SOCKET MARKET

Test and Burn-In Socket Market



VLSI Research 2017 Preliminary

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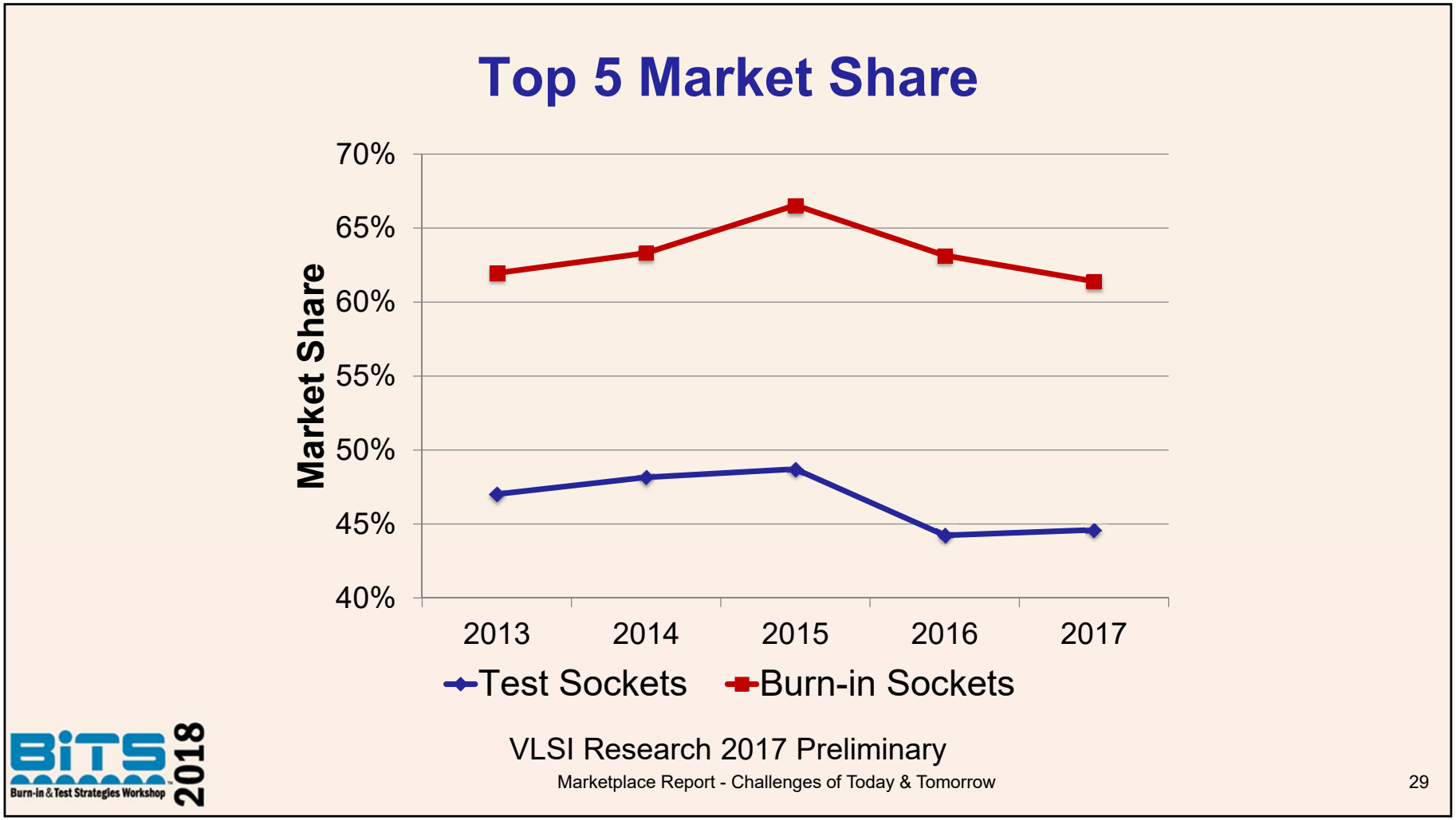
Top 5 Market Share
70%
65%
60%
55%
50%
45%
40%
Market Share
2013
2014
2015
2016
2017
Test Sockets
Burn-in Sockets
VLSI Research 2017 Preliminary
Marketplace Report - Challenges of Today & Tomorrow
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Top Test & Burn-in Vendors

Rank	2015	2016	2017 Preliminary
1	Yamaichi Electronics	Yamaichi Electronics	Yamaichi Electronics
2	Enplas	Enplas	Enplas
3	Smiths Connectors	ISC	ISC
4	ISC	Smiths Connectors	Smiths Interconnect
5	Sensata Technologies	LEENO Industrial	LEENO Industrial

VLSI Research 2017 Preliminary

Acknowledgements

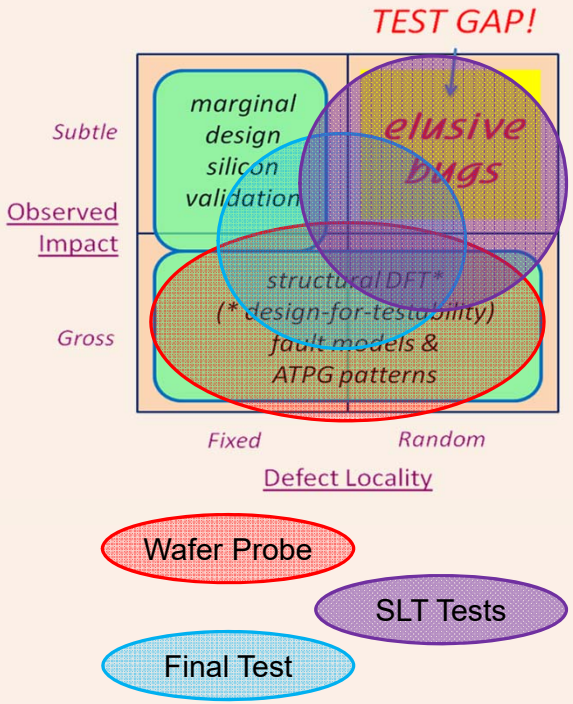
- Lin Fu and John West – VLSI Research
- Dave Armstrong – Advantest / HIR Test TWG Leader
- Jan Vardaman – TechSearch International
- Roger Sinsheimer - Teradyne

BACKUP

System Level Test (SLT)

Today . . .

1. Structural test techniques find most silicon defects.
2. The industry is seeing a rise in random/subtle defects. (those found by SLT)
3. Multiple test steps are resulting in many faults being re-tested multiple times over again.



Tomorrow . . .

1. We will better understand the faults identified in SLT testing.
2. We will expand the test content at wafer probe to cover more of these issues.
3. We will manage an expanded fault dictionary to ensure that faults are only tested once during the manufacturing flow.

Courtesy Dave Armstrong / Advantest & HIR Test TWG

Right Answer – Distorted Process

Protanopia Color Blindness