# NINETEENTH ANNUAL Burn-in & Test Strategies Workshop

#### March 4 - 7, 2018

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Archive

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Session 5 Presentation 2

Semiconductor Device Manufacturer

# Life Cycles of Sockets; Specification vs Reality and Setting Standards

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<b>End of Life Requiremen</b>	ts
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Validation Disciplines	Validation Coverage	Test	Coverage	
Power Thermal and Valid Performance Validation pow sens thro pow	Validates thermal design power (TDP), thermal sensor accuracy, thermal throttling algorithm and power delivery	Burn-in	Accelerates latent defects to meet time zero reliability	
		Class	Continuity tests, power measurements, dynamic frequency/voltage, test of all logic, arrays, I/O testing and SKU	
Analog and electrical	nd electrical Validates electrical performance and IO design		calculations	
Validation		Circuit Marginality	Validates the safety margins of circuits	
Functional validation	Validates logical	Validation (CMV)		
Validation → Find Logical Bugs Validation uses validation boards or reference boards		System Level Validation (SLT)	Uses a product specific tester interface unit based on the reference motherboard SLT insures shipping quality parts and for measuring outgoing Quality	
Socket and thermal system uses quick release retention designs or simple loading mechanisms Socket EOL > 200 cycles		Quality and Reliability	Extended life test	
		Test $\rightarrow$ Transforms design into competitive products.		
		Test→ Remove the defects introduced by Si fabrication process		
		Class and SLT utilizes robotic handlers		
		Socket EOL > 500K cycles		
<b>Bits</b> Socket Electrical, Mechanical, Thermal Performance, Lifecycle and Cost are critical vectors				
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#### **Additional Socket Evaluation Methodology**

- Equipment
  - Tester/Handler with actual devices
  - Socket and test fixture
  - Cres measurement equipment
- Process
  - Maintenance Cleaning intervals
  - Insertion/extraction tracking
- Other
  - Evaluation are done per technology
  - Then done for every families
  - Per device, only tested for opens/shorts, mechanical fit check



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#### **Socket Evaluation Methodology**

#### Electrical

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- Daisy Chained Test Boards are used to evaluate the force/pin and contact resistance per pin and variations between sockets of same or alternate technology
- Insertion loss and return loss
- Mechanical

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- Force/pin, socket tip wear on the DUT side and PCB side, marks on the package
- Checking for contamination on the pins under the microscope
- The socket is then run for 1000 mechanical cycles in the system level testing setup, then through actual system level testing.
  - Passed the short test and passed the long test content except for a specific content for 1000 cycles. Cres tests were repeated using the daisy chained test boards.
  - Similar exercise were done for 2000, 3000 and 5000 cycles. At 5000 cycles, failed short and long test content for SLT.



#### Clear disconnect between socket vendor data of 100K cycles vs > 3K and < 5K cycles

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