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DUT ATE Test Fixture S-Parameters Estimation using 1x-Reflect Methodology

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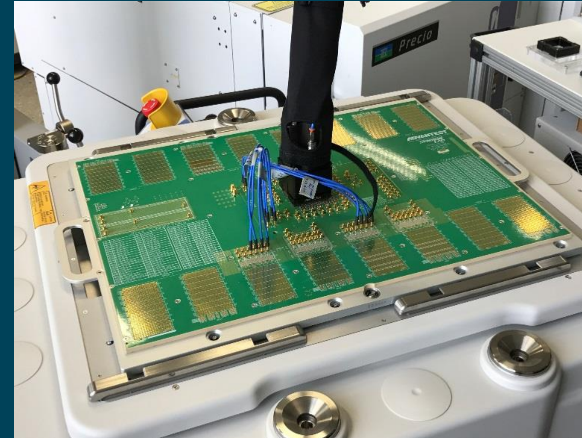
Presentation Outline

- ATE Test Fixture Challenges
- ATE Test Fixture Measurement Challenges
- 1x-Reflect Based S-Parameter Estimation
- Examples of Using the Methodology
- Conclusions

ATE Test Fixture Challenges



- The ATE DUT test fixture is the performance bottleneck for high-speed digital and high-frequency RF applications.
- An unsuspected performance degradation in one DUT pin due to the test fixture can result in lower yield ($$$).
- ATE test fixtures can contain a large number of high-speed I/O pins.
- Modern ATE channels have programmable loss compensation mechanisms (equalization) that require the user to know the test fixture loss for optimal setting.

References [1]

ATE Test Fixture Measurement Challenge

- Two-side probing is the most accurate approach but is challenging because of the DUT socket side where the BGA pitch and ballout have a significant impact.
- It is also very time consuming especially for a high pin count DUT.

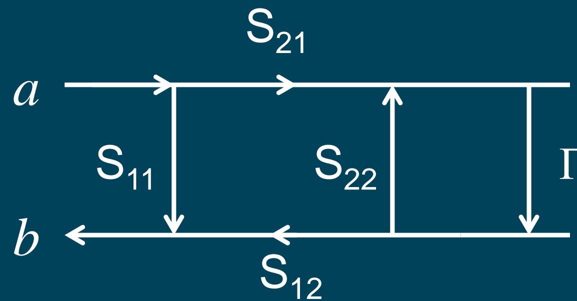
Reference: [1]

ATE Test Fixture Measurement Challenge

- A TDR measurement is enough to debug most of the ATE test fixture possible manufacturing problems.
- But we also sometimes need the test fixture loss for evaluating the test fixture performance and possible de-embedding or equalization setting.
- A 2-port measurement provides an accurate loss measurement but is complex and time consuming. In most cases a good estimate would be enough.
- S-Parameter de-embedding algorithms based on 1x-reflect have been evolving in the last years. One side result of the 1x-reflect de-embedding algorithms is the estimation of the test fixture loss based only on the return loss measurement.

1x-Reflect Based S-Parameter Estimation

- Want to extract fixture's insertion loss (S12 or S21) from 1x open or short measurement (S11 open/short).

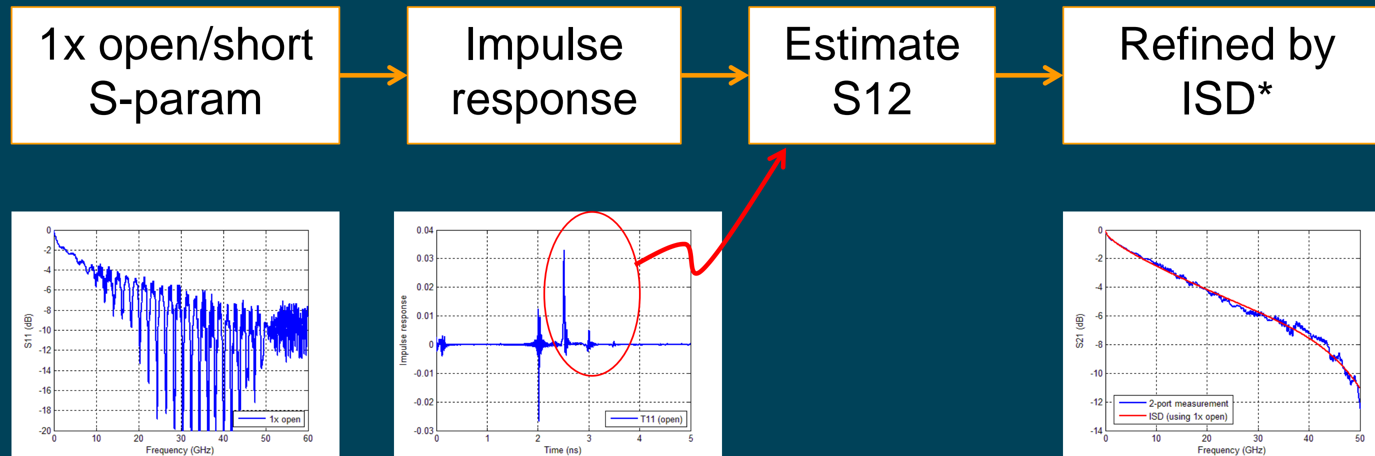


To extract

$$S_{11}^{\text{open or short}} = \frac{b}{a} = S_{11} + \frac{S_{12} S_{21} \Gamma}{1 - S_{22} \Gamma}$$

1x-Reflect Based S-Parameter Estimation

- Fixture’s insertion loss (S12 or S21) can be calculated from impulse response of 1x open or 1x short S Parameters.
- Typically using 1x short or both short and open provides better accuracy.



*In-Situ De-embedding (ISD): www.ataitec.com

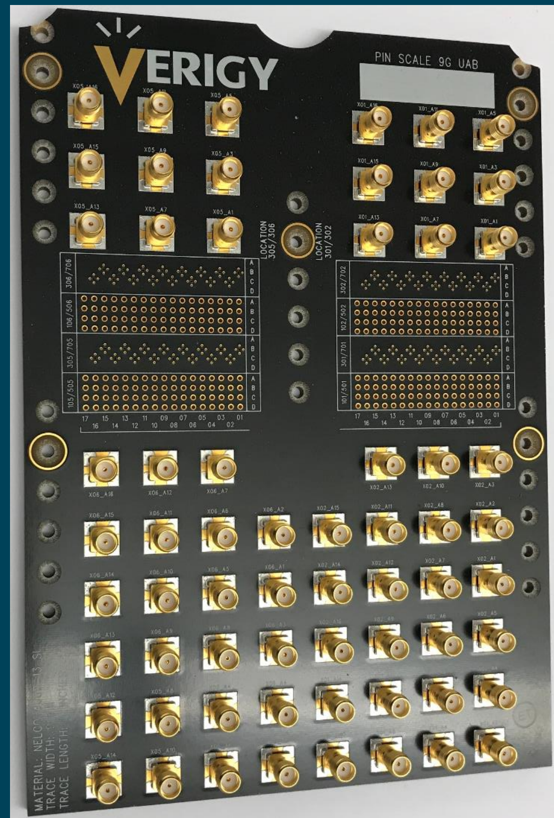
Reference: [2]

Measuring the Test Fixture Return Loss

- Measuring the test fixture return loss is not something that can usually be done by the ATE system unlike for example the fixture delay calibration.
- To perform the measurement a proper probe should be used. Ideally the probe should mimic exactly the ATE to test fixture interface.
- It requires a properly calibrated vector network analyzer (VNA).
- Measurement cables are critical. Invest in good cables and keep movement to a minimum
- Usually the 1x-reflect measurement is done into open (no DUT in the socket). For a measurement into short it is necessary to use a proper shortening device at the DUT socket.

EXAMPLES

Example 1: Pogo Pin Based ATE Test Fixture



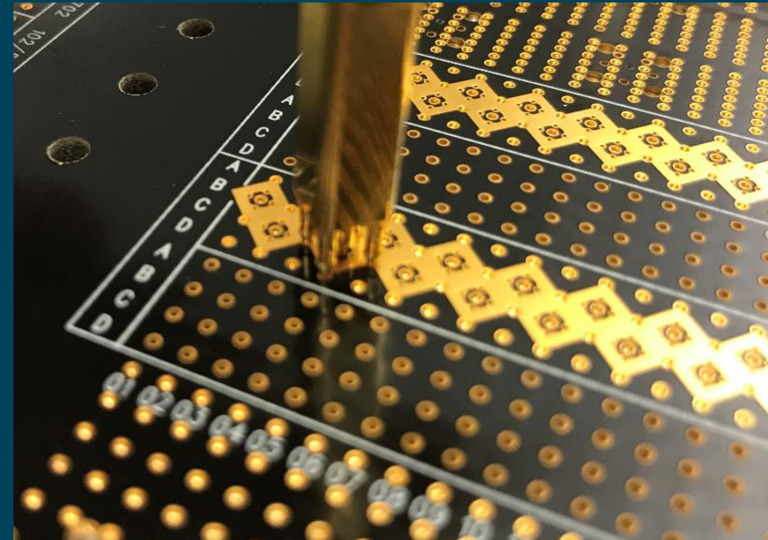
5 inch 9 mil wide stripline
in Nelco 4000-13 SI

ATE POGO PIN VIA

SMA CONNECTOR

- In this ATE test fixture PCB, the DUT side is substituted by an SMA connector.
- This allows an easy comparison between a full 2-port measurement and a 1x-reflect based extrapolation of the insertion loss.

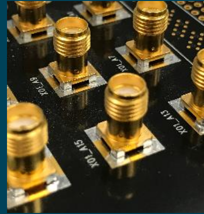
Example 1: 1x-Reflect Measurement Setup

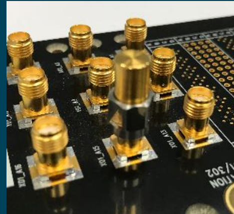


A custom pogo pin to 2.92 mm adapter was developed that mimics exactly the ATE pogo pin interface on one side and provides a high-performance coaxial connection on the other side.

Reference: [3]

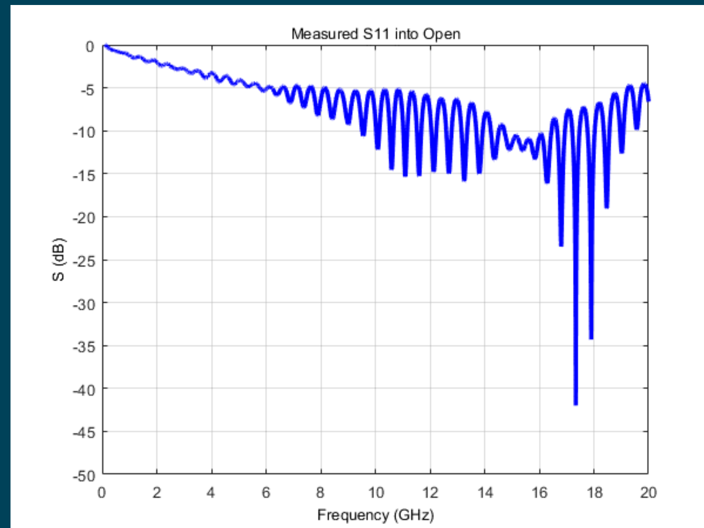
OPEN

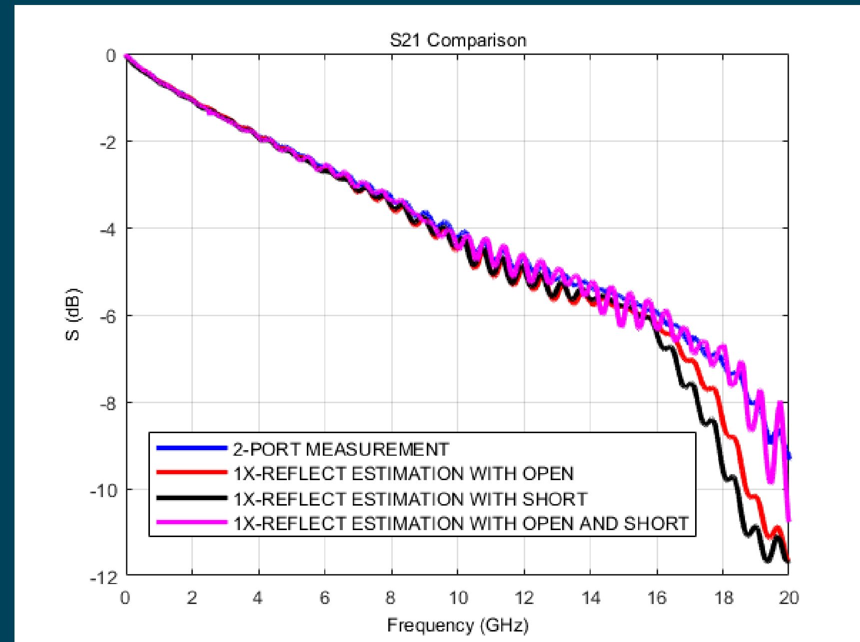




Example 1: Results

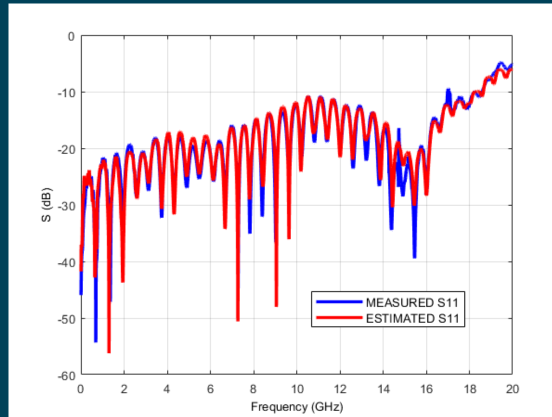
SHORT USING A FLUSH SHORT (ZERO DELAY)

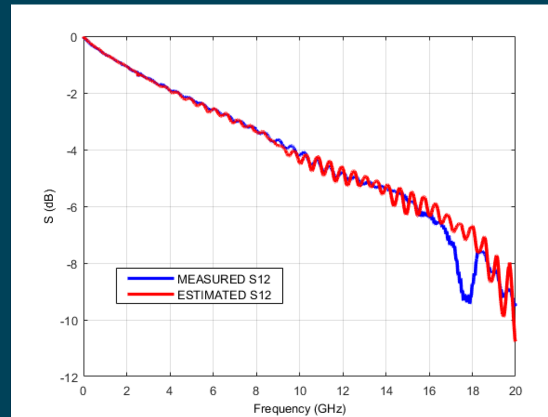


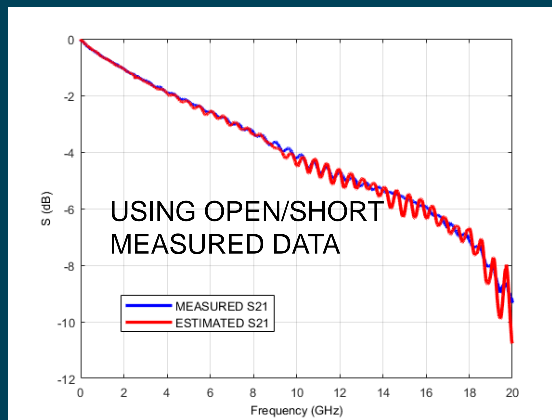


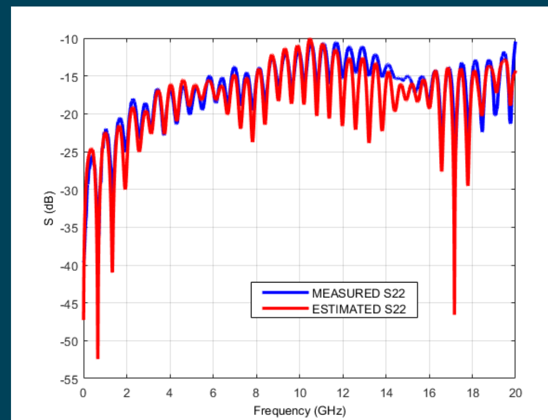
Reasonable correlation with the full 2-port measurement.

Example 1: Results



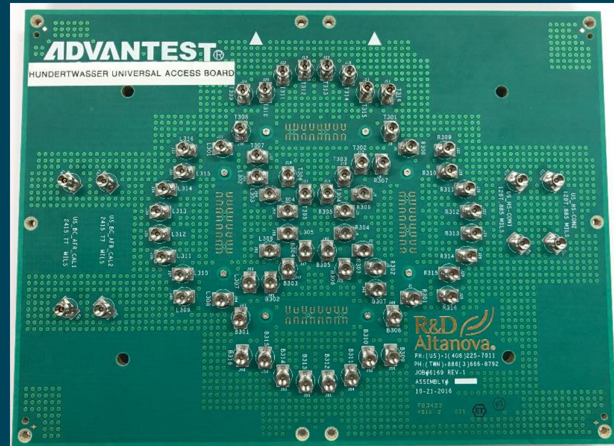


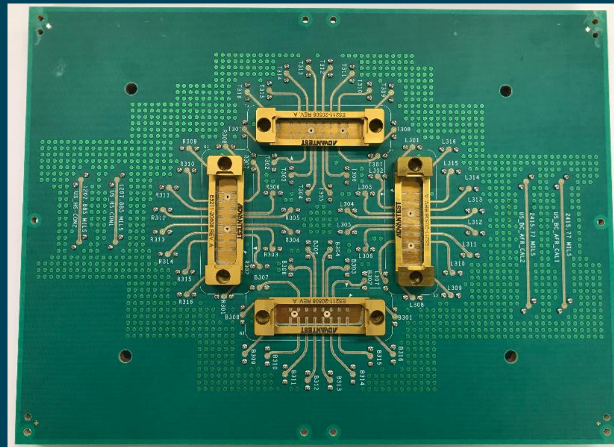




- Methodology provides an estimation of all S-parameters.
- The S22 is the hardest to estimate accurately with this methodology.

Example 2: A 32.8 Gbps ATE Test Fixture

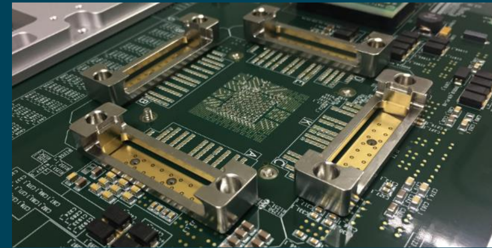


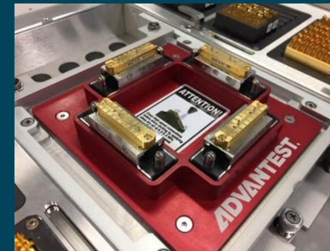


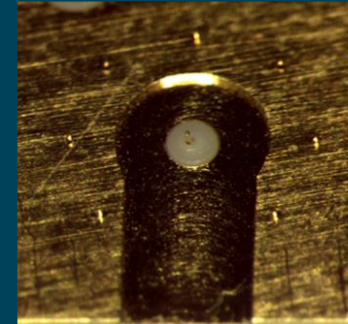
- This is an example for a 32.8 Gbps ATE test fixture.
- The ATE to test fixture interface is much smaller making a hand probe approach very hard. So a bench setup was developed.
- In this ATE test fixture PCB example, the DUT side is substituted by a 2.4 mm connector.
- This allows again an easy comparison between a full 2-port measurement and a 1x-reflect based extrapolation of the insertion loss.

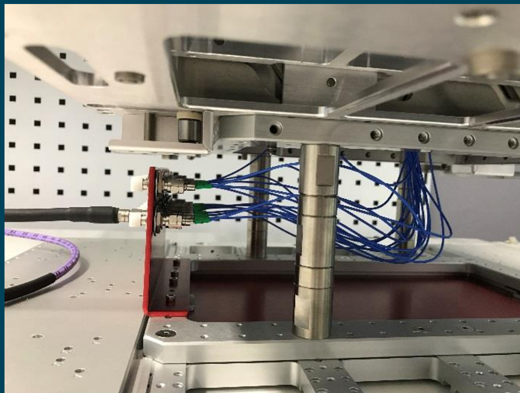
Reference: [4]

Example 2: 1x-Reflect Measurement Setup



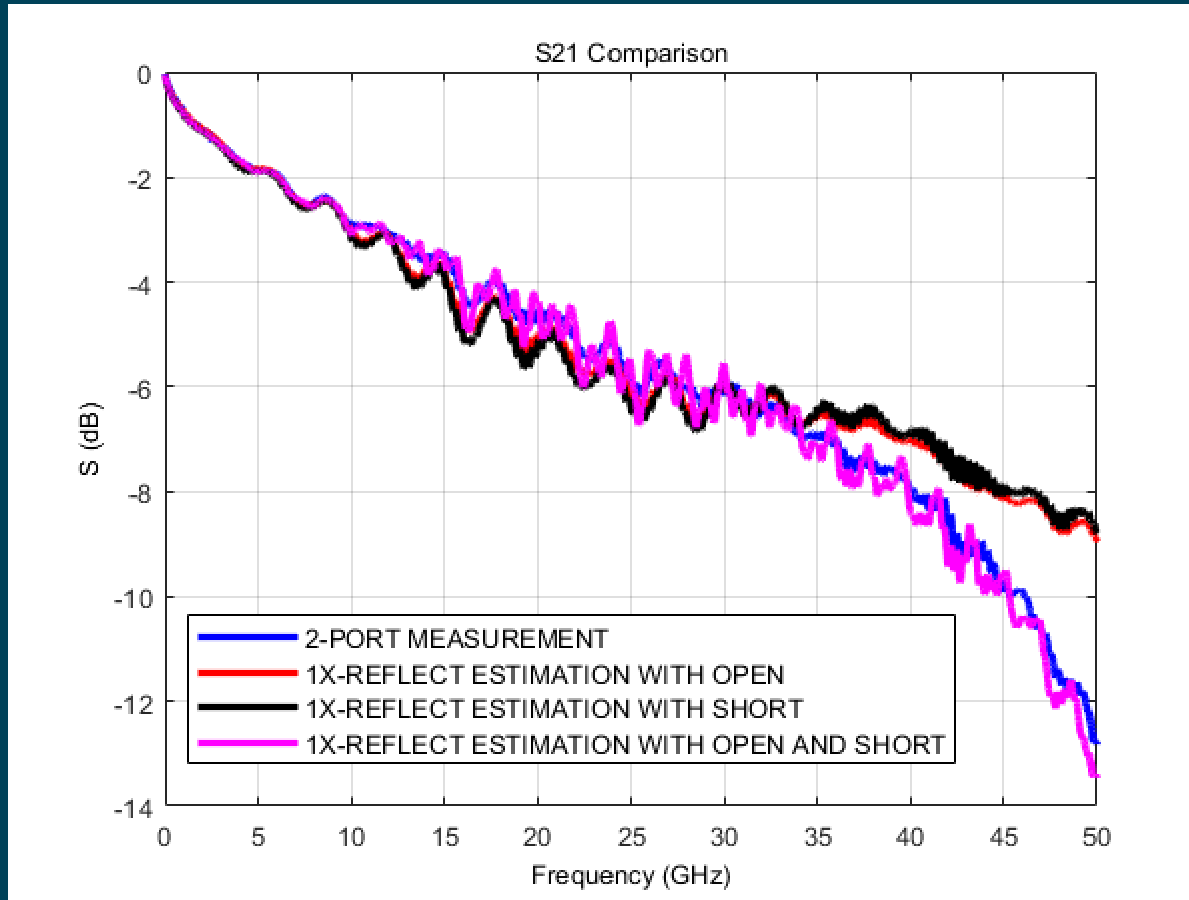






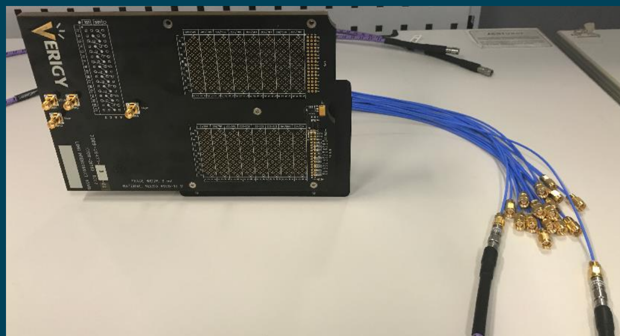
- A hand based probing solution like on the pogo pin example is not possible.
- To address this challenge a bench setup was developed that mimics exactly the ATE interface for this application with a 1.85 mm coaxial connector on the other side.

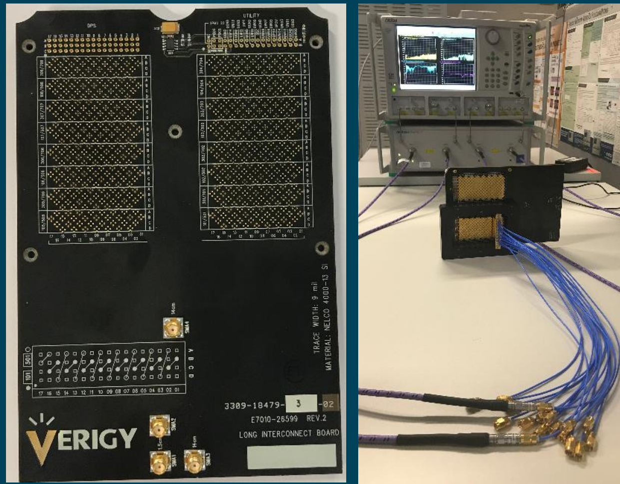
Example 2: Results

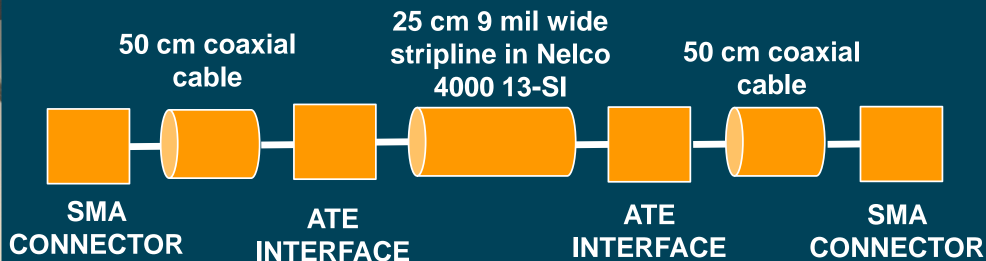


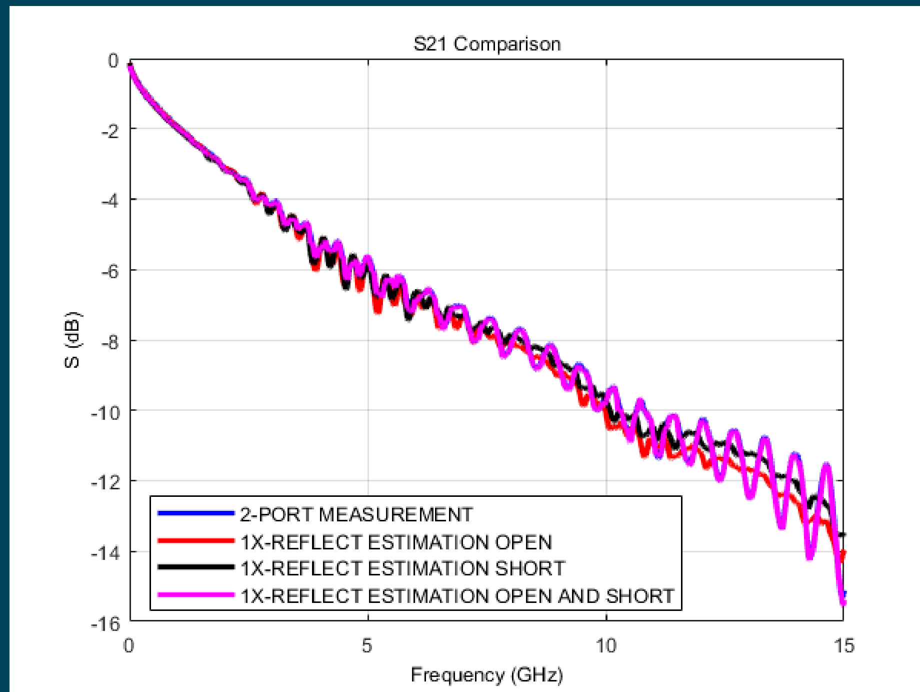
Good correlation with the full 2-port measurement.

Example 3: A Lossy Test Fixture + Coaxial Cable



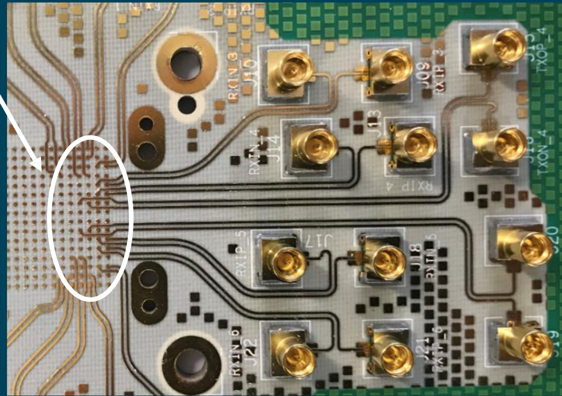




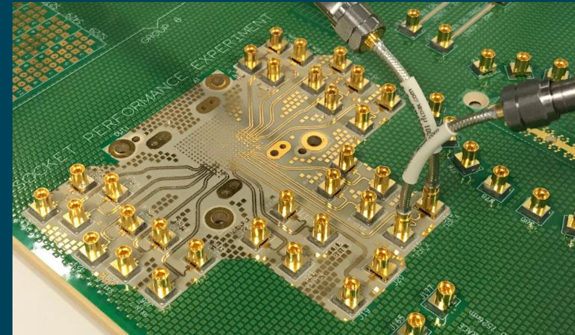


Example 4: Differential Coupled BGA Test Fixture

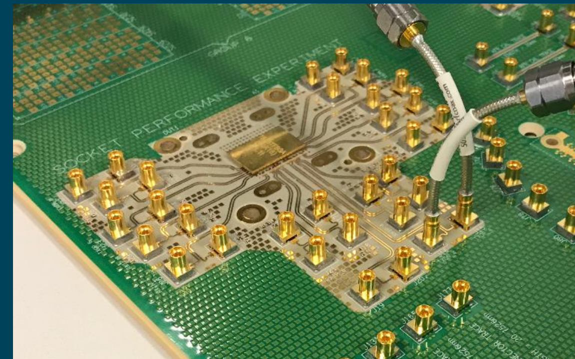
BECAUSE OF MICROSTRIP TRACE CREATING A GOOD SHORT IS NOT EASY

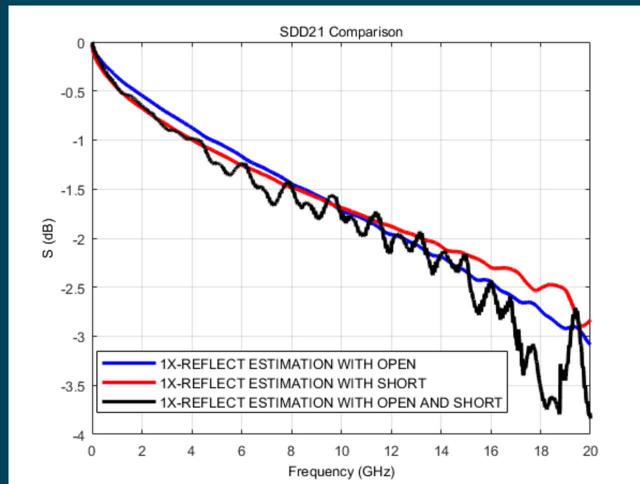


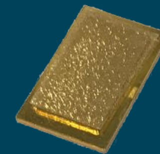
OPEN MEASUREMENT



SHORT MEASUREMENT

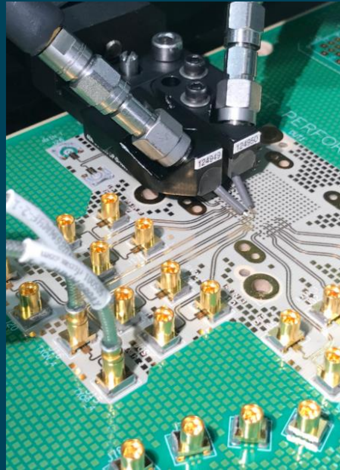


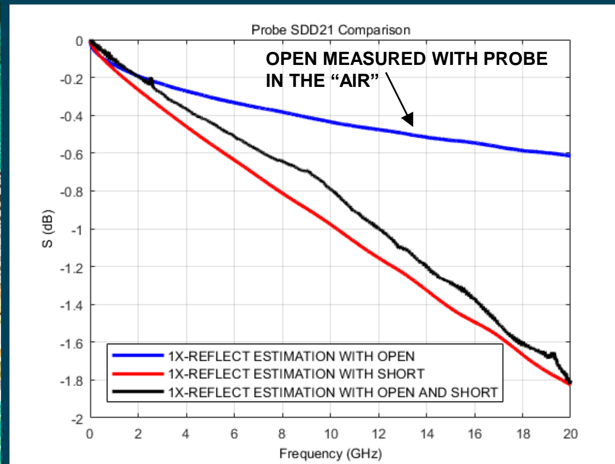


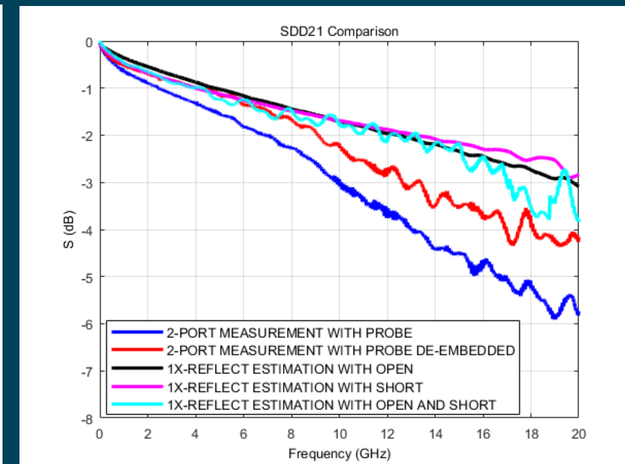


SHORT DEVICE
- CONDUCTIVE METAL BLOCK
- PARICON INTERPOSER

Example 4: Results



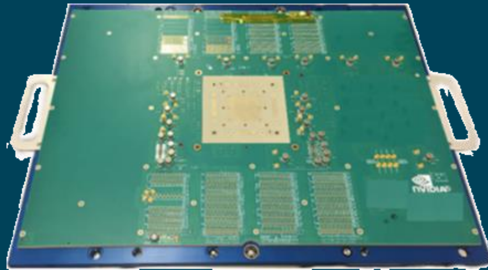




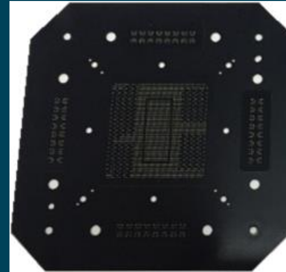
- Coupled differential traces creates a tougher challenge (e.g. mode conversion) for the 1x-reflect S-parameter estimation.
- Creating an open and short on a BGA via field is much harder than on a coaxial connector with a flush short.
- For verification a 2-port measurement with a differential (GSSG) micro-coaxial probe was performed
- Coaxial probe also has a loss that was estimated and de-embedded using 1x-reflect.
- The results show a good correlation at low frequencies that gets worse at higher frequencies because the short and open are also worse at higher frequencies.

Example 5: A High-End GPU Test Fixture

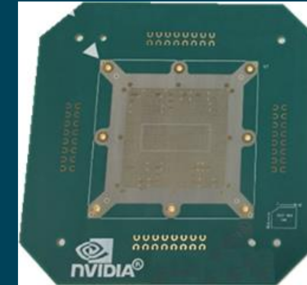
MOTHERBOARD

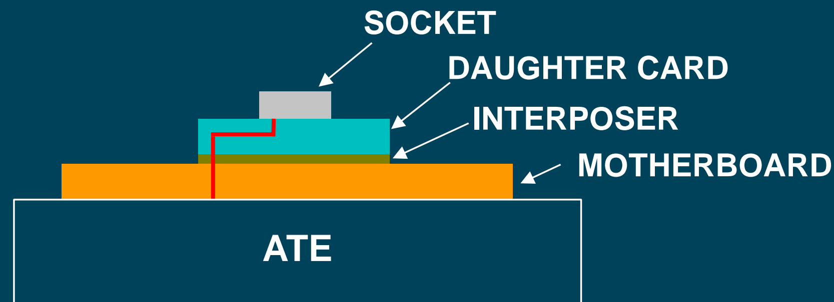


INTERPOSER



DAUGHTER CARD





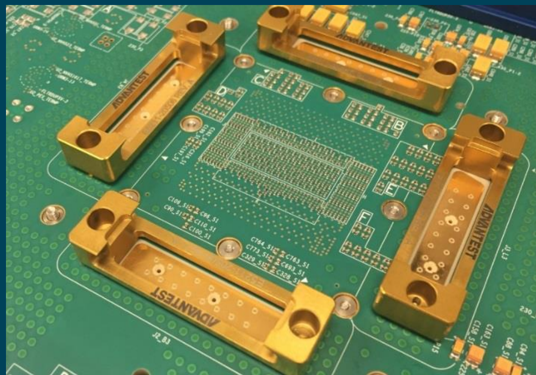
- This is a real ATE test fixture example.
- The test fixture is composed by a motherboard and a daughter card.
- Signal traces are differential but non-coupled
- The objective is to estimate the loss of the daughter card.

Reference: [5]

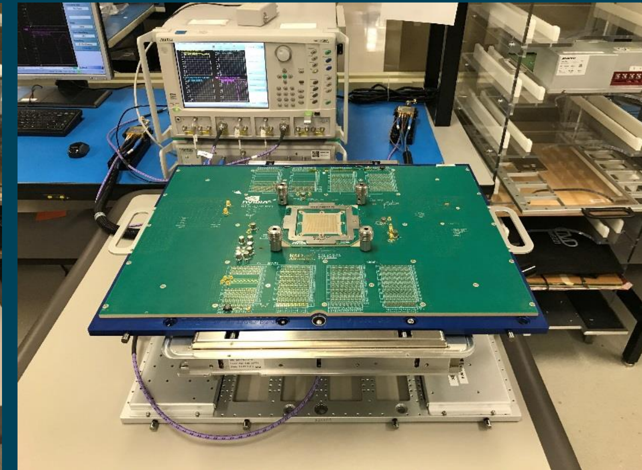
Example 5: A High-End GPU Test Fixture

ATE INTERFACE

MOTHERBOARD INTERFACE (BOTTOM SIDE)

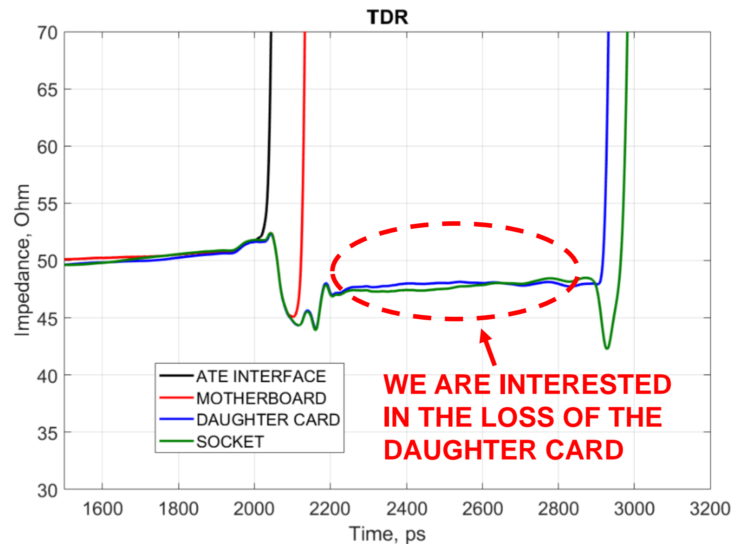


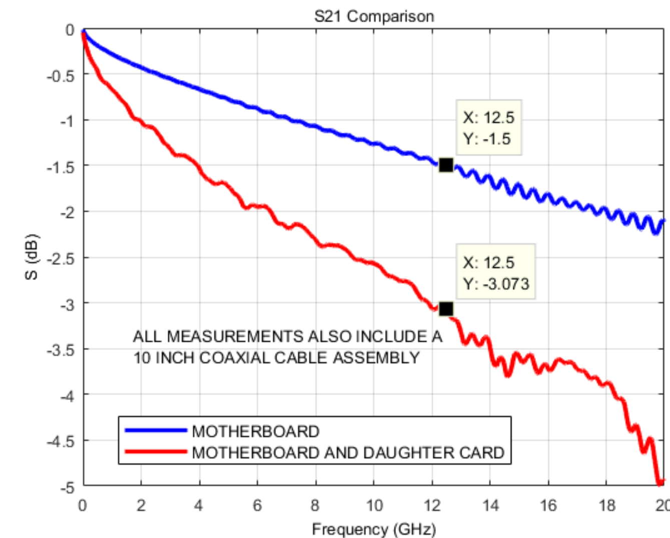
BENCH MEASUREMENT SETUP



- First measurement is of the motherboard alone (this includes also the 10 inch ATE interconnect cable assembly which is not de-embedded).
- Second measurement is of the motherboard plus the daughter card.

Example 5: A High-End GPU Test Fixture





The results provide an estimation of the daughter card loss. For the application critical frequency of 12.5 GHz (25 Gbps) the daughter card adds ~1.6 dB of insertion loss.

Conclusions

- The ATE test fixture is the major performance bottleneck for high-speed digital and high-frequency RF applications.
- Return loss measurement can be used to estimate the ATE test fixture insertion loss by using an appropriate software tool.
- Do not use the 1x-reflect blindly. There are always limitations to every algorithm.
- Open and short quality are critical for the 1x-reflect estimation accuracy.
- This technique requires a VNA measurement. TDR instruments can provide S11 results through SW post-processing but the accuracy is much lower compared to a VNA measurement.
- For a thorough comparison of the S-parameter estimation accuracy it is necessary to also take into account the phase when looking at the estimation error.
- For high accuracy a full 2-port measurement is still the golden standard.
- The IEEE P370 standard is being developed to provide guidelines for de-embedding algorithms accuracy including 1x-reflect based de-embedding.

References

- [1] Jose Moreira and Hubert Werkmann, “An Engineers Guide to Automated Testing of High-Speed Interfaces”, 2nd Edition, Artech House 2016.
- [2] Ching-Chao Huang, “In-Situ De-Embedding,” EDI CON, Beijing China 2016.
- [3] Jose Moreira, Heidi Barnes, Callum McCowan and Rose Winters, “Time Domain Reflectometry Kit for ATE Test Fixtures”, Verigy VOICE Users Conference 2008.
- [4] Jose Moreira, Hubert Werkmann, Daniel Lam and Bernhard Roth, “Implementation Challenges of an ATE Test Cell for At-Speed Production Testing of 32 Gbps Applications”, BITS China Workshop 2016.
- [5] Jinlei Liu, Derek Lee, Jinglan Jia and Takatoshi Yoshino, “ V93000 32G High Speed Extension Solution to Test High-End GPU”, Advantest VOICE Users Conference 2017.

ISD Estimation Setup