
BiTS
CHINA 中国
September 6 - 7, 2017
InterContinental Shanghai Pudong Hotel -
Shanghai, China
Archive
©2017 BiTS Workshop. Image: Easyturn/iStock

COPYRIGHT NOTICE

www.bitsworkshop.org

Coplanar Waveguide Calibration Technology for High Volume Microwave On-Wafer Test

Yuzhe Yin
China Electronics Standardization Institute

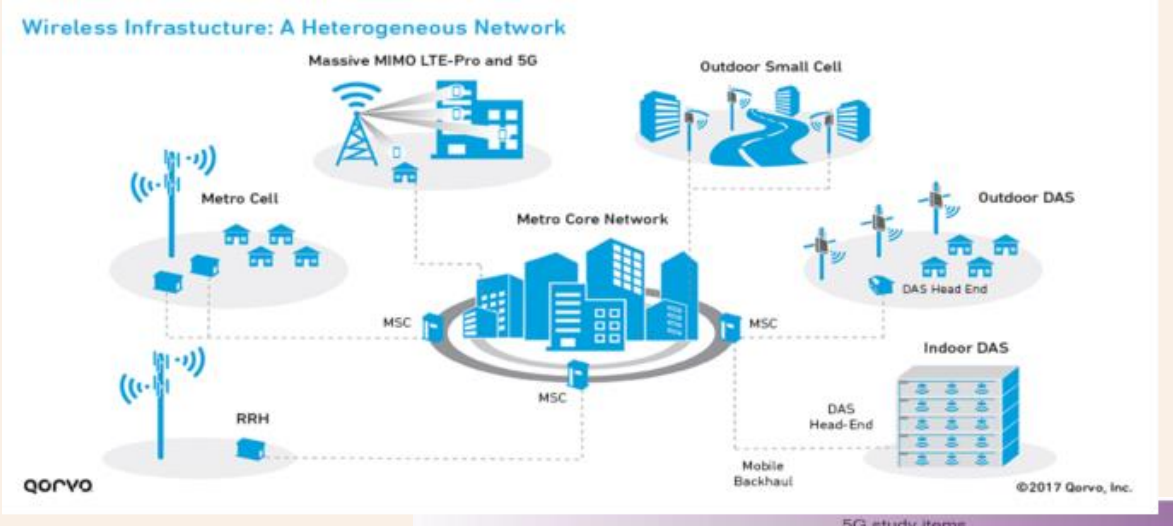
BiTS China Workshop
Shanghai
September 7, 2017

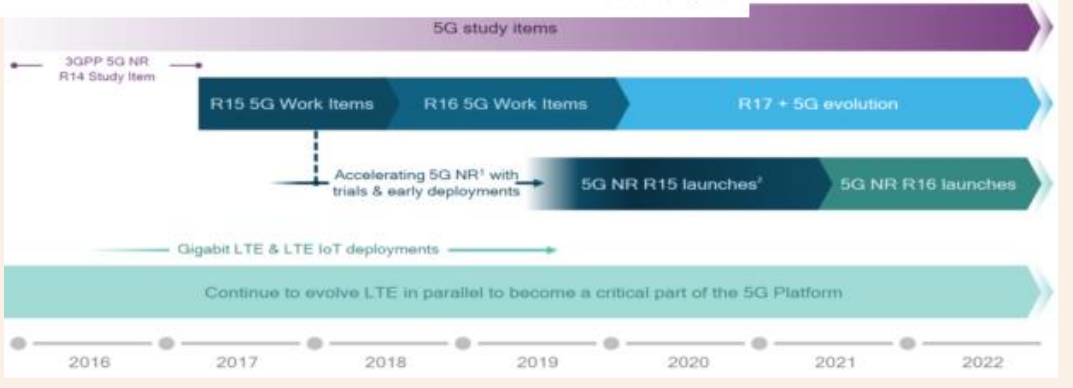
Index

- 5G Background
- Vector Network Analyzer based On-Wafer Test
- ATE based On-Wafer Test
- 93k Architecture
- On-Wafer Calibration Technology
- SOLT/TRL/LRRM
- CESI 8190 Calibration Kits
- CESI Calkit Calibration Software
- Future work

Background: Path to 5G

5G service scenario and roadmap：





Background: Components for 5G

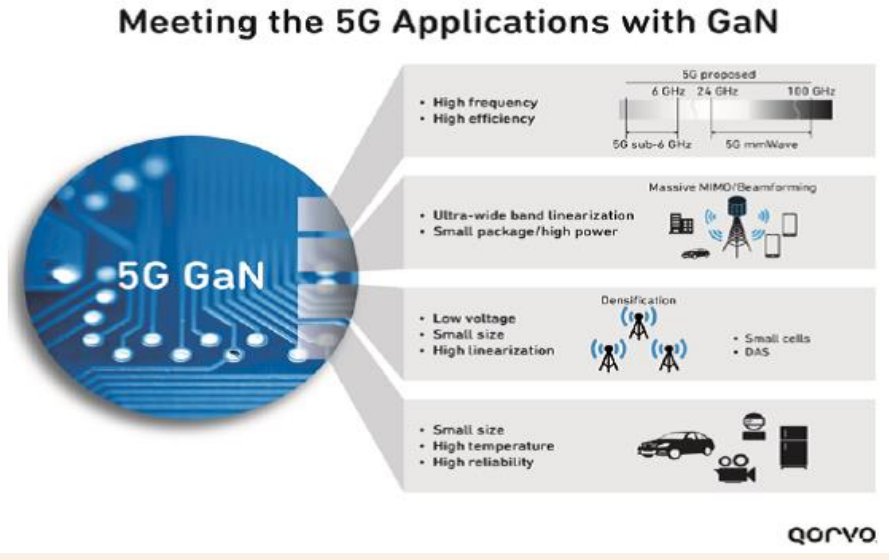
Spectrum: new 6GHz+ mmWave.

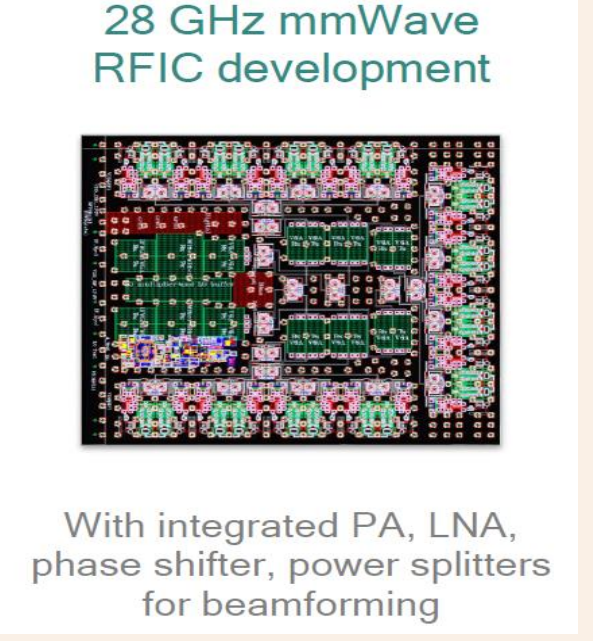
Bandwidth: 20MHz～1GHz.

Bands: 50+.

Candidates:

GaN/SOI/MEMS... compound semi and Si.





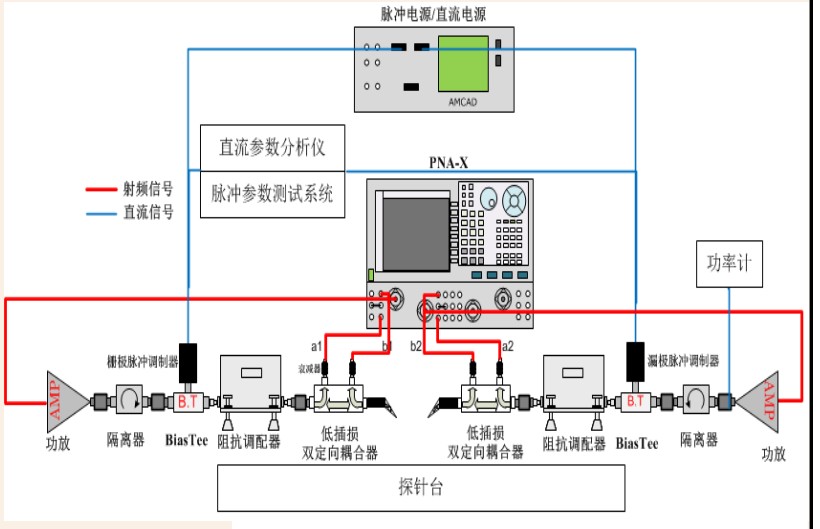
Vector Network Analyzer based On-Wafer Test

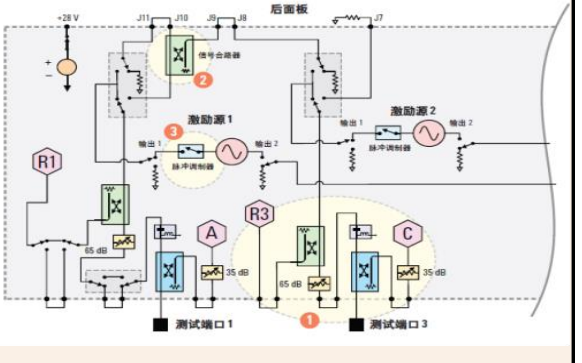
On-Wafer microwave characters:

- Power: input, output, gain, flatness
- Noise: ENR, noise parameter
- Harmonics: IP3
- Transient: Rise/Fall time

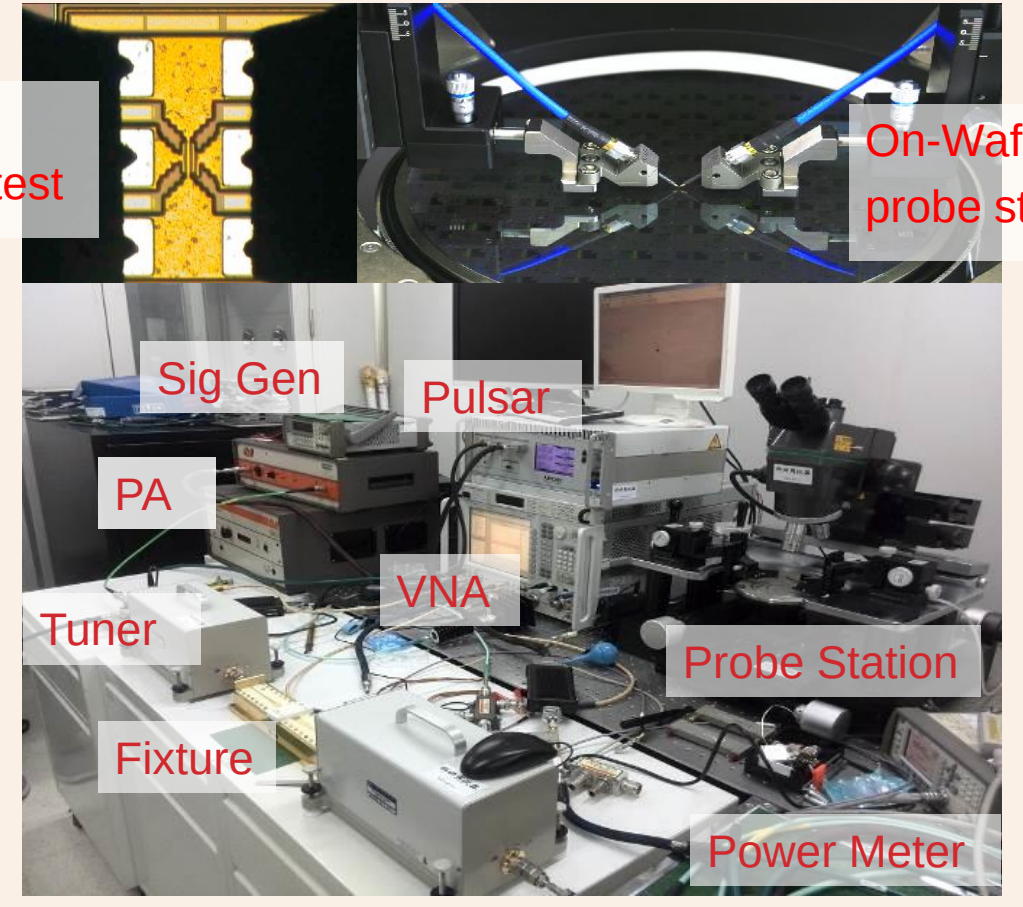
Measuring system:

- VNA: 2 source/4 port/8 receiver
- Tuner: non-50Ohm scanning
- Power Amplifier: driver
- Power meter: VNA receiver power calibration
- Probe station: semi-auto, on-wafer calibration
- Pulse I/V: driver, measure. 50V, 500ns
- Scope: GaAs, GaN, InP, COMS-RF, etc.





Vector Network Analyzer based On-Wafer Test



Vector Network Analyzer based On-Wafer Test

Advantages:

- Precision: high, Power and S-parameter
- Capability: all microwave parameters
- Extension: tuner etc.
- Range: 110GHz above

Disadvantages:

- Integration: multi-vendor puzzle
- Complexity: high, poor automation
- Data channel: difficult, microwave specified
- RF channel: 1-2 in/output
- Volume test: not appropriate, no other choices

Challenge:

- Mixed signal: wideband test for 5G
- Volume test: Efficiency

ATE based On-Wafer Test

Advantages:

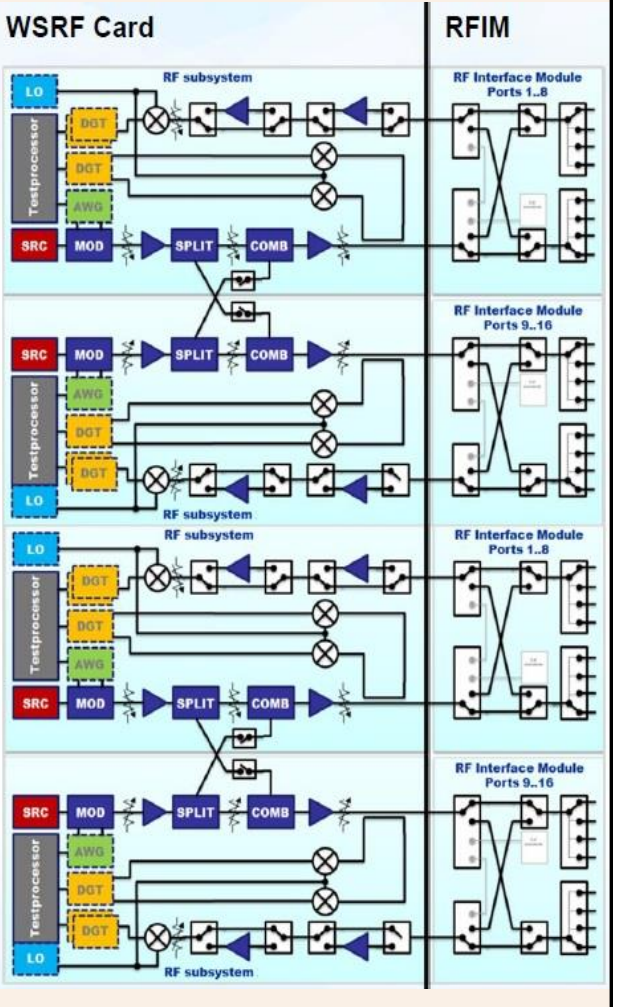
- Integration: Good, 93k's WSRF and WSMX
- Complexity: low, mono-vendor
- Data channel: scalable
- RF channel: 4 RF subsystem/card
- Volume test: best choice

Disadvantages:

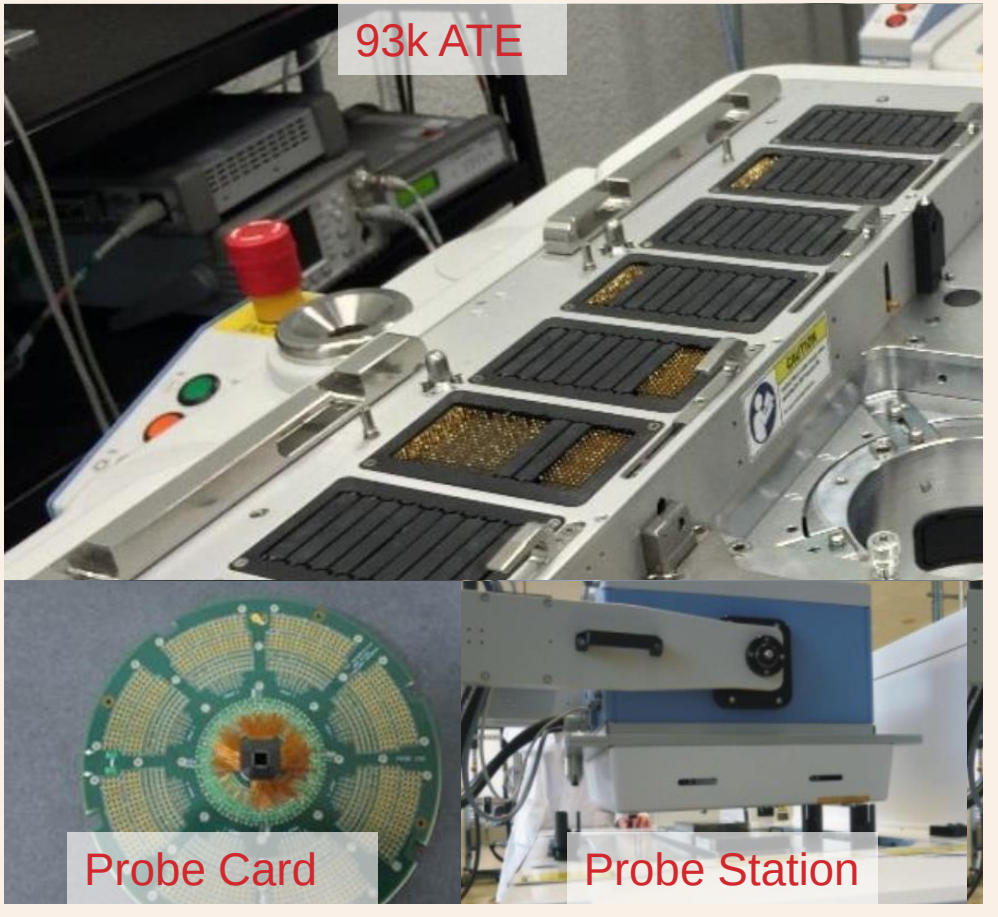
- Precision: lower than VNA
- Capability: not all microwave parameters
- Extension: tuner integration poor. Only 50Ohm
- Range: 6GHz and below

Highlights:

- Mixed signal: wideband test for 5G
- 5G test: RF combo/Carrier Aggregation



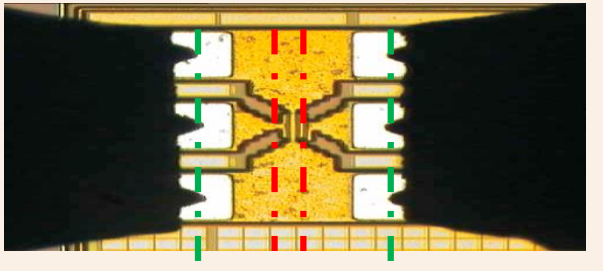
ATE based On-Wafer Test



On-Wafer Calibration

Probes:
- Coaxial to Coplanar Waveguide (CPW)
- GSG:

S-parameter Calibration:
- SOLT (Short Open Load Thru)
- TRL (Thru Reflect Line)
- LRRM (Line Reflect1/2 MatchLoad)
- CPW calibration cell
- Calibration algorithm



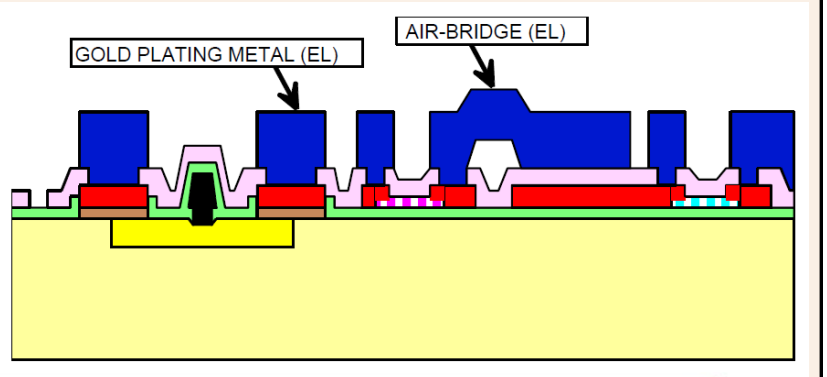
Intrinsic calibration:
de-embed to cell edge

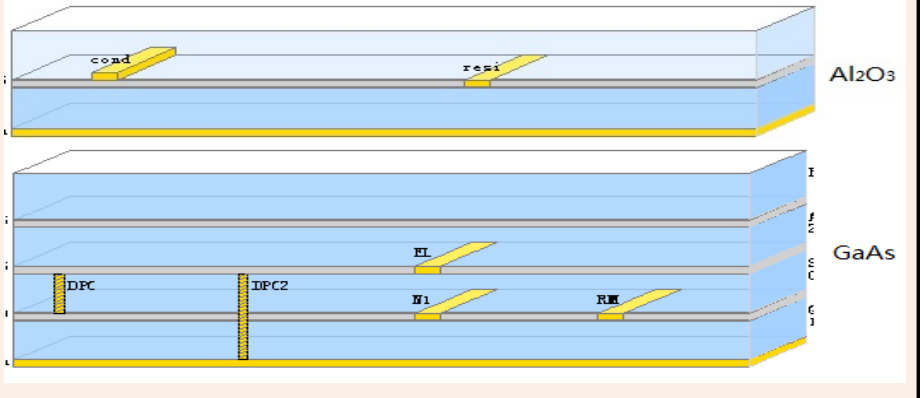
Challenge:
- Standard chip design: Foundry service
- Algorithm: CPW optimized
- Intrinsic calibration: de-embed pad and stub

On-Wafer Calibration Chip Design

Design flow:

- Substrate model
- Matched 50Ohm CPW TX line
- Matched load
- SOLT set
- TRL set
- Attenuation set
- VSWR set
- Momentum EM simulation
- Manual optimization

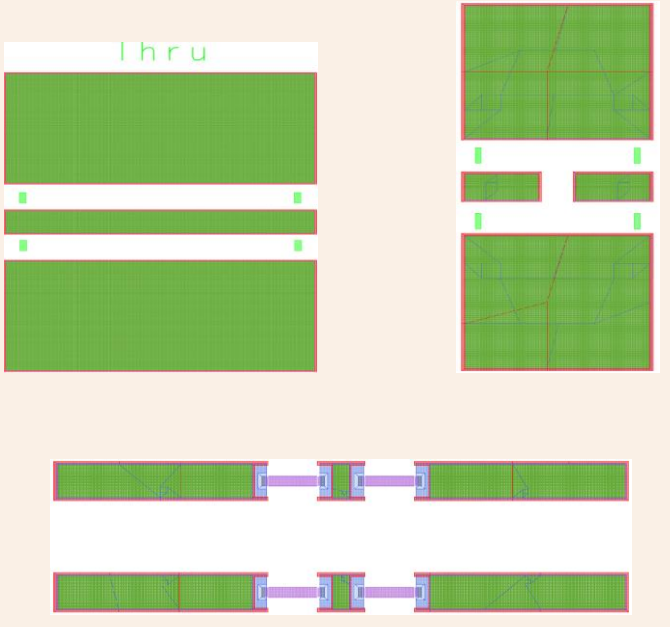




On-Wafer Calibration Chip Design

Design flow:

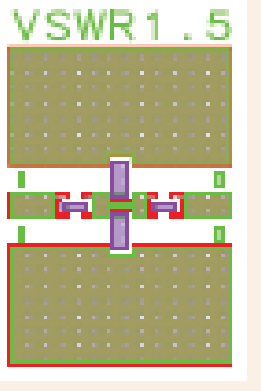
- Substrate model
- Matched 50Ohm CPW TX line
- Matched load
- SOLT set
- TRL set
- Attenuation set
- VSWR set
- Momentum EM simulation
- Manual optimization

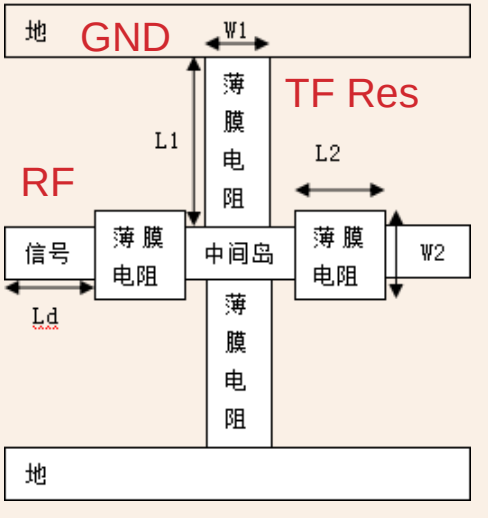


On-Wafer Calibration Chip Design

Design flow:

- Substrate model
- Matched 50Ohm CPW TX line
- Matched load
- SOLT set
- TRL set
- Attenuation set
- VSWR set
- Momentum EM simulation
- Manual optimization

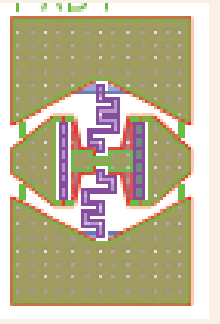


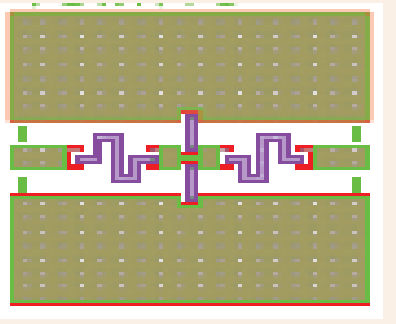


On-Wafer Calibration Chip Design

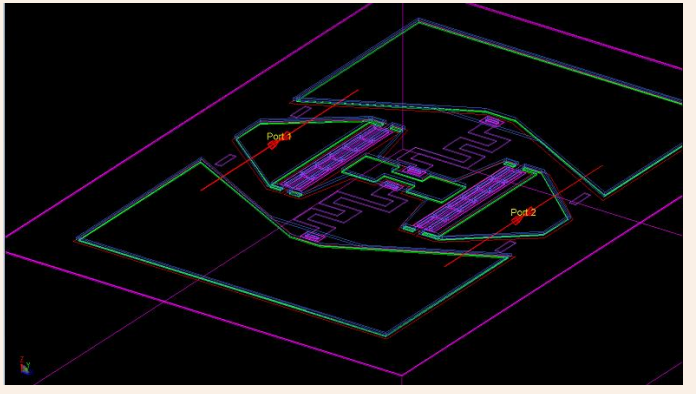
Design flow:

- Substrate model
- Matched 50Ohm CPW TX line
- Matched load
- SOLT set
- TRL set
- Attenuation set
- VSWR set
- Momentum EM simulation
- Manual optimization：
  Gradient and snake line





Manual layout optimization：
Gradient and snake line

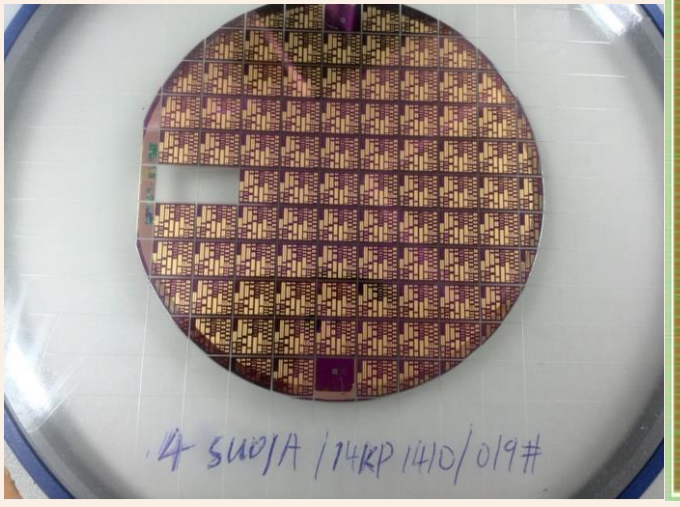


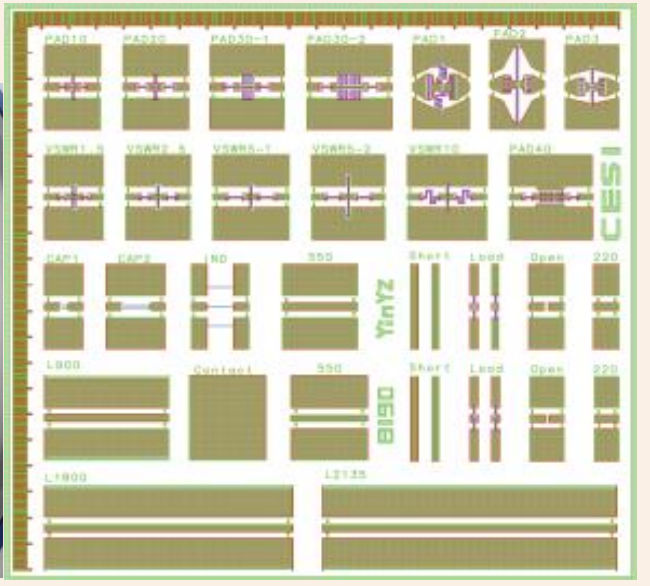
3D effect of manual layout optimization

CESI 8190 Calibration Standard

Main Features:

- SOLT and TRL Calkits. Long Line: 2.135mm
- Geometry Standard. 10um
- VSWR Verification: 1.1、1.5、2.5、5、10
- Attenuation Verification: 1dB、2dB、3dB、-10dB、-20dB、-30dB、-40dB
- On-Wafer capacitor and inductor
- Air bridge 1/2/4 cascade





ATE based On-Wafer Test

Algorithm flow:

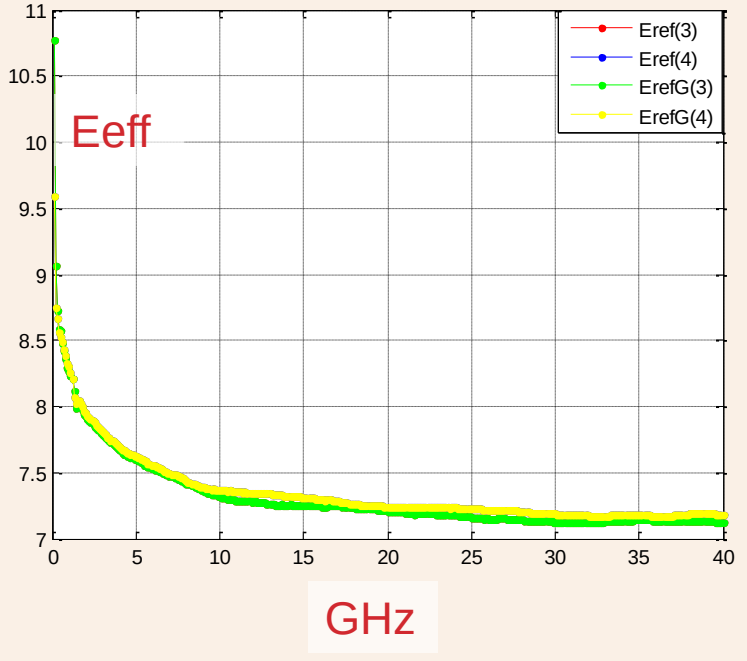
- Substrate effective dielectric constant (Eeff) and loss tangent (TanD) extract.
- Probe vector S parameter extract.
- Verification module calibration.
- 2/4 port calibration: Unique crosstalk for CMOS-RF.

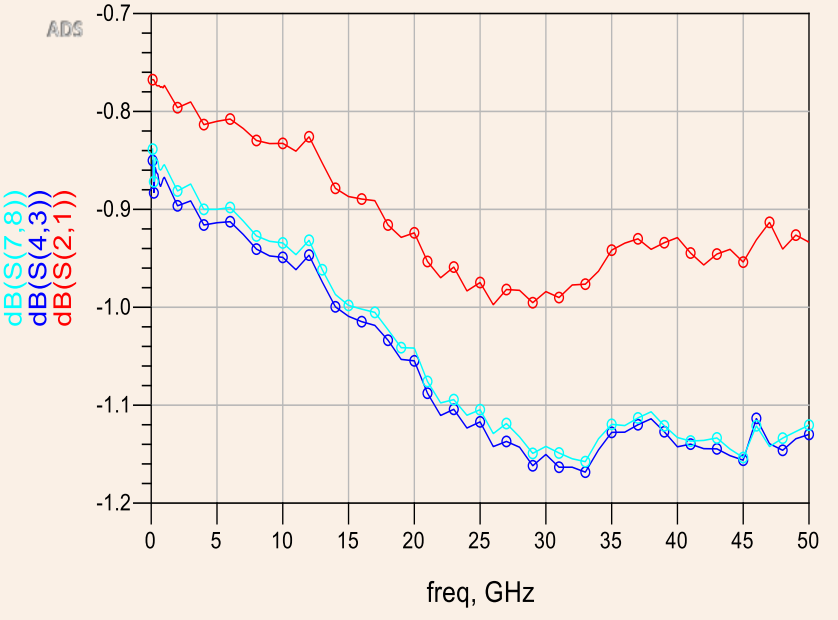
$$Q_{thru} = T_A \cdot T_{thru} \cdot T_B \qquad \gamma = \alpha + j\beta$$

$$Q_{Line} = T_A \cdot T_{Line} \cdot T_B \qquad Q_{Line} \cdot Q_{thru}^{-1} = T_A \cdot \left(T_{Line} \cdot T_{thru}^{-1}\right) \cdot T_A^{-1}$$

$$T_{Line} \cdot T_{thru}^{-1} = \begin{bmatrix} e^{-\gamma \cdot \Delta l} & 0 \\ 0 & e^{-\gamma \cdot \Delta l} \end{bmatrix} \qquad \gamma = \frac{1}{\Delta l} \cdot \ln\left(eig\left(Q_{Line} \cdot Q_{thru}^{-1}\right)\right)$$

Calibration Result





Summary

- The development of 5G promotes new IC volume test demands such as GaN and CMOS-RF/MEMS-RF components
- New 5G features brings to new test demands such as 6GHz+ mmW, RF Combo and Carrier Aggregation
- VNA On-Wafer test platform and 93k volume ATE take different advantages
- Both for VNA and ATE approach, the CPW On-Wafer calibration is required
- CESI 8180/8190 is developed for CPW On-Wafer calibration
- CESI Calkit algorithm and software are developed and compared to industrial solutions
- Future work: New 5G featured test and calibration; Si standards etc.