### Archive



Burn-in & Test Strategies Workshop

www.bitsworkshop.org

September 6-7, 2017

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#### **RF & High Speed Test**

### BiTS China 2017

# **100G Testing Fixture Design and Verification**

### Jackie Luo Shanghai Zenfocus Semi-Tech



BiTS China Workshop Shanghai September 7, 2017



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# Agenda

- 100G High-Speed Interface Introduction
- 100G High-Speed Interface Testing
- 100G Testing Fixture Design
- Testing Verification based on PLTS
  (*Physical Layer Test System*)
- Conclusion



100G Testing Fixture Design and Verification

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### **100G High-Speed Interface Introduction**

- Core/Data
- Switches
- Routers
- Servers
- Storage
- Standard I/O Interface
  - SFP+
  - QSFP+
  - miniSAS
  - ZQFP+

- ZQSFP+
- XCP
- CFP
- CFP2CFP4

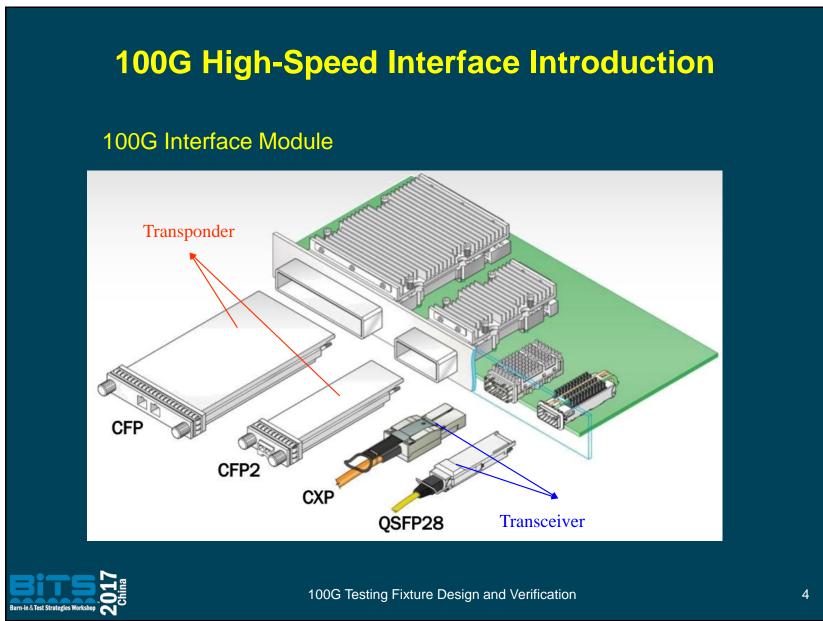




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### **100G High-Speed Interface Testing**

#### Host-to-Module Electrical Specifications (host output)

Parameter	Min.	Max.	Units			
Differential input		See Equation	ďB			
return loss	-	See Equation	۵D	ſ	9.5 - 0.37f	$0.01 \le f < 8$
Common to differential				$RLd(f) \ge $		, , , , , , , , , , , , , , , , , , , ,
mode conversion return	_	See Equation	dB	ning() =	$4.75 - 7.4 \log_{10}\left(\frac{f}{14}\right)$	8 ≤ <i>f</i> < 19
loss				l		J

#### Module-to-Host Electrical Specifications (host input)

Parameter	Min.	Max.	Units
Differential input return loss	_	See Equation	dB
Differential to common mode input return loss	_	See Equation	ďB

$$RLdc(f) \ge \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \le f < 12.89\\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \le f < 19 \end{cases}$$

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### **100G High-Speed Interface Testing**

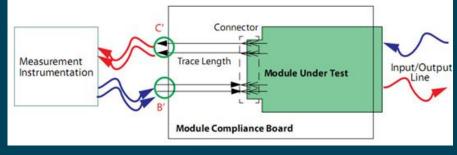
• Based on IEEE802.3bm (CAUI-4) Specification



**MCB : Module Compliance Board** 

**Parameters to be Tested:** 

**Test point: B'** Module\_OUTPUT\_SDD11max Module\_OUTPUT\_SDC11max



Test point: C' Module\_INPUT\_SDD11max Module\_INPUT\_SCD11max

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 $0.01 \le f < 8$ 

 $8 \le f < 19$ 

# **100G High-Speed Interface Testing**

 $RLd(f) \geq \langle$ 

### Module-to-Host Electrical Specifications (module output)

Parameter	Min.	Max.	Units
Differential input return loss	-	See Equation	dB
Common to differential mode conversion return	_	See Equation	dB
loss			

### Host-to-Module Electrical Specifications (module input)

Parameter	Min.	Max.	Units
Differential input		See Equation	ďB
return loss	—	See Equation	ι Ψ
Differential to common		See Equation	ďB
mode input return loss	-	See Equation	æ

$$RLdc(f) \ge \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \le f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \le f < 19 \end{cases}$$

9.5 - 0.37f

 $4.75 - 7.4 \log_{10} \left( \frac{f}{14} \right)$ 



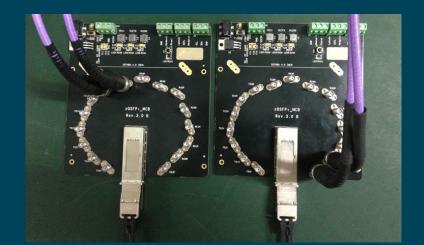
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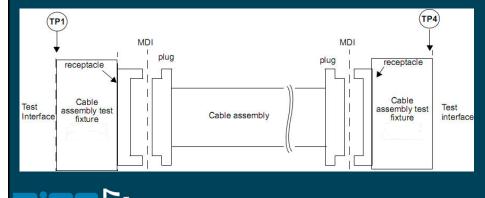
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### **100G High-Speed Interface Testing**

• Based on IEEE802.3bj Specification





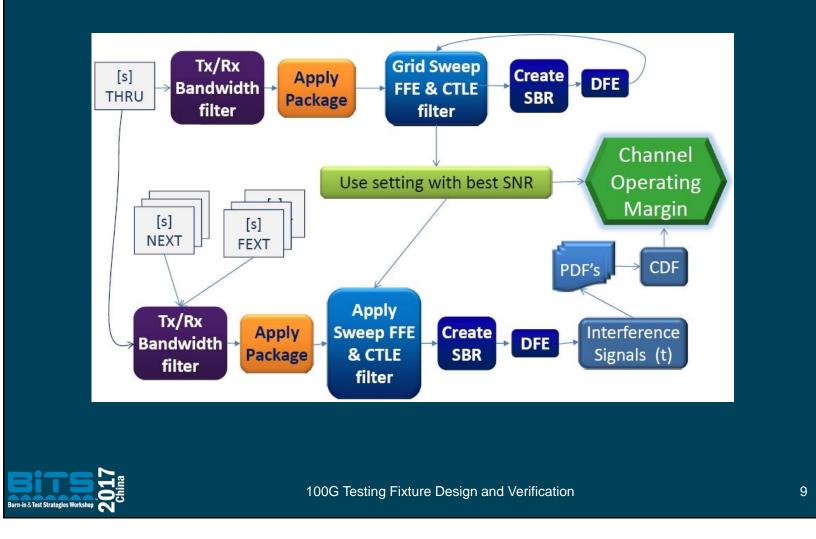
**Parameters to be Tested: Insertion** loss **Return loss Differential to common-mode** return loss **Differential to common-mode** conversion loss **Common-mode to common**mode return loss **COM** (Channel Operating Margin)

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### **100G High-Speed Interface Testing**



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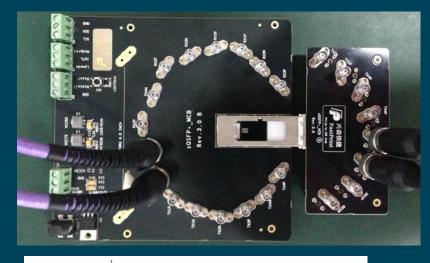
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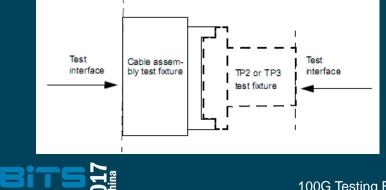
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# **100G High-Speed Interface Testing**

Fixture Mating Testing Based on IEEE802.3bj Specification



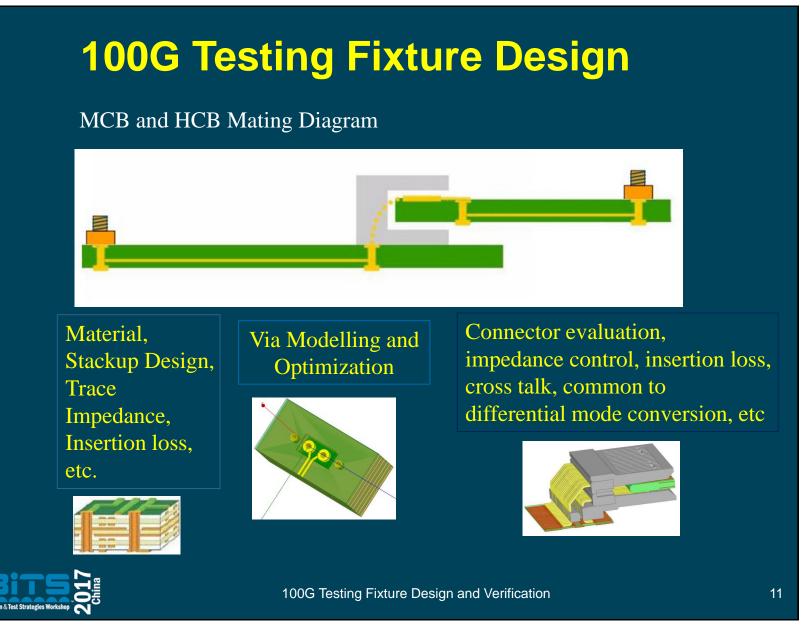


Parameters to be Tested: Insertion loss Return loss common-mode to Differential return loss Differential to common-mode conversion loss Common-mode to common-mode return loss Integrated crosstalk noise

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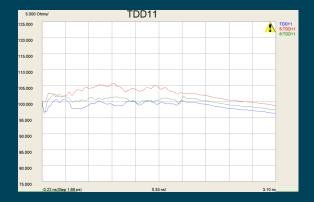
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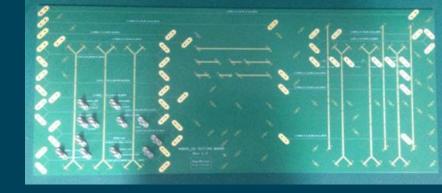
### **100G Testing Fixture Design**



IL VS. Trace Width/Air Gap



Impedance VS. Trace Width/Air Gap



Material Verification Board, use AFR (Automatic Fixture Removal) or PLTS ((Physical Layer Test System) ) to do calibration, to get real performance of the material after fabrication

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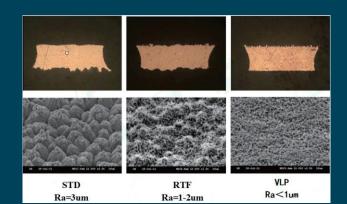
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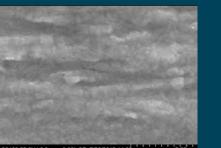
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# **100G Testing Fixture Design**

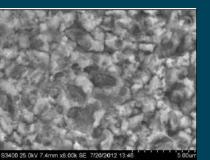
#### copper foil Roughness

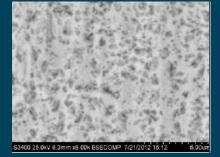


Different Processes contribute to different roughness after fabrication









Before Fabrication(VLP) After Traditional Process After low-roughness process



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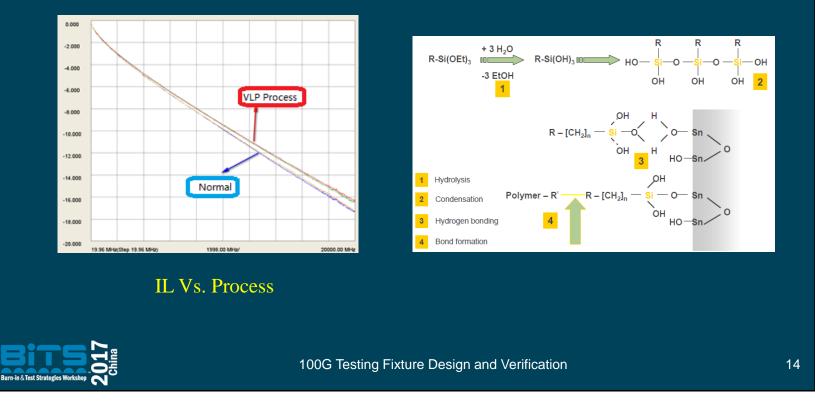
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# **100G Testing Fixture Design**

### Low-Roughness Process

#### Take full advantage of HVLP copper foil



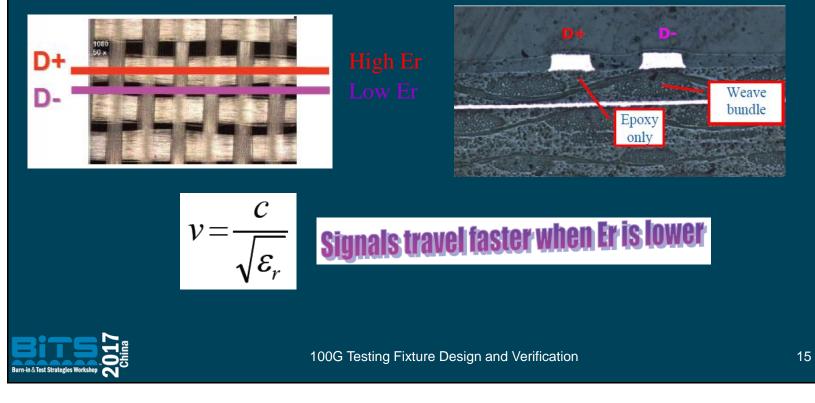
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### **100G Testing Fixture Design**

#### **Glass Fiber Impact to Differential Signals**

Differential signals transmit on High Er and Low Er media will have differential delays



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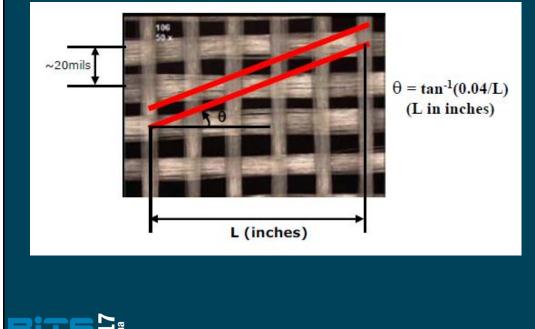
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# **100G Testing Fixture Design**

#### **Glass Fiber Impact to Differential Signals**

Improvement:

- 1. Design rotated traces;
- 2. Fabricated rotated patterns;



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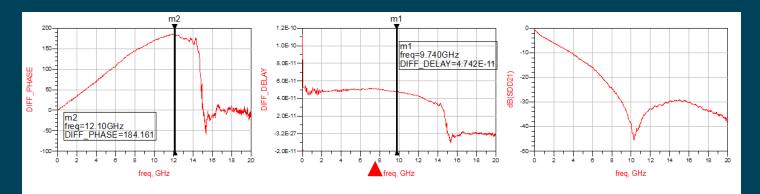
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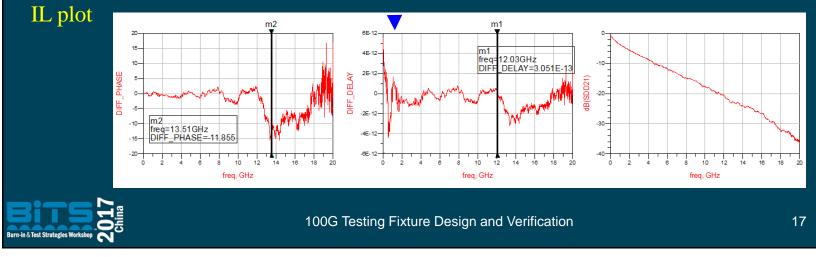
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# **100G Testing Fixture Design**

Material with issue, phase and delay will be abnormal, and has resonance in IL plot



Material without issue, the phase and delay will be normal, and has no resonance in

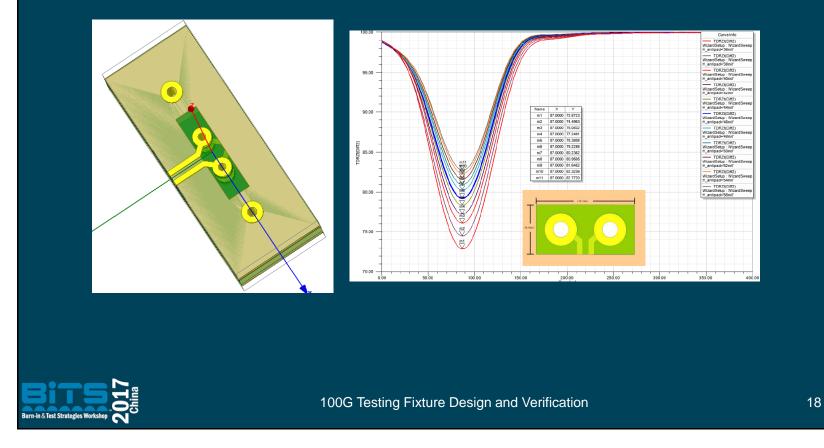


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# **100G Testing Fixture Design**

### Via Modelling and Optimization

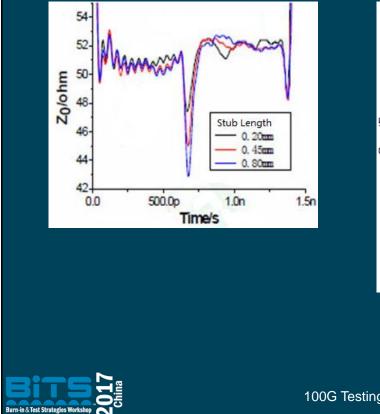


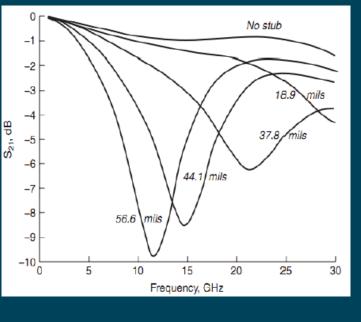
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# **100G Testing Fixture Design**

### STUB length impact to signal Performance





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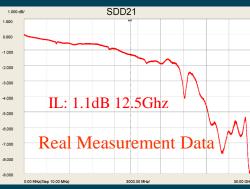
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### **100G Testing Fixture Design**



### **Connector Selection**

- 1. Insertion Loss
- 2. Return Loss
- 3. Differential pair delay
- 4. Xtalk



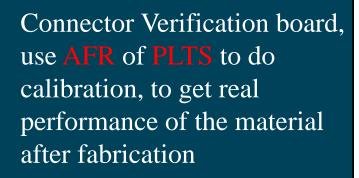
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### **100G Testing Fixture Design**





3. Measure Standards	4. Rem	ove Fixture	5.	Save Fixture	٢	
1. Describe Fixture	2. Specify			y Standards		
This 5 step wizard characterizes an	id removes	the fixture eff	ects from y	our measurement	<u>t.</u>	
My fixture inputs are:						
Single Ended					Ш.	
ODifferential	- 7					
My measurement is:	с	urrent Fixture	and DUT A:	sumptions		
○1 Port		Fixture Match				
2 Ports		Fixture Length DUT ZO: will b		vstem ZO		
OMultiport 🚽						
Advanced Settings						
After fixture removal set Calib		eference ZO to				
⊙″System ZO″						
○Measured Fixture Z0						
0 50 Ohms						
Set "System ZO" to Calibrat:	ion Refe	rence ZO				
▼I want to correct for Fixture						
I want to correct for Fixture	Length	A ≠ B				
My fixture is band limited(us			mode)			
Lay ristare is band rimited (da	ie ballape	uo cimo uomain	2040/			
	N	ext	Exit	Help		



100G Testing Fixture Design and Verification

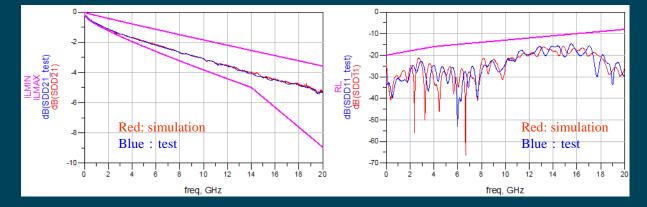
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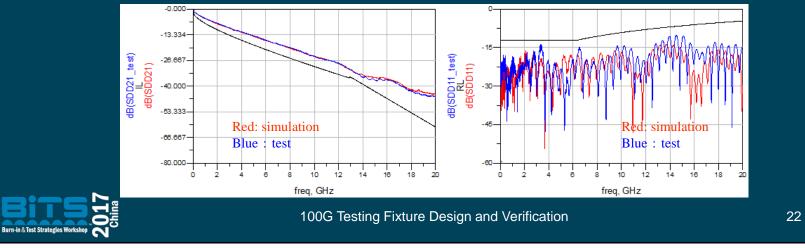
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### **100G Testing Fixture Design**

Get parameters from real evaluation board of material and connectors, then simulate to get the performance of the whole trace



This method works for long distance board also (40inch, Meet IEEE802.3bj Spec)



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### **Fixture Verification based on PLTS**

#### MCB and HCB Verification







### Testing Setup :

- 1. Keysight PXI Modular network analyzer
- 2. PLTS physical layer testing SW
- 3. Calibration kits, Coaxial Cables, etc.

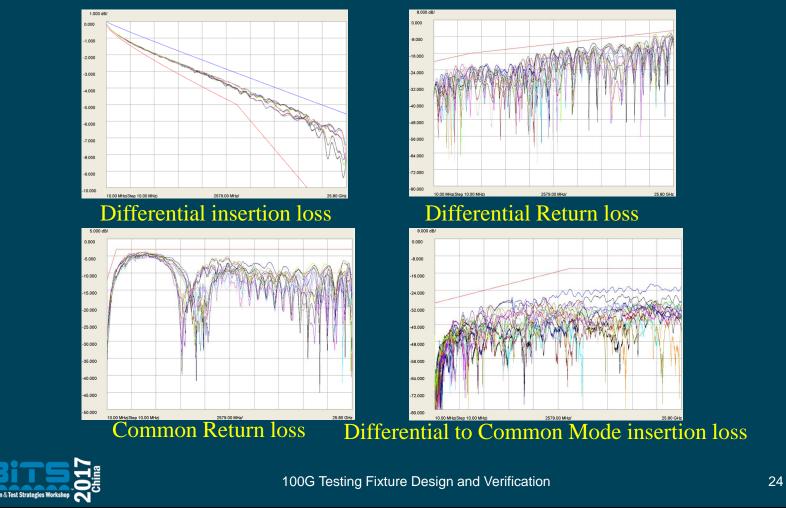
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### **Fixture Verification based on PLTS**

#### Comparison with IEEE802.3bj Spec



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### Conclusion

- High-Speed Testing moved from some independent modules to an integrated complex system
- To design a testing fixture which perform as good as expected, we need to evaluate material, stackup, trace, via, interconnection and connectors to get real performance of each segment, then simulate the whole trace to get whole trace performance.
- Fixture verification based on PLTS gives the fixture performance comparing with Specification
- The same methodology can be leveraged to cover higher and higher testing requirement in ATE environment.



100G Testing Fixture Design and Verification