
BiTS
CHINA 中国
September 6 - 7, 2017
InterContinental Shanghai Pudong Hotel -
Shanghai, China
Archive
©2017 BiTS Workshop. Image: Easyturn/iStock

COPYRIGHT NOTICE

www.bitsworkshop.org

Fan Out Technology Overview

Dr. Tingyu Lin
National Centre for Advanced Packaging (NCAP China)

BiTS China Workshop
Shanghai
September 7, 2017

Contents

- **NCAP Overview**
- **Fan out Technology Introduction**
  - Market analysis
  - Major technologies and global players
  - Patent aspects & distribution
  - Main process technologies
  - Challenges & solutions
  - China OSATs on fan out executions
- **NCAP Wafer Level and Panel Level Fan out**
- **Consortium Updated**
- **Conclusions**

NCAP Overview

- **Established in Wuxi in 2012**
- **10 investors**
  - Including the Institute of Microelectronics and the largest OSATs and substrate companies in China (JCAP, NT Fujitsu, WLCSP, ANJILI, WULIWANG, SCC, NDB, IME, Hua Tian, XIN Sheng Kuai Jie)
- **Independent business entity**

NCAP Platform

Wuxi Headquarters

- 3000m^2 Cleanroom
- Class 10/100/1,000/10,000
- 8″/12″ wafer

Beijing Center

- 1000m^2 Cleanroom
- Class 1,000/10,000

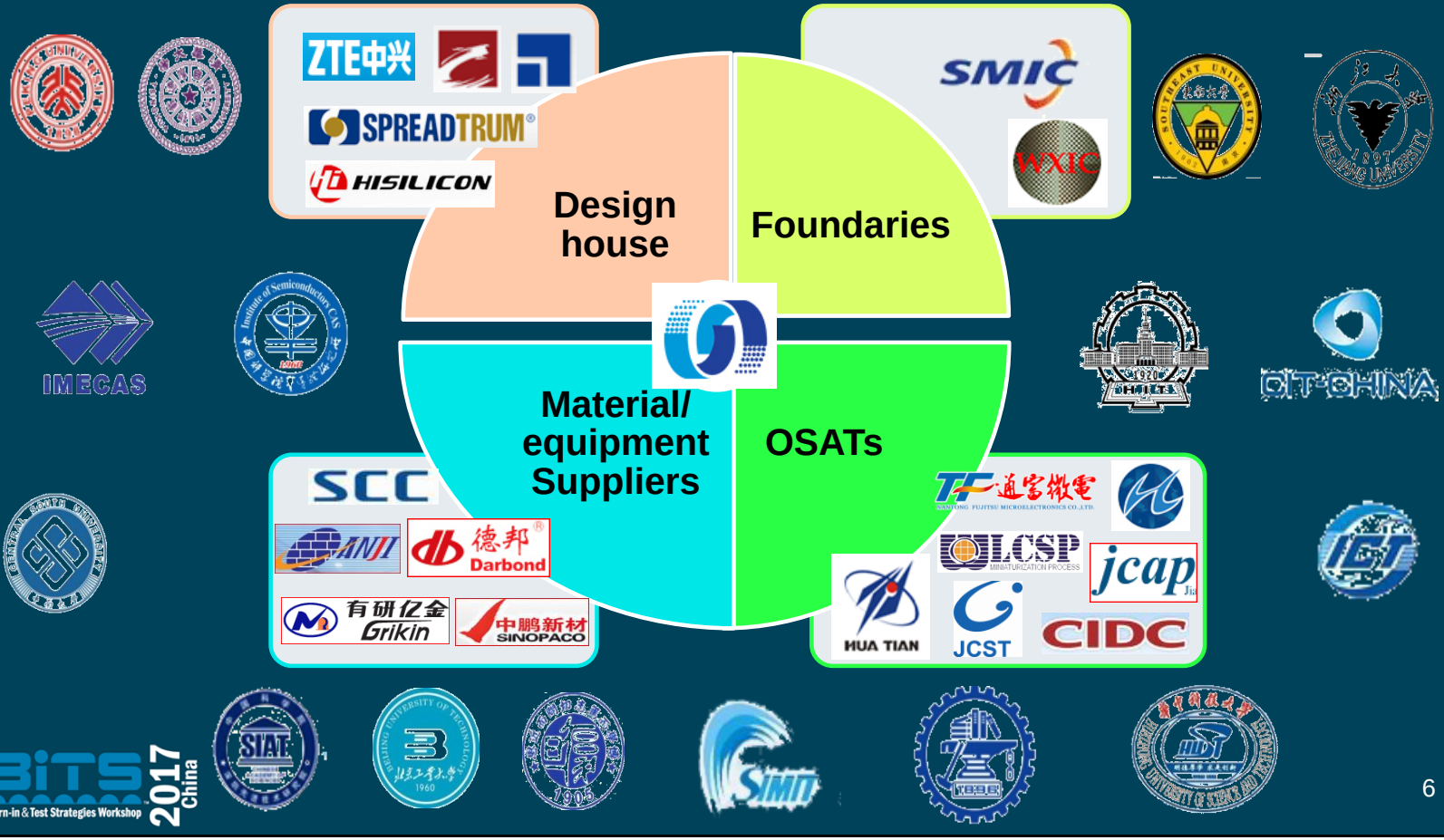
- **R&D & Engineering with 9000m2**
- **engineering assembly &metrology equipment with ￥160 million，fixed total equipment value ￥ 345 million。**

R&D Infrastructures

address：Building D1, China Sensor Network, International Innovation Park, 200 Linghu Boulevard, WuXi, Jiangsu Province, China

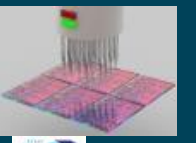
Industry / Institute Collaboration

- collaborate with industry partners and institutes, proceed small quantity of manufacturing



NCAP Role in Innovative Channel

Equipment / Materials



Final Test

Substrate

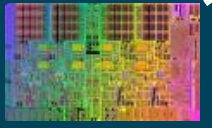
Package Assembly

Wafer Bumping/Probing

SIP Design

TSV

Fab



IC Design

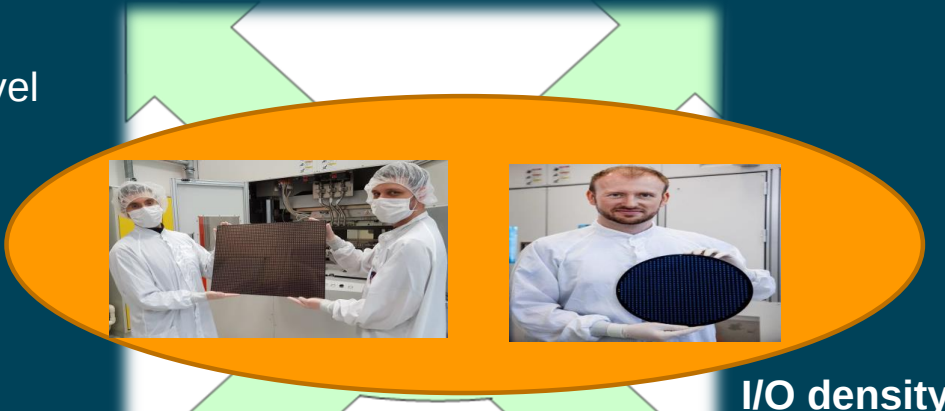
Why Fan-out

Performance

- ☑ Shorter interconnect length, high speed application;
- ☑ Superior package level reliability,
- ☑ Excellent board level reliability

Form Factor

- ☑ Thinner package,
- ☑ Package size Scalability



Cost Advantage

- ☑ Substrate /gold free,
- ☑ Scalable to the large panel (600mm above)

I/O density

- ☑ Small pitch,
- ☑ High pin counts

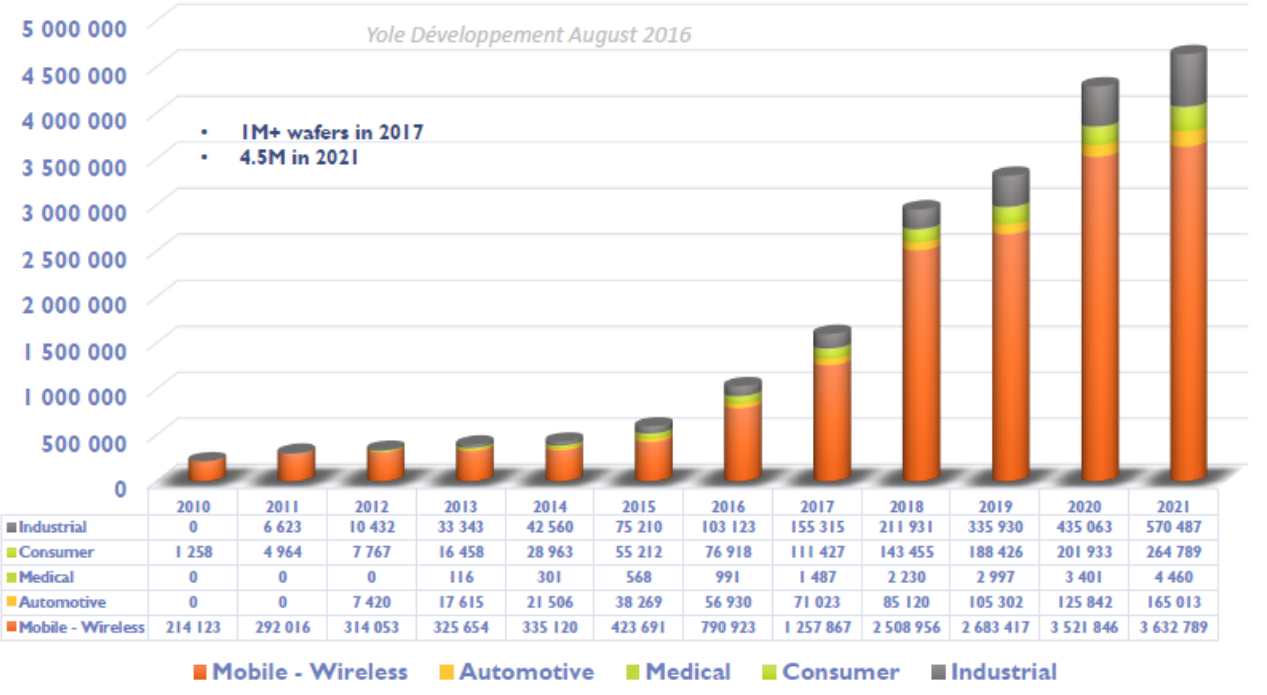
Fan Out Market Forecast

FAN-OUT ACTIVITY - MARKET FORECAST

Executive Summary

Fan-out activity forecast (300mm eq wafers) breakdown per end-market

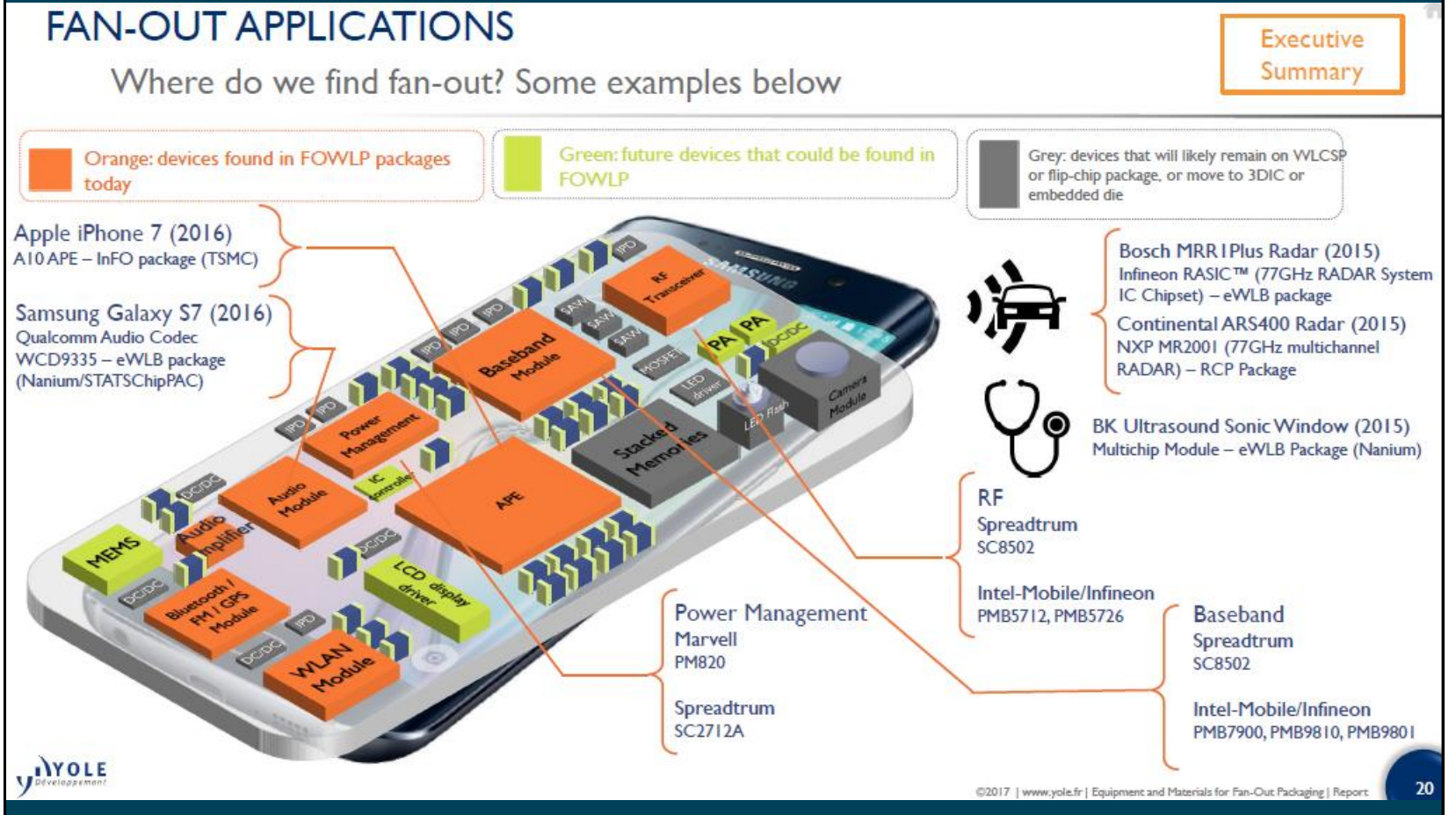
Apple's example will show competitors the way



	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
Industrial	0	6 623	10 432	33 343	42 560	75 210	103 123	155 315	211 931	335 930	435 063	570 487
Consumer	1 258	4 964	7 767	16 458	28 963	55 212	76 918	111 427	143 455	188 426	201 933	264 789
Medical	0	0	0	116	301	568	991	1 487	2 230	2 997	3 401	4 460
Automotive	0	0	7 420	17 615	21 506	38 269	56 930	71 023	85 120	105 302	125 842	165 013
Mobile - Wireless	214 123	292 016	314 053	325 654	335 120	423 691	790 923	1 257 867	2 508 956	2 683 417	3 521 846	3 632 789

19

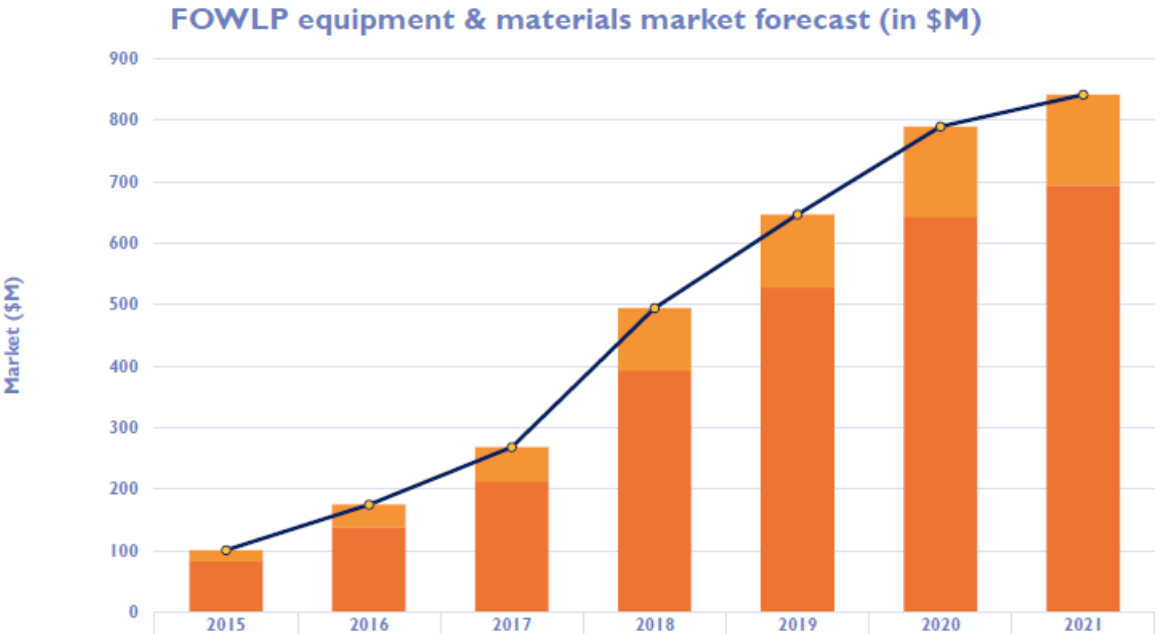
Fan Out Applications



Fan Out Material & Equipment

FOWLP* - TOTAL MARKET FORECAST FOR EQUIPMENT AND MATERIALS

Executive Summary



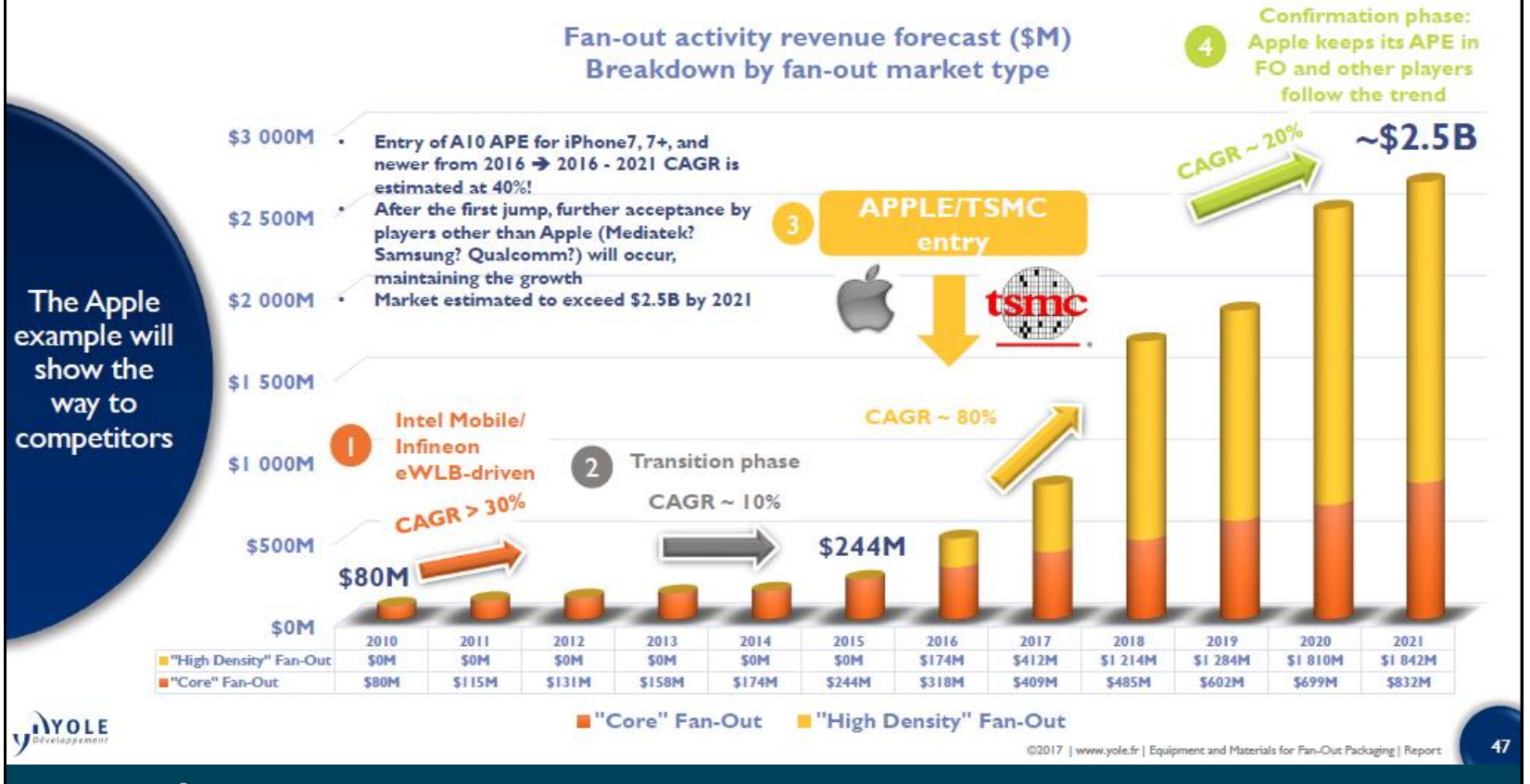
	2015	2016	2017	2018	2019	2020	2021
Materials	18	36	56	102	119	147	148
Equipments	83	138	213	392	528	642	694
Total	101	175	268	494	646	789	841

*The market estimated here only includes process steps investigated by Yole for this report, and is not exhaustive. For details, see the following slides for breakdowns, along with the "fan-out process steps to focus on" slides in the "Challenges" section.

26

Fan Out Market Development

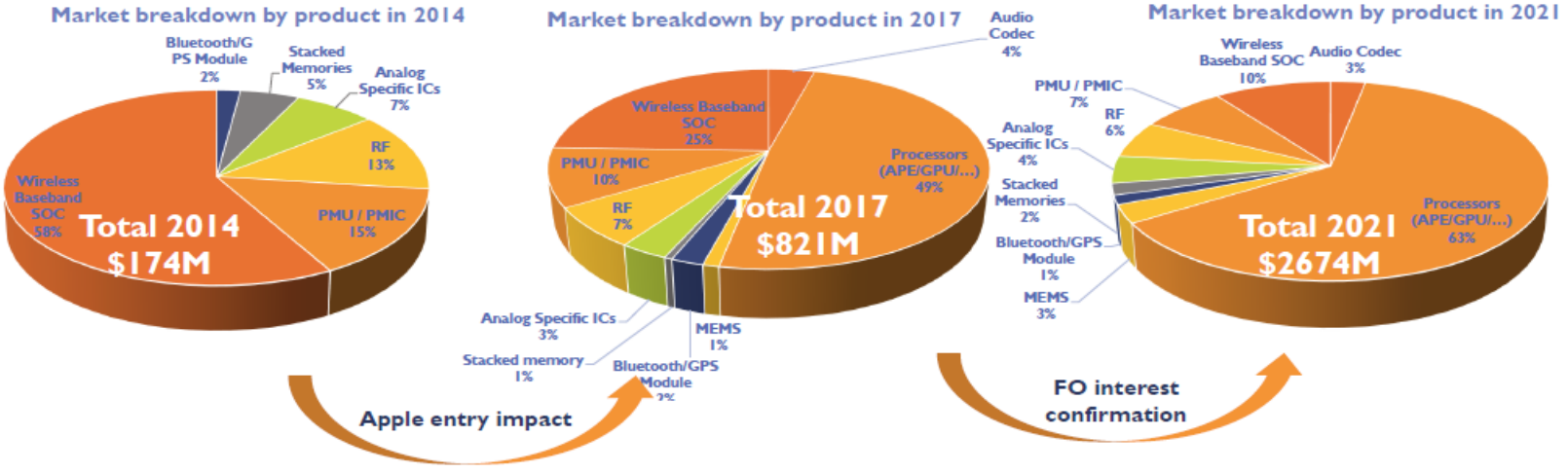
FAN-OUT ACTIVITY - MARKET FORECAST (1/2)



Fan Out Market Scale

FAN-OUT ACTIVITY - MARKET FORECAST

Breakdown by product type and evolution



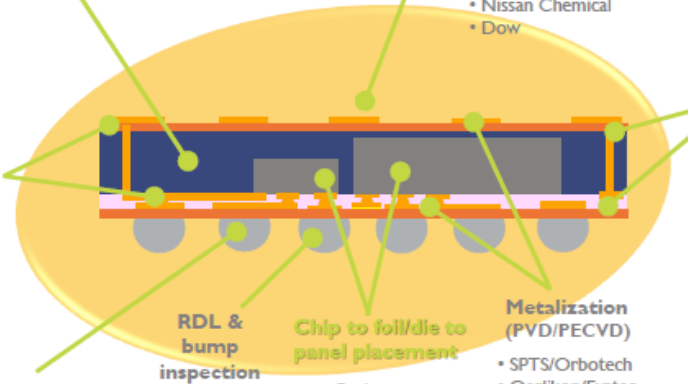
- The « core » fan-out market is evolving:
  - BB/Wireless, PMU/PMIC, and RF are the main driving applications, but fan-out has improved and qualified for MEMS and other non-mainstream products
  - Fan-out is starting to appear in wider applications: GPS modules, Wifi applications, Audio codec, and some specific niche automotive and medical
  - applications
- « HD » fan-out APE/GPU and complex applications will comprise the majority of the fan-out market (high revenue), fueled by iPhone followers
  - Fan-out's higher integration capability will offer access to markets where flip-chip PoP/SiP currently dominate
  - More complex applications will follow: stacked memory, ASICs, CPU/GPU, etc.

YOLE Développement

51

Global Fan Out Supply Chain

SPECIFIC EQUIPMENT & MATERIALS FOR FAN-OUT MANUFACTURING*



Mold compound encapsulant
- Nagase ChemteX
- Henkel
- Sumitomo
- Nitto-Denko
- Hitachi
- Panasonic
- Shin Etsu

Wafer/panel molding equipment
- ASM
- Towa
- Yamada
- Hanmi
- Besi

Exposure & lithography
- SUSS MicroTec (Laser Ablation)
- Rudolph, Ultratech, Ushio, SUSS MicroTec, ORC, Nikon, Canon (Steppers)

Temporary bonding/debonding solution

→ Laminated adhesive tapes
- Nitto Denko
- JSR
- Brewer Science
- 3M
- Shin Etsu
- Wacker
- TOK
- HD Microsystems
- Nissan Chemical
- Dow

→ Glass hard carrier
- Corning
- Schott
- AGC
- NGK
- NEG

→ Temporary bonding/debonding equipment
- Nitto Denko
- EVG
- SUSS MicroTec
- Tazmo
- TEL

Dielectric passivation and photo-resists
- Merck
- Fujifilm
- JSR
- Asahi Kasei
- Shin-Etsu
- Sumitomo
- DOW
- AGC
- Toray
- HD Microsystems
- Nippon Kayaku
- TOK

→ Coaters
- SUSS Microtec
- Screen
- TEL

Metalization (PVD/PECVD)
- SPTS/Orbotech
- Oerlikon/Evatec
- Tango Systems
- ULVAC
- Canon
- Applied Materials
- NEXX/TEL
- Veeco
- Lam Research

Chip to foil/die to panel placement
- Besi
- Amicra
- Capcon
- Hanmi
- Toray
- Shibaura
- ASM
- Shinkawa
- Kulicke&Soffa

RDL & bump inspection
- Rudolph
- Camtek
- Unity SC
- Nanometrics
- Xradia
- KLA-Tencor

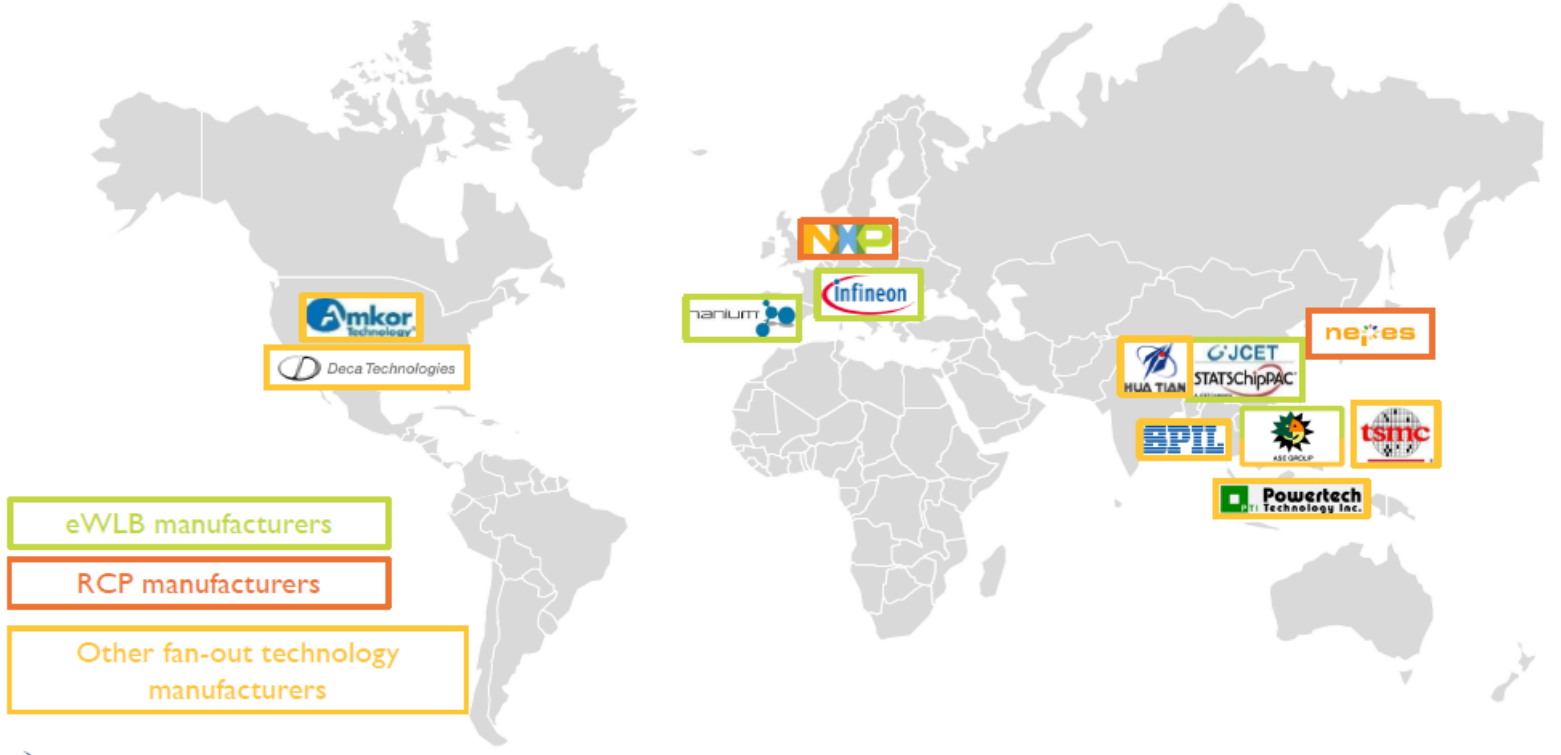
Wafer test & Functional test
- Akrometrix

*Partial list of players

YOLE Développement

Global Fan Out Players

FAN-OUT PACKAGING LANDSCAPE - MAIN PLAYERS (1/2)

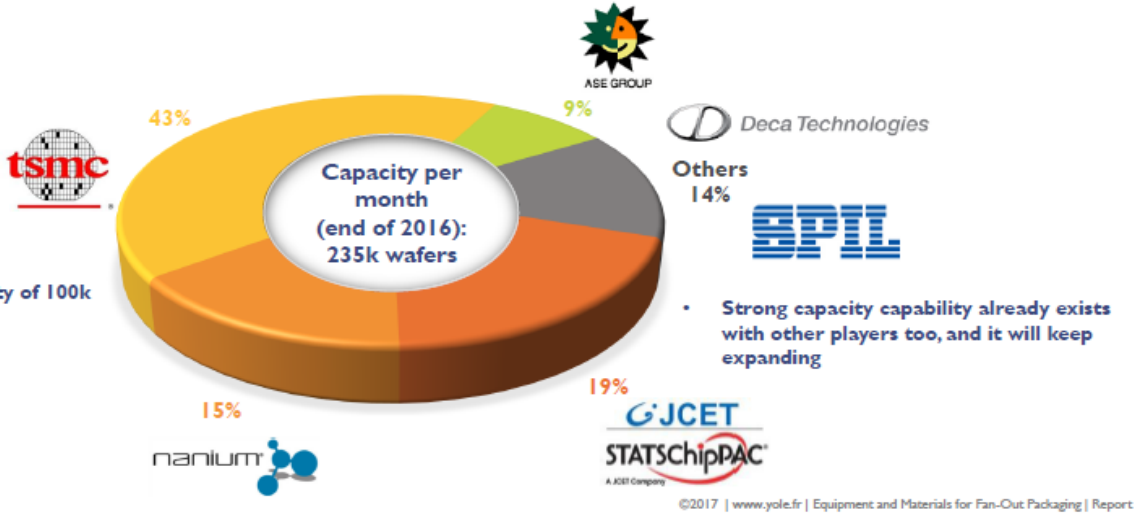


55

Global Fan Out Market Capacity

FOWLP - ALREADY-INSTALLED CAPACITY

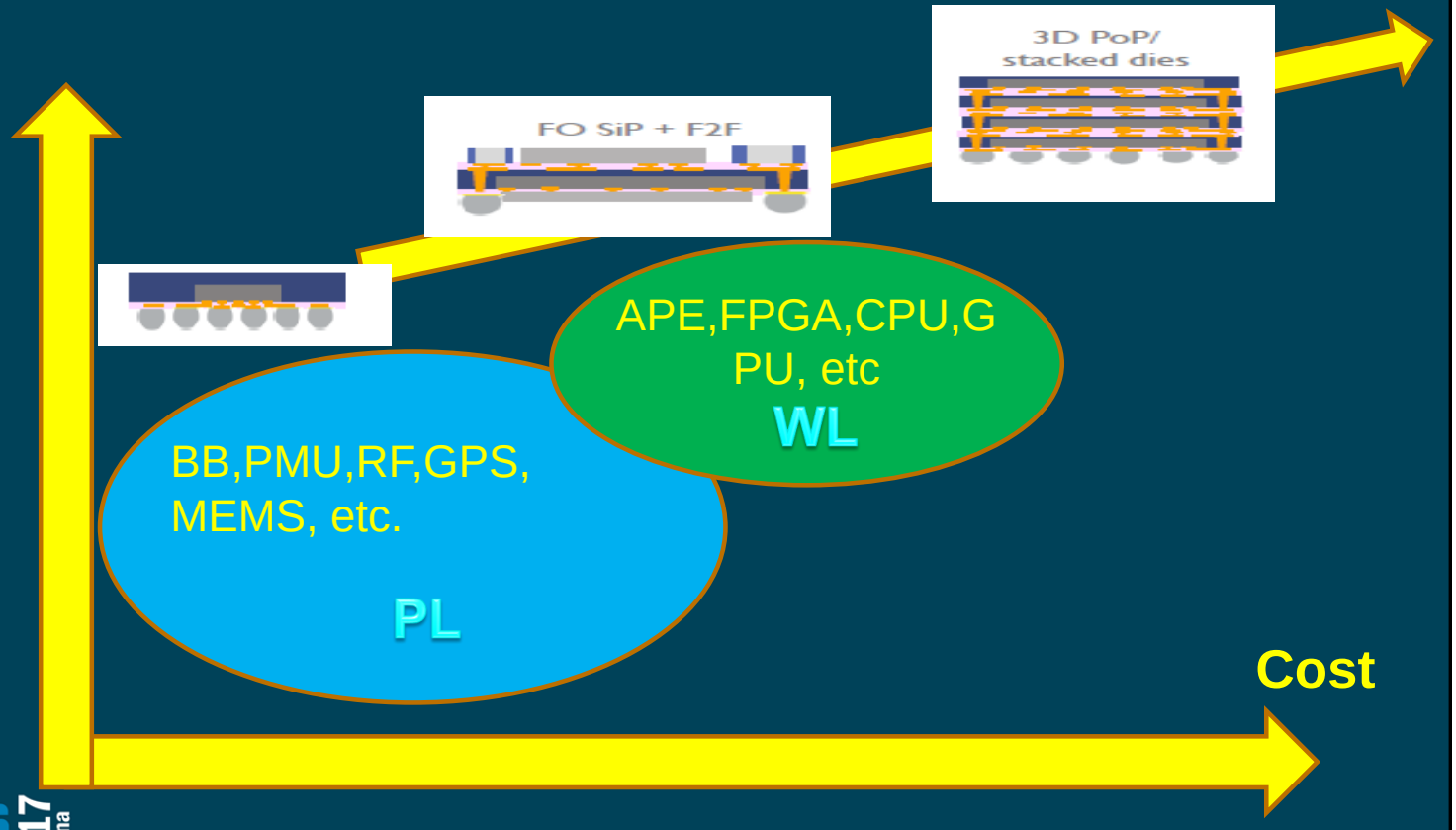
- At the end of 2016, fan-out investments were already very important, and consequently so is capacity
  - With a capacity of 100,000 wafers/month, TSMC's InFO product has the largest capacity
  - Other main manufacturers are established eWLB providers: Nanium and STATS ChipPAC. Each can produce around 10,000 wafers per week.
  - STATSChipPAC is enlarging its capacity to raise production
  - Since TSMC's action was quite formidable, investment in equipment for 2017 will not be as high - but it will still be decent:
  - Led by newcomers willing to have a FOWLP offer
  - As well as major players willing to enlarge their capacity (STATSChipPAC and potentially ASE together with Deca)
- With 4.5M wafers to be produced in 2021, capacity must be increased by TSMC and/or other actors. Therefore, a second wave of investment will occur later on; otherwise, capacity be insufficient for addressing the FOWLP market if it keeps growing (see the following slides).



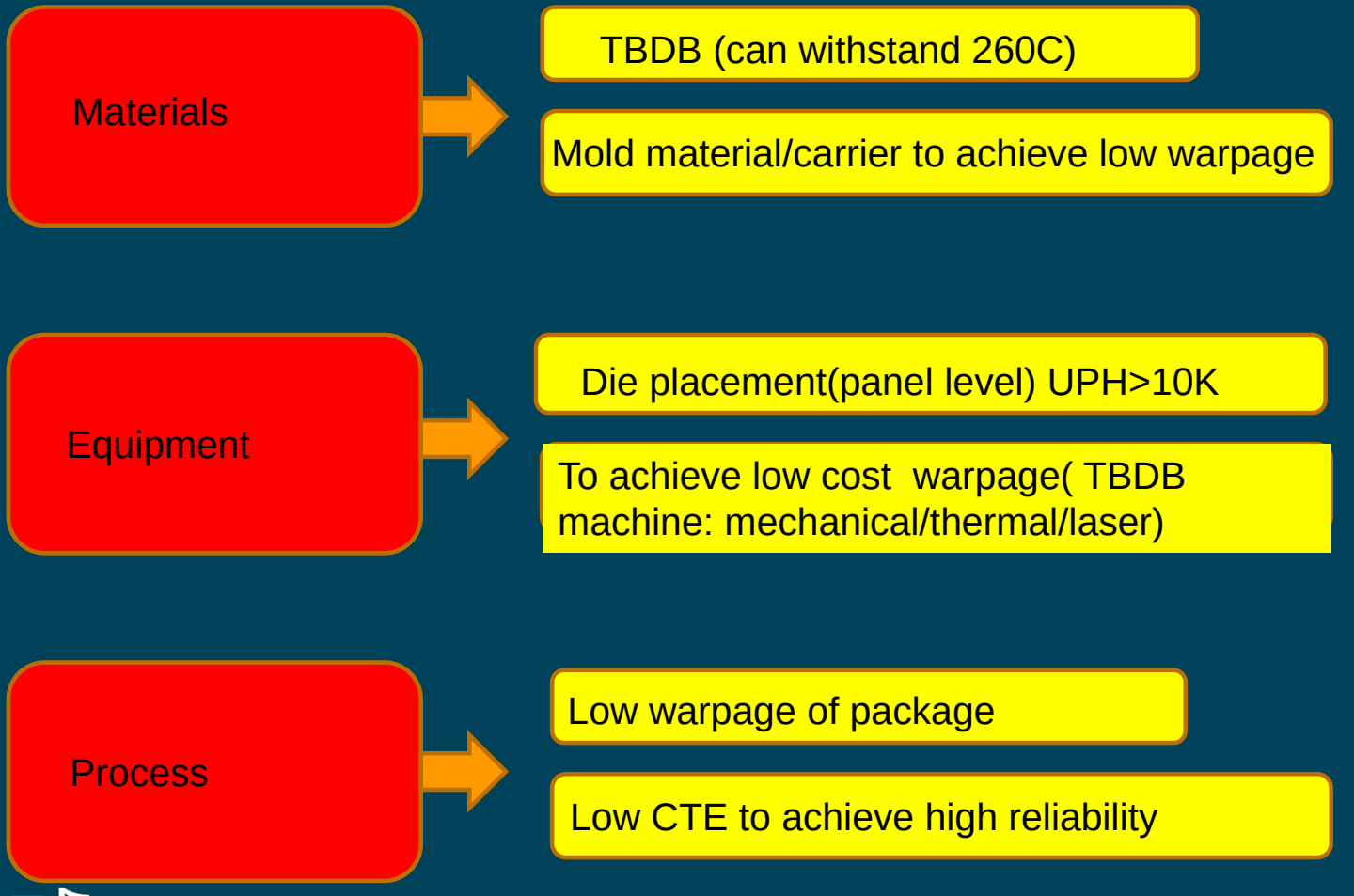
Development Trend

Performance (L/S; pitch; multiple die, etc.)

Single chip to Multichip , Development from two dimensional to three-dimensional



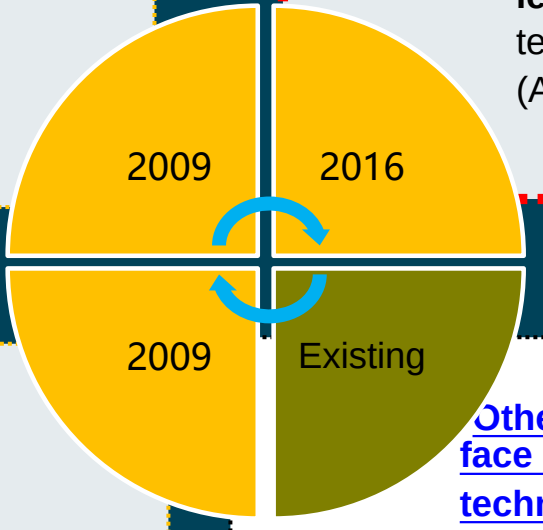
Technology Challenges



Major Fan Out Technologies

- **eWLB (wafer level)**
- First fanout patent filed at 2001
- Shipped out 1billion units since mass production in 2009

- **TSMC InFO (wafer level)** : Apple used this technology in iPhone 7 (A10 processor)。



- **RCP** technology

(wafer level), from frees , and licensed NEPES,
- Low volume shipment

Others (e.g., DECA (chip face up panel level) technology ; ASE licensed this technology (panel level, and ship out 100 million units)

Key Player Technology

FAN-OUT - KEY PLAYERS' ACTIVITY SUMMARY (1/2)

	Production status	Production information	Technology	L/S minimal features (2016)	Driving applications	Driving customers
ASE (TW)	• In volume production on 300mm (eWLB and in-house fan-out) • Line creation (M-series)	• Production on 200mm until 2012 • 300mm volume production since 2015 • In 2016, fab start for panel manufacturing (M-series)	• eWLB license (Chip-first face-down) • M-Series license (Chip-firstface-up)	5µm L/S	BB, PMU, RF	Qualcomm, Mediatek
STATSChipPAC (SG)	• In volume production on 300mm and 330mm	• >10,000 wafers/week • >1B units sold since 2009 • R&D ongoing for production on panels	• eWLB license (Chip-first face-down)	5µm L/S	BB, PMU, RF	Qualcomm, Broadcom, Spreadtrum, Cirrus Logic, Mediatek
Deca Technologies (US)	• In volume production on 300mm • Line creation for panel ongoing	• >100 million units since 2011 • Panel production 80% ready	• M-Series (Chip-first face-up)	5µm L/S	BB, PMU, RF	Cypress, Qualcomm
NANIUM (PT)	• In volume production on 300mm	• >500 million units on the market since 2010	• eWLB license (Chip-first face-down)	5µm L/S	BB, PMU, RF, GPS, MEMS	Qualcomm, Marvell, Mediatek

Nanium and STATSChipPAC are about to be joined by strong competitors in the FOWLP market

59

Key Player Technology

FAN-OUT - KEY PLAYERS' ACTIVITY SUMMARY (2/2)

	Production status	Production information	Technology	L/S minimal features (2016)	Driving applications	Driving customers
SPIL (TW)	• R&D and sampling	• Production capability since 2015 on 300mm wafers	• SLIT (Chip-last with fab BEOL)	• <1µm L/S expected	FPGA, CPU, GPU	Xilinx
Amkor (US)	• R&D and sampling	• Production capability since 2015 on 300mm wafers	• SWIFT (Chip-last) • SLIM (Chip-last with fab BEOL)	• 2µm L/S expected (SWIFT) • <1µm L/S expected (SLIM)	• BB, PMU, RF, APE • CPU/GPU	?
TSMC (TW)	• In volume production on 300mm	• 300mm volume production since 2016	• InFO (Chip-first face-up)	• 5µm L/S	• APE	Apple
Nepes (KR)	• In volume production on 300mm	• 300mm volume production since 2013 (previous experience in Singapore since 2009)	• RCP license (Chip-first face-Down)	• 5µm L/S	• BB, PMU, RF, APE	NXP, Sony
PTI (TW)	• R&D and line creation	• 510 x 515mm panels - volume production expected in 2017 • Wafer production capability since 2016	• CHIEFS (Chip-first) • CLIP (Chip-last)	• 2µm L/S expected	• BB, PMU, RF • APE • FPGA, CPU, GPU	?

Nanium and STATSChipPAC are about to be joined by strong competitors in the FOWLP market

Major IPs for Fan out

RDLs to fan out the circuitry from die edges without using substrate

US006727576B2

(12) **United States Patent**
Hedler et al.

(10) **Patent No.: US 6,727,576 B2**
(45) **Date of Patent: Apr. 27, 2004**

(54) **TRANSFER WAFER LEVEL PACKAGING**

(75) Inventors: **Harry Hedler**, Germering (DE); **Thorsten Meyer**, Erlangen (DE); **Barbara Vasquez**, Munich (DE)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/044,000**

(22) Filed: **Oct. 31, 2001**

(56) **References Cited**

U.S. PATENT DOCUMENTS

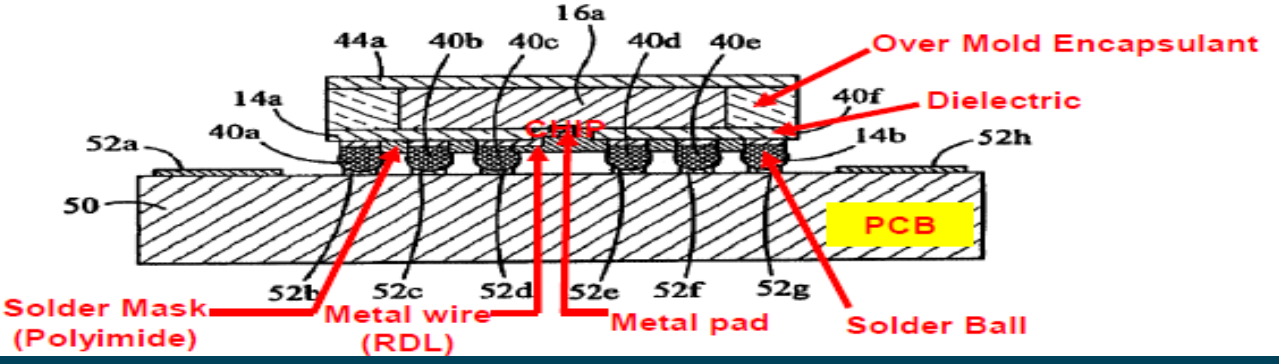
6,537,848 B2 * 3/2003 Camenforte et al. 438/106

* cited by examiner

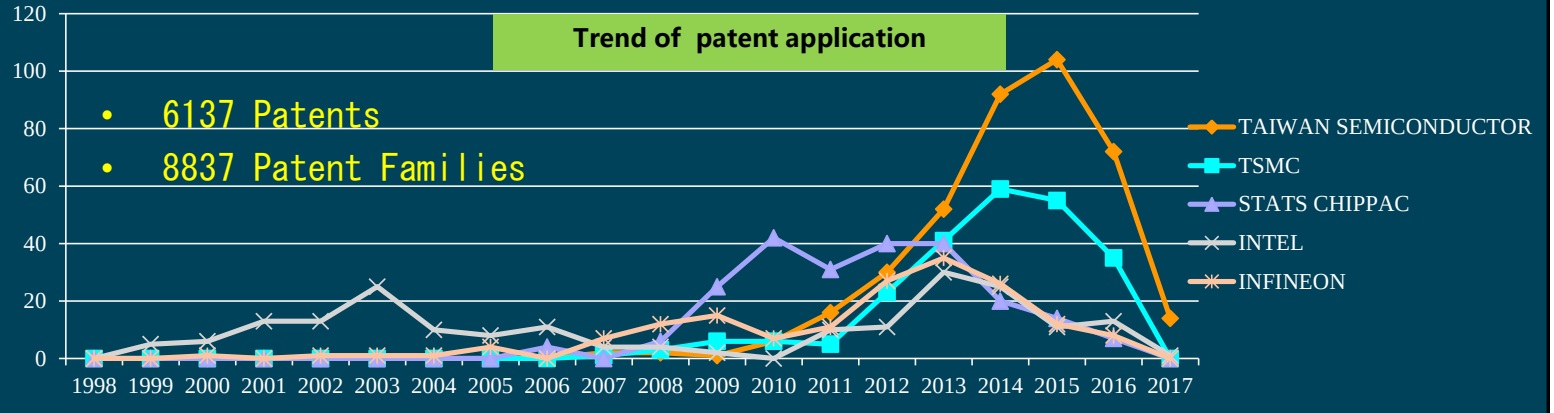
Primary Examiner—David Nelms
Assistant Examiner—Mai-Huong Tran
(74) *Attorney, Agent, or Firm*—Fish & Richardson

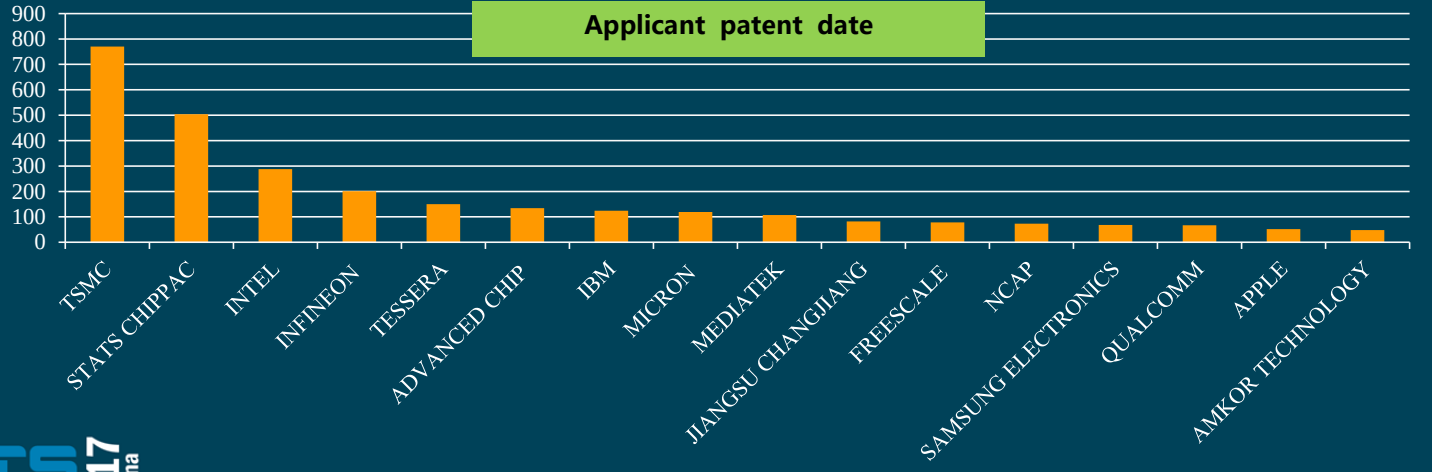
(57) **ABSTRACT**

A semiconductor structure and a method for forming the semiconductor structure, including a semiconductor chip



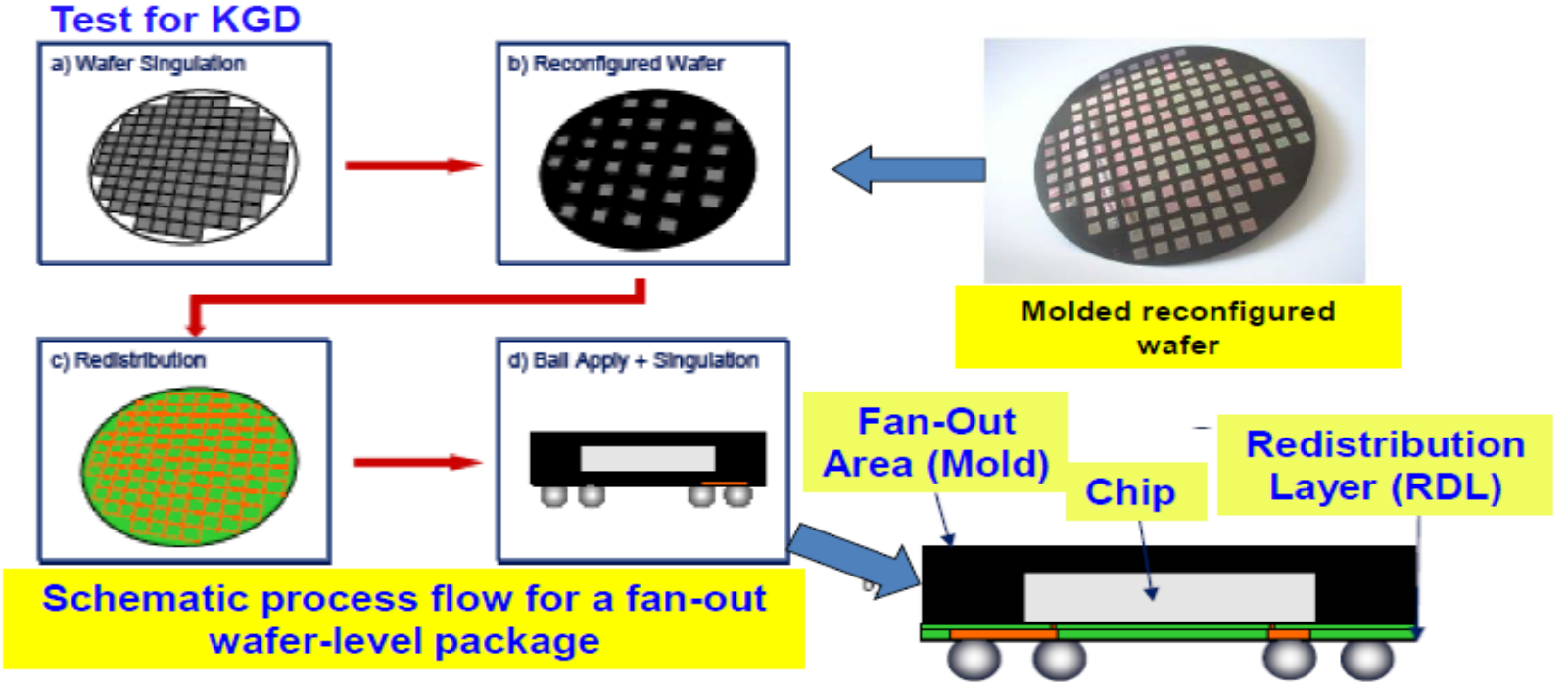
Global IP Distribution





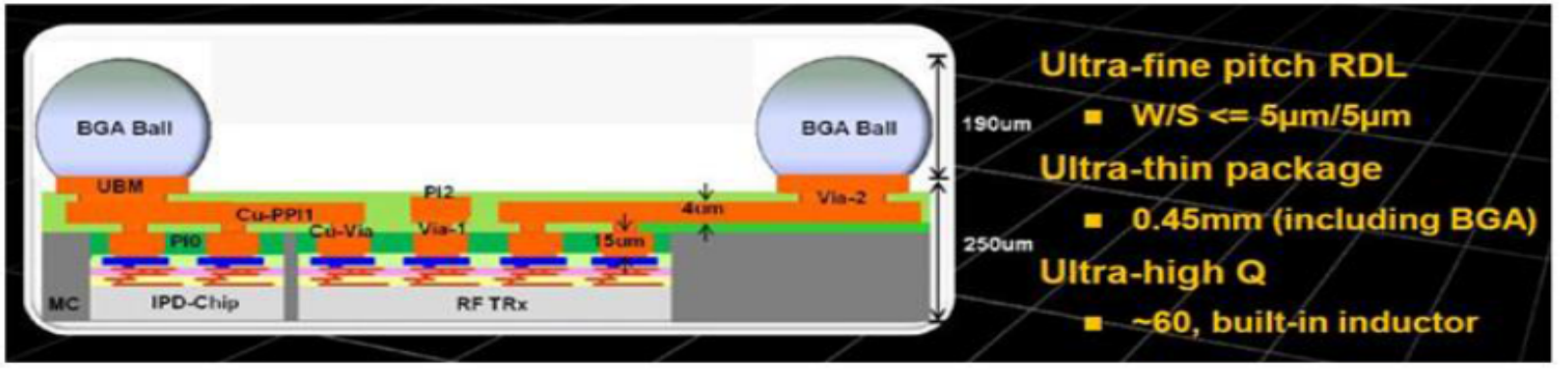
eWLB Major Process

Infineon's Embedded Wafer-Level Ball Grid Array (eWLB)



TSMC InFO Main Process

TSMC InFO-WLP (Integrated Fan-Out WLP)



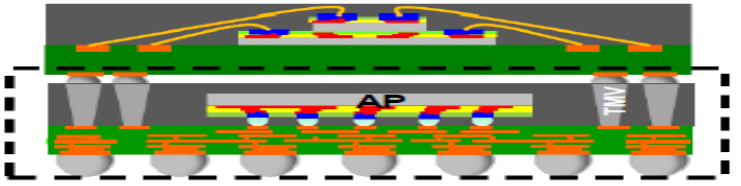
At the TSMC Technology Symposium in San Jose, CA in April 2014, TSMC announced the latest InFO-WLP platforms:

- 8mm x 8mm is targeted at RF and WiFi chips
- 15mm x 15mm is targeted at application processor and baseband chips
- 25mm x 25mm could be applied to GPU and networking chips

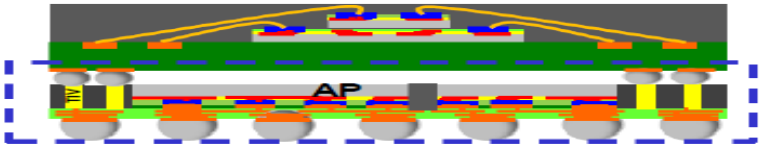
TSMC InFO PoP Structure

TSMC's InFO_PoP

Conventional PoP for Application Processor (AP) chipset



TSMC's PoP for Application Processor (AP) chipset

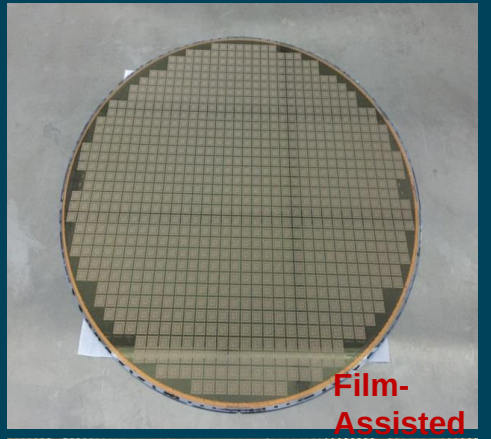


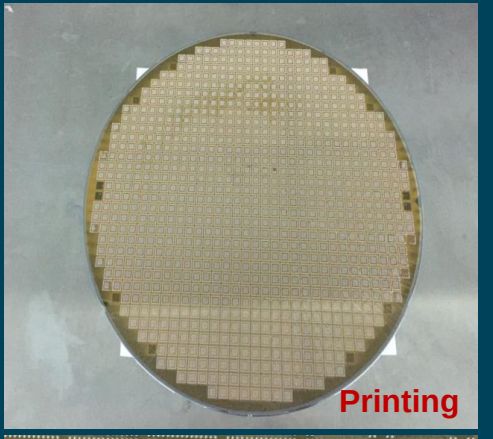
Eliminated solder bumps, underfill, and package substrate. Lower Profile!

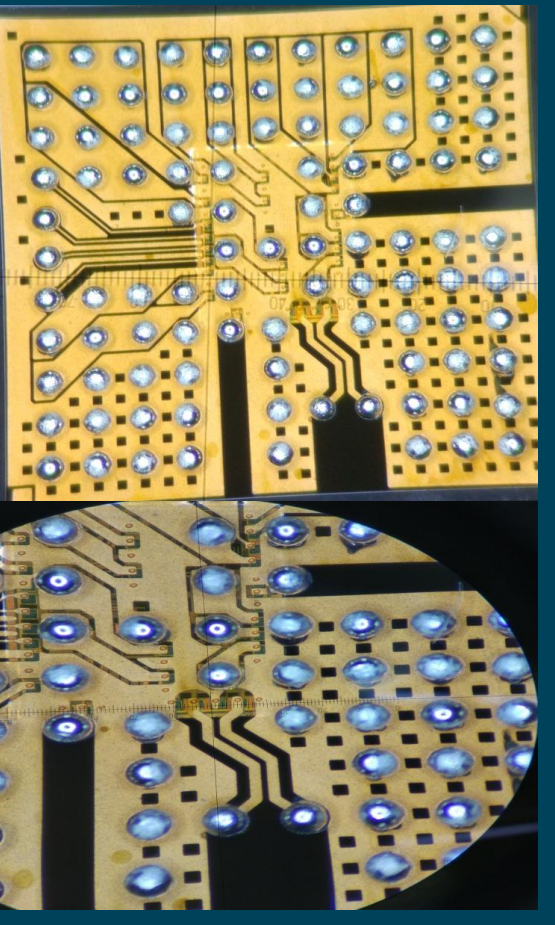
Status of Fan Out Development (China OSATs)

OSAT in China	Packaging Fan out Technologies available	status
Hua Tian Scientific Co., Ltd	eSIFO ™	Qualified and engineering samples are ready; and ready for ramping in the production
JCET	MIS technology based	Ready for mass production
NT Fujitsu	Panel level fan out	In development

NCAP eWLB Sample Builds

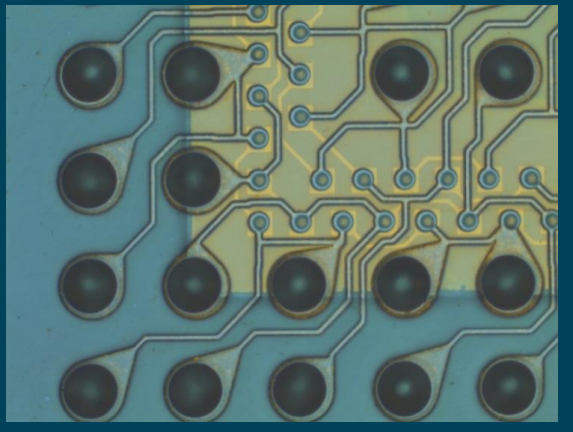


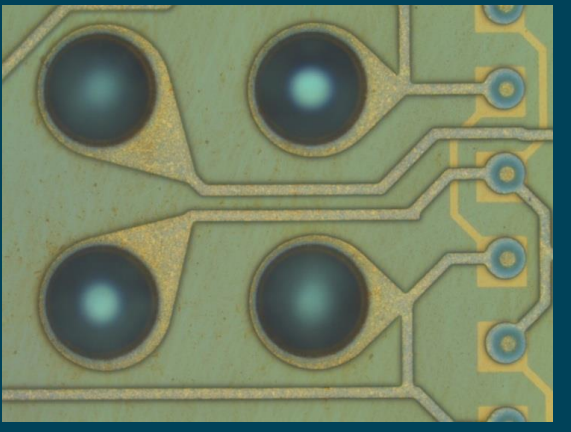


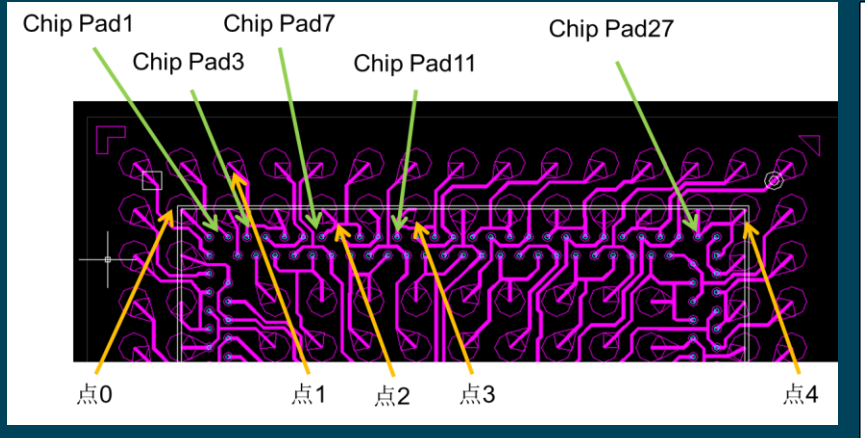


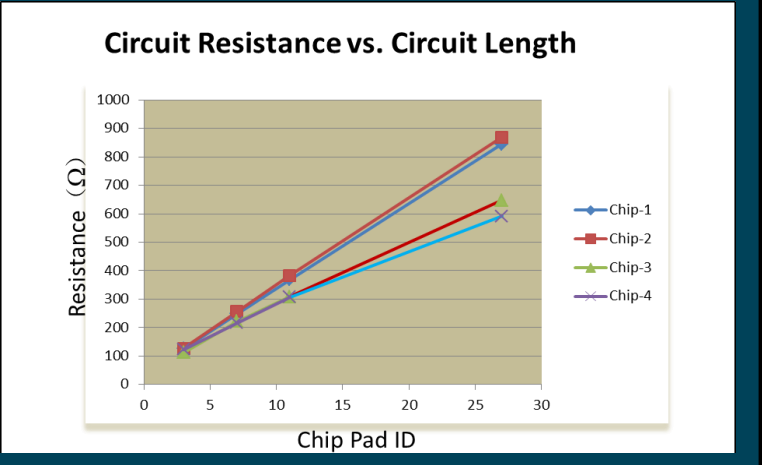
77G eWLB sample

NCAP WL Fan out Test Results





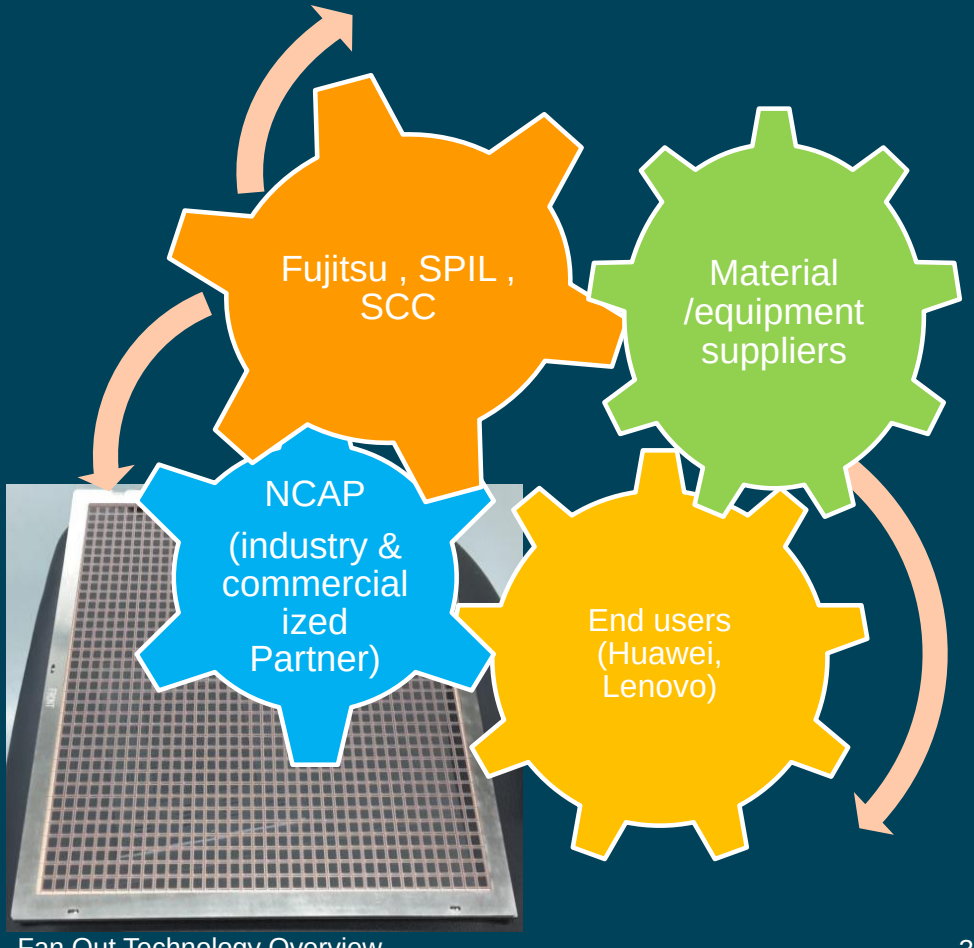




Large Panel Fan Out Consortium

- **Objective:** Development and characterization of large panel fan out design, process and reliability, provide supply chain analysis and justification for commercialization

No.	Key members
1	NCAP
2	SCC (深南)
3	SPIL (Taiwan)
4	Sinopaco（中鹏）
5	AMC（Taiwan)
6	Delphilaser（德龙）
7	Fujitsu
8	TOWA
9	Bee-semi(中电科)
10	JSR
11	Screen
12	KohYoung (高永)
13	Savansys
14	Huawei
15	Mascem（技美）
16	Sumitomo
17	Shin-Etsu(信越)
18	DNP（大日本印刷）
19	ASM
20	Ingenic(君正)
21	ORC
22	SCHOTT
23	Atotech
24	See ray
25	Lenovo

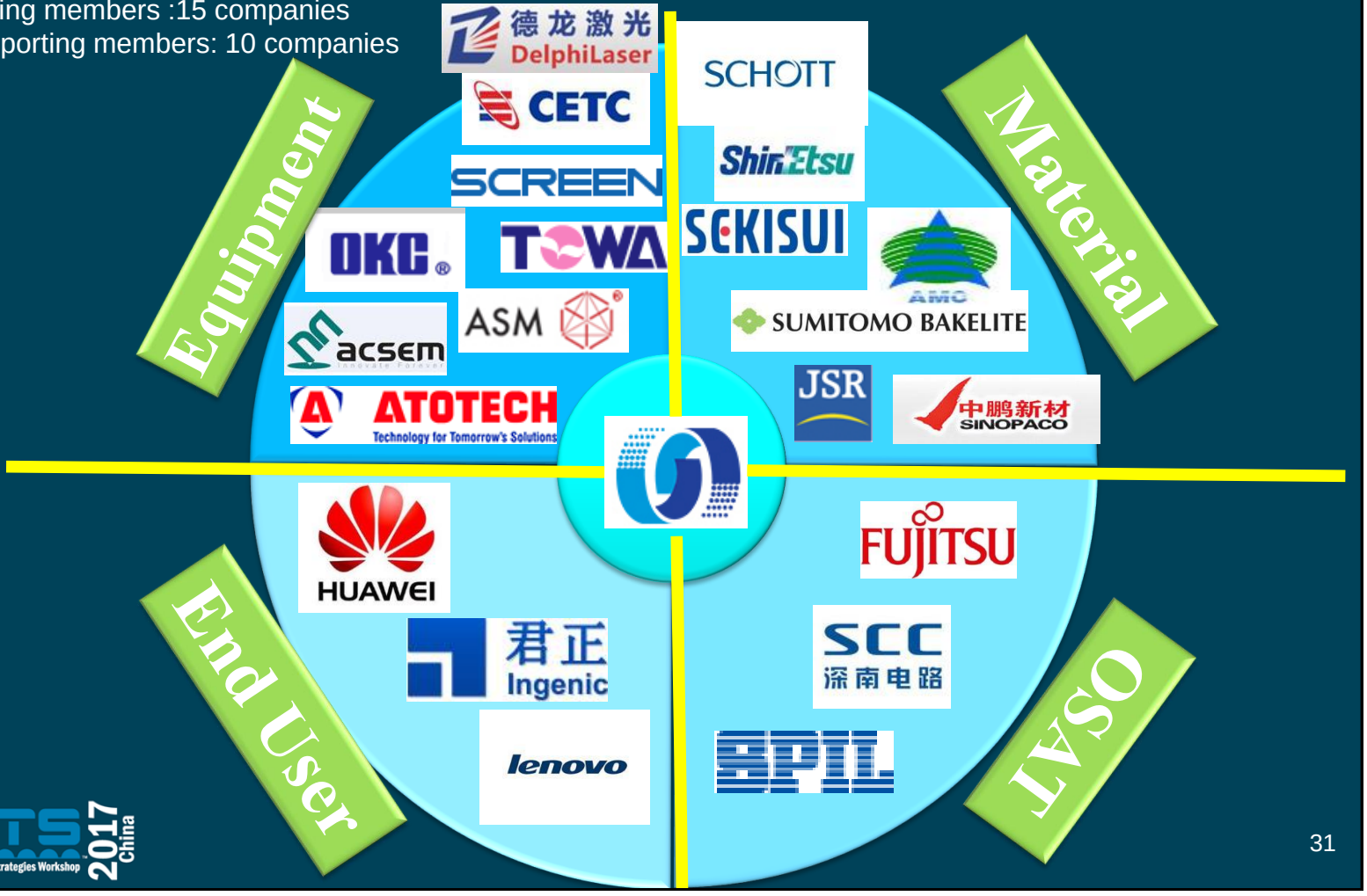


Fan Out Technology Overview

30

Consortium Key Members

Membership fee: US$20K
Paying members :15 companies
Supporting members: 10 companies



Panel Level Fan Out Consortium

Consortium
on Low Cost Panel Level Fan-out Technology Development

- 25 International Companies joined the Consortium
- Target single die fan-out (one layer RDL) development & demonstration (Phase 1)
- Establish design, simulation, process capability and panel level fan-out supply chain build up
- Complete single die fan-out lesson learnt and preliminary process & reliability qualification
- Drive low cost solutions & commercialization
- Establish panel level fan-out technology Industry chain embryonic in China

Die First Process

Die First Process

Lamination

Die Attach

Panel Molding

2nd Bonding

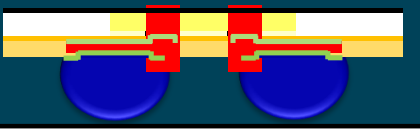
RDL

UBM

Ball Drop

Testing

Package structure



Package size: 8.9 x 7.7 mm
RDL: 1 layer
RDL Line/Space: 20/20μm
Ball Pad Size: 250 μm
Ball Pad PI Open: 230 μm

Die sizes: 5.24 x 4.835mm
Die pad pitch: 96 μm
Die thickness: 200 μm
Die Pad PIO: 65x65 μm
Die Pad Qty.: 207

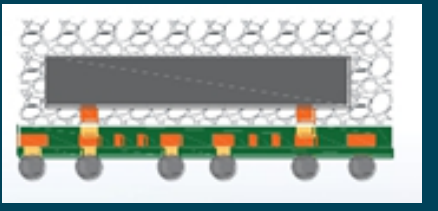
Key Benefits

- Have advantage of easier process
- Thinner than flip chip package (no substrate)
- Support increased I/O density
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance
- Fine line & space
- Panel level molding process
- Establishing panel level fan out industrial base

Die Last Process

- Die Last Process
- Substrate Pattern
- Substrate Surface Finishing
- Temporary Bonding
- Flip Chip
- Panel Molding
- Singulation
- Ball Drop
- Testing

Package structure



Package size: 8 x 8 mm
Package ball Qty : 185
Substrate Line: 1 layer
Line/Space: 30/30um

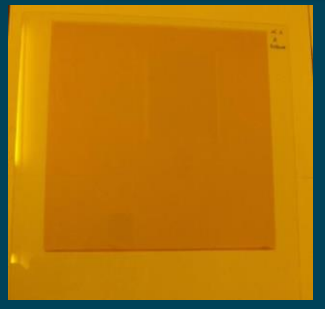
Die sizes: 6 x 6 mm
Die pad pitch: 200 µm
Die Thickness: 150 µm
Cu pillar height : 70um
Copper pillar Qty.: 203

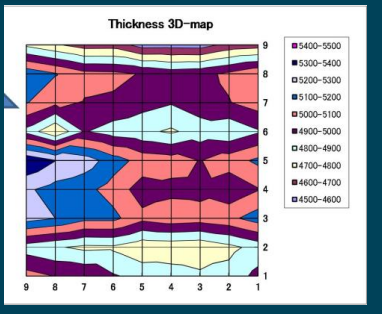
Key Benefits

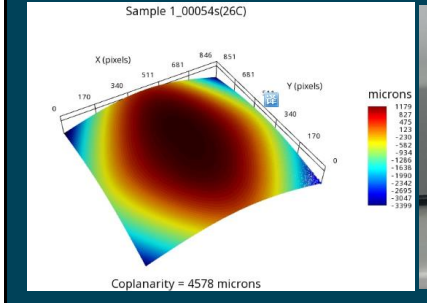
- Utilizes a Low Cost FC Coreless Substrate
- Panel processing (low cost)
- No FO Wafer Fab Investment needed, can use existing Flip Chip Packaging manufacturing lines
- Fan-Out Packages with low thickness
- Design based on flip chip die
- Test as module as usual
- Establishing panel level fan out industrial base

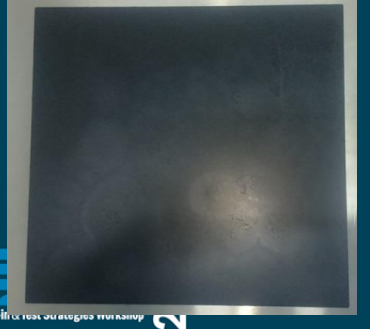
Major Results Sharing

Die First Process

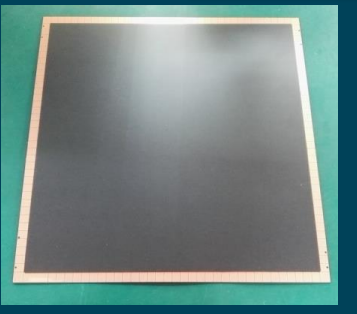


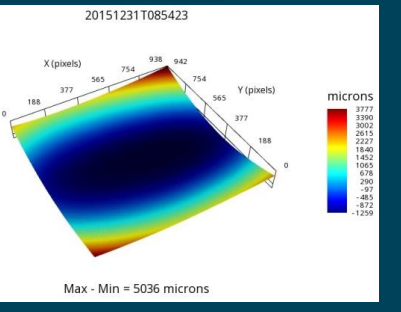


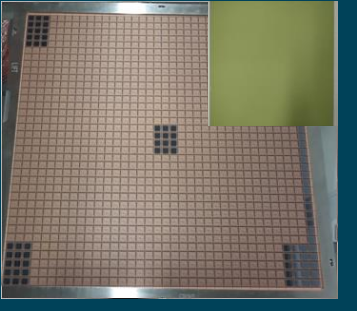


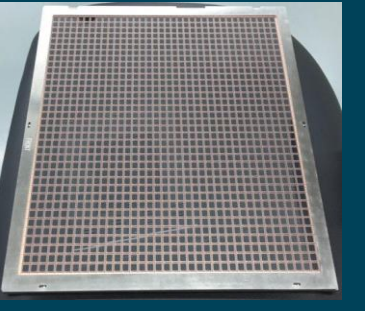


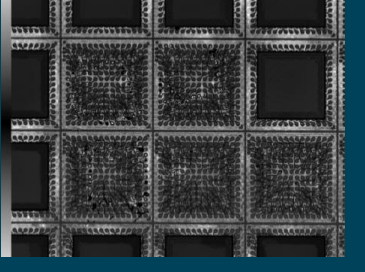
Die Last Process

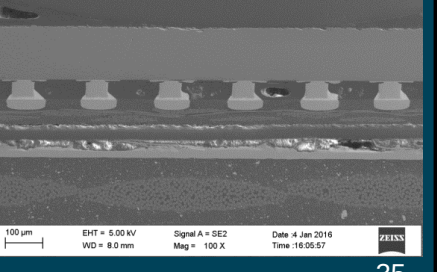












BiTS China 2017 - Fan Out Technology Overview

35

Conclusions

1. Fan out technologies are commercialized in the major forms of eWLB, RCP, InFO, and other mixed technologies.
2. The market will be booming for fan out especially after Apple iPhone 7 was using InFO technologies. LPFO will be commercialized soon.
3. The material and equipment suppliers are facing challenge of supplying qualified solutions with time frame and low cost.
4. China will be the hot place to execute fan out manufacturing and products in next 5 years.

Thank You !


华进半导体封装先导技术研发中心有限公司
NCAP CHINA
Vision
World Class R&D and Commercialization Center
for Adcanced Packaging & System Integration
Mission
Innovate Incubate Influence Impact
Value
Collaboration Innovation Perseverance Excellence
National Center for Advanced Packaging
www.ncap-cn.com