BiTS 2017

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

www.bitsworkshop.org

March 5-8, 2017

Copyright Notice

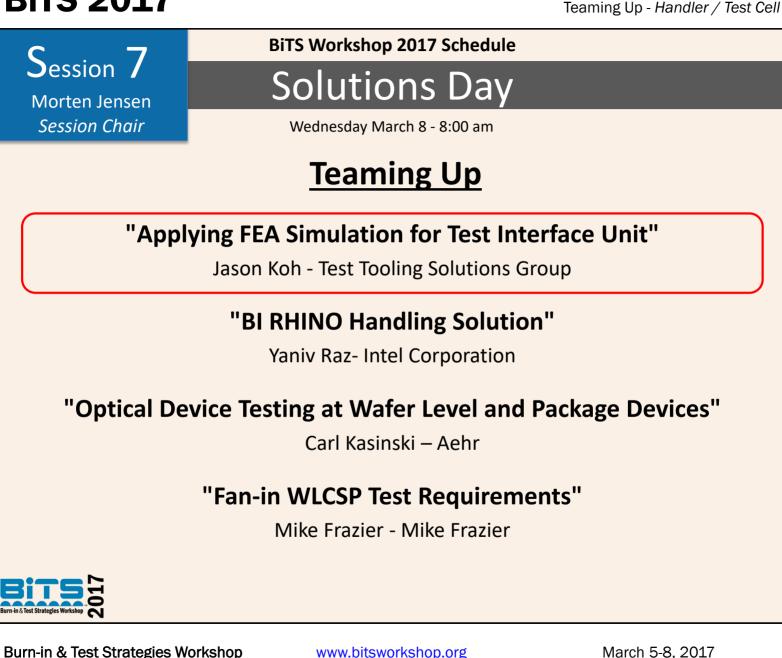
The presentation(s)/poster(s) in this publication comprise the Proceedings of the 2017 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2017 BiTS Workshop. This version of the presentation or poster may differ from the version that was distributed in hardcopy & softcopy form at the 2017 BiTS Workshop. The inclusion of the presentations/posters in this publication does not constitute an endorsement by BiTS Workshop or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by BiTS Workshop. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop. All rights reserved.



BiTS 2017



Teaming Up - Handler / Test Cell

BiTS 2017

Applying FEA Simulation for Test Interface Unit

Jason Koh Shiann Chern Test Tooling Solutions Group



BiTS Workshop March 5 - 8, 2017



Burn-in & Test Strategies Workshop

www.bitsworkshop.org

March 5-8, 2017

Teaming Up - Handler / Test Cell

Contents

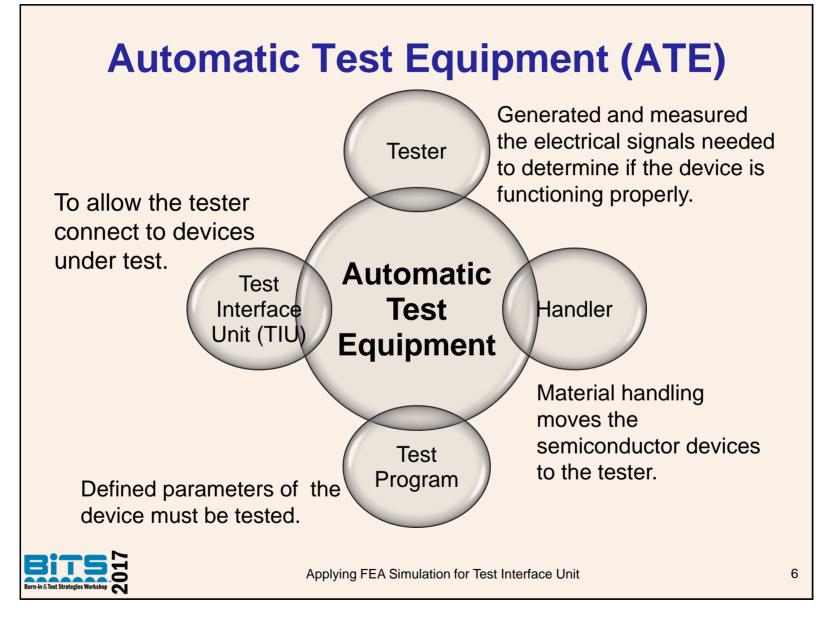
- 1. ATE & Test Interface Unit (TIU) Stack Up
- 2. TIU Challenges
- 3. TIU products that involved for FEA Simulation
- 4. Benefits and Challenges in FEA Simulation
- **5. FEA Simulation Process Flow**
- 6. Test Socket Analysis & Example
- 7. Conclusions



Applying FEA Simulation for Test Interface Unit

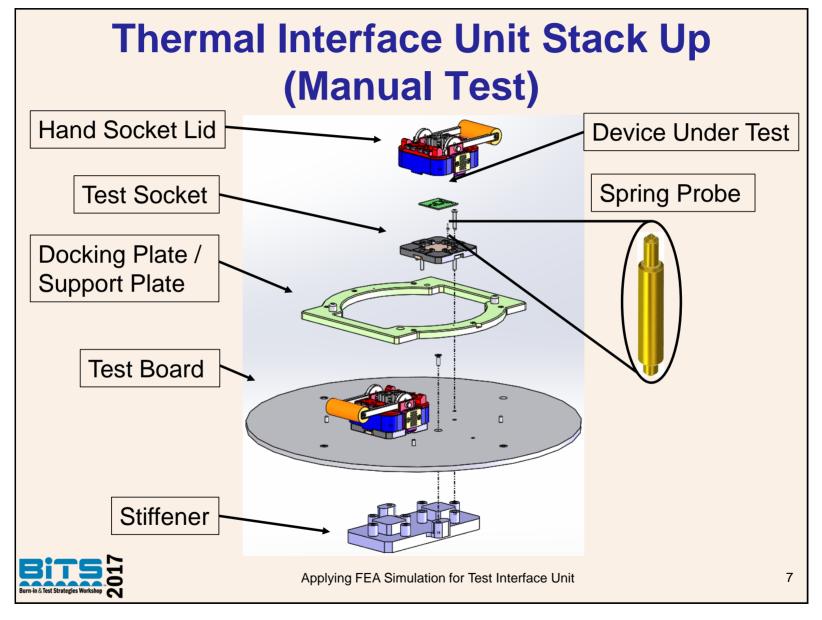
5

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

Thermal Interface Unit Challenges

Challenges

- Narrow Pitch (<0.20mm)
- High pin count (4000++)
- High bandwidth, short pin requirement (Pin test height <2.0mm and below)
- High insertion force (TIU need to overcome100kgf)
- Time to market, Reliability and Cost

Impacts

- Spring probe diameter become more challenging.
- High warpage and high stress concentration on test socket.
- Thinner socket design potential to cause high deformation on socket body during preload stage.
- Hand socket lid, package, test socket, PCB and stiffener have structure stiffness concern.
- Product development cycle, factor of safety, material selection



Applying FEA Simulation for Test Interface Unit

Teaming Up - Handler / Test Cell

How to Approach New Challenges?

- Design something that worked in the past and made it bigger/smaller.
- Use spreadsheets or hand calculations
- Build and test prototypes
- Trial and error method

Or

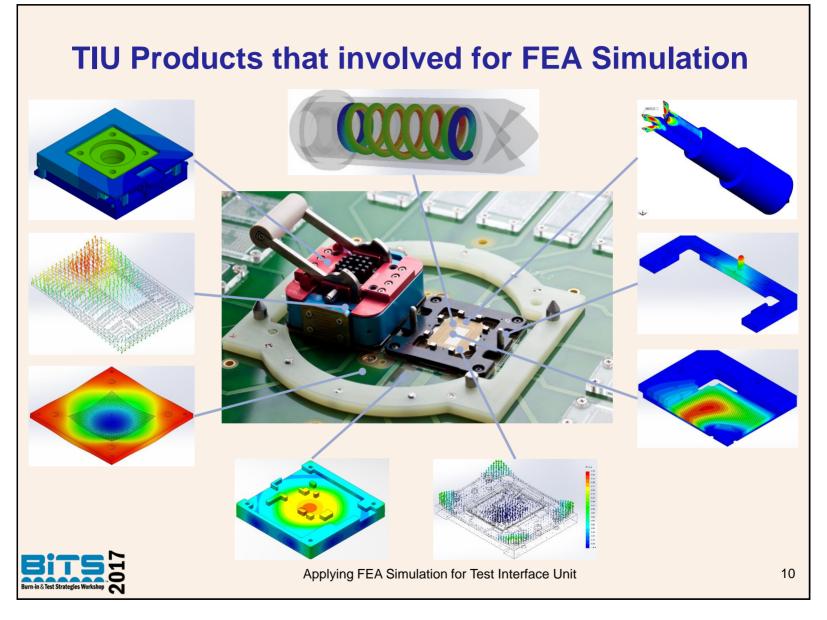
Utilize Finite Element Analysis method to solve your engineering problems



Applying FEA Simulation for Test Interface Unit

BiTS 2017

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

www.bitsworkshop.org

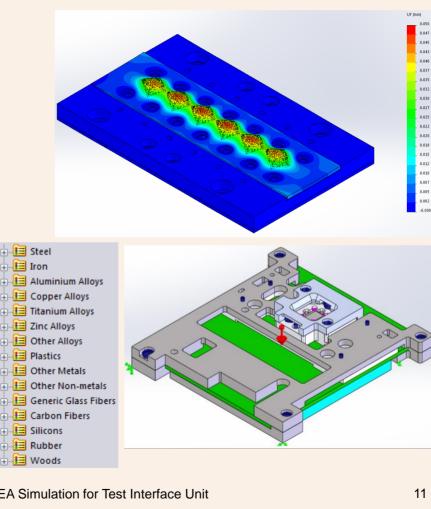
March 5-8, 2017

Teaming Up - Handler / Test Cell

BiTS 2017

Benefits of FEA Simulation

- Solve a wide variety of engineering problems
- Can handle very complex geometry
- Useful for problem with complicated restrains and loading
- Analyze the impact of different material properties





Applying FEA Simulation for Test Interface Unit

Burn-in & Test Strategies Workshop

BiTS 2017

Challenge in FEA Simulation

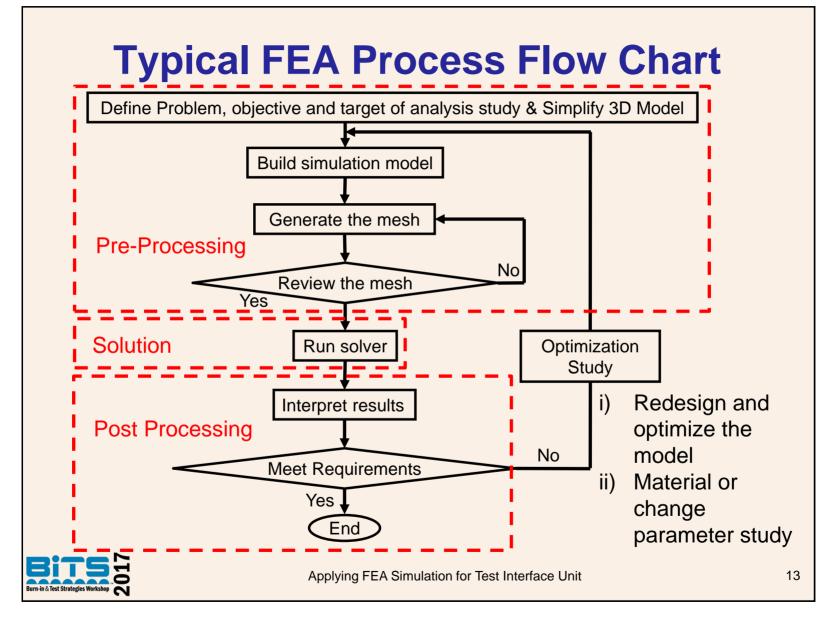
- Simulation building requires experience and judgment in order to construct a good finite element model
- Simulation results may be difficult to interpret
- The simulation results provide "approximate" solutions
- The simulation has "inherent" errors
- Mistakes by users can be fatal

User error 🛛 🕅					
8	This error can be caused by the user doing something stupid. Please replace user!				
[Ignore OK Sorry!				



Applying FEA Simulation for Test Interface Unit

Teaming Up - Handler / Test Cell



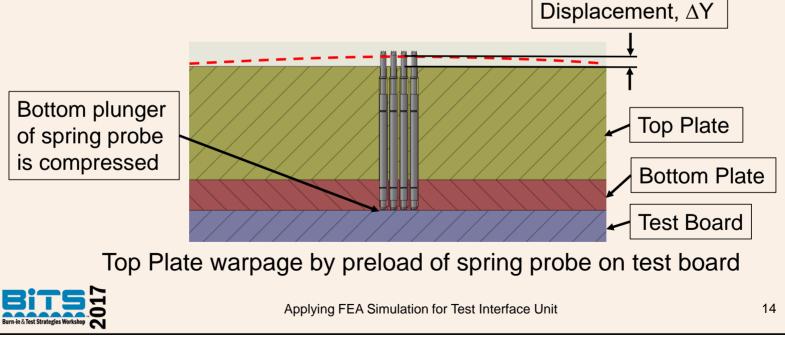
Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell

Example Test Socket Warpage

Problem Statement:

- i) Pin counts increase, stress and displacement on the test socket stiffness becomes a major concern.
- ii) Stable electrical performance of spring probe, bottom plunger of spring probe is always compressed when test socket is mounted on test board.



BiTS 2017

Teaming Up - Handler / Test Cell

Inputs for Analysis

<u>Target</u>

- i) Less than 0.15mm for Top Plate coplanarity
- ii) Material stress for factor of safety (FOS) at least or more than 2.0

<u>Input</u>

- i) 3piece design, consist of Guide Plate (GP), Top Plate (TP) and Bottom Plate (BP)
- ii) Spring Probe Preload 13gf
- iii) Total 4352 pins counts
- iv) Total preload acting on TP = 4352 * 0.013 kgf = 56.576kgf

Type of Analysis

Linear Static FEA



Applying FEA Simulation for Test Interface Unit

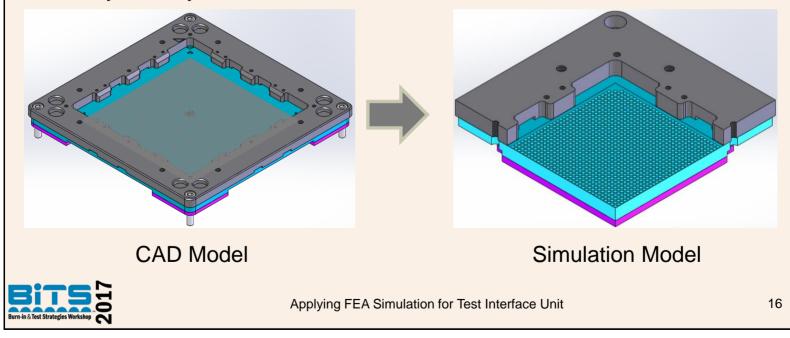
15

Teaming Up - Handler / Test Cell

CAD Modelling for FEA

Guideline for 3D CAD Simplification

- i) Remove outside corner chamfer and fillet.
- ii) Remove small holes, slot and step cut outside the load path.
- iii) Remove decorative and indication features
- iv) Use of quarter of CAD model, if load and support are symmetry.



Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell

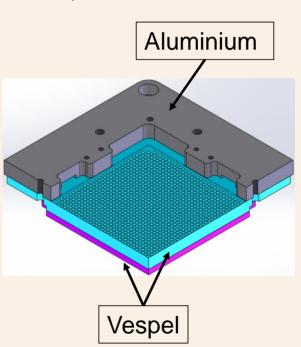
Build Simulation Model

i) Assign Materials

Linear static FEA material property required are,

- Elastic Modulus, (E)
- Poisson's Ratio, (v)
- Shear Modulus, (G)
 G = E / (2(1+v))
- Yield Strength (or Ultimate Strength)

Material		Elasric Modulus GPa	Poisson's Ratio	Yield Strength MPa	
GP	Aluminium	72.0	0.33	505	
TP & BP	Vespel	4.0	0.41	155	





Applying FEA Simulation for Test Interface Unit

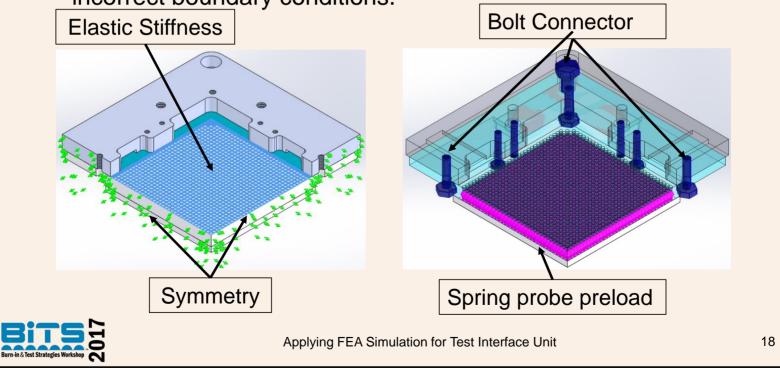
Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell

Build Simulation Model

ii) Apply Boundary Conditions & Loads

- The choices of boundary conditions & external loadings have a direct impact on the overall accuracy of the model.
- Over-constrained model will cause stiff model due to apply incorrect boundary conditions.



Teaming Up - Handler / Test Cell

Build Finite Element Mesh

Generate & Review the Mesh Modelling

- Accuracy of the solution is primarily dependent on the quality of the mesh.
- Check the mesh quality (Aspect Ratio, Distortion Element)
- Apply mesh control on critical area

	Study name	F (-Default-)	T		
	Mesh type	Solid Mesh			
	Mesher Used	Curvature based mesh			
	Jacobian points	4 points			
	Mesh Control	Defined			
	Max Element Size	2.8 mm			
	Min Element Size	0.56 mm			
	Mesh quality	High			
	Total nodes	1158482			
	Total elements	698528			
1	Maximum Aspect Ratio	9.7947			
i.	Percentage of elements with Aspect Ratio < 3	92	li –		
I.	Percentage of elements with Aspect Ratio > 10	0	1		
	% of distorted elements (Jacobian)	0			
	Remesh failed parts with incompatible mesh	011			
	Time to complete mesh(hh:mm:ss)	00:01:24			
	Computer name	TTDMSIMULATION			
			-	Mesh View	
Burn-in	Applying FEA Simulation for Test Interface Unit				

BiTS 2017

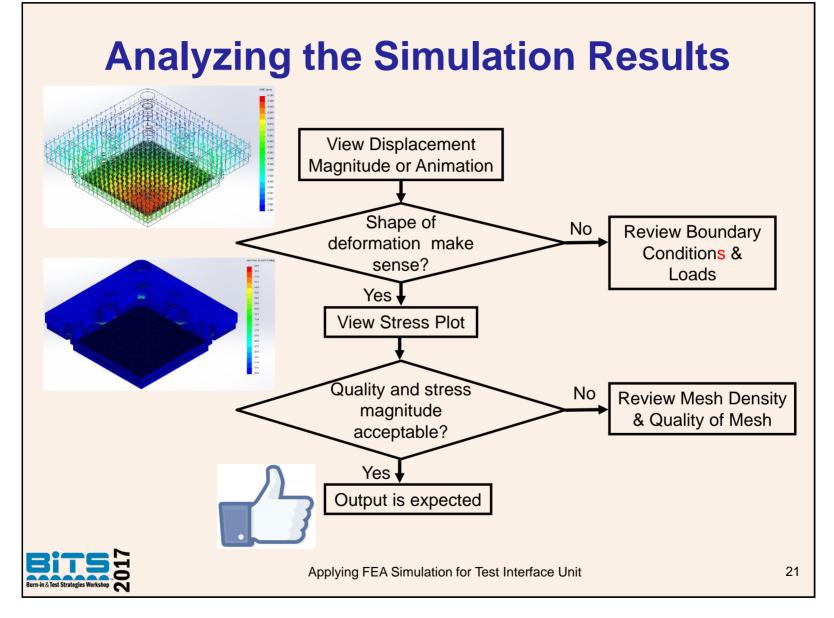
Teaming Up - Handler / Test Cell

	FEA Solver <u>Run Solver</u> Factors when choose the proper solver				
		Direct Sparse	Iterative		
	DOF over 1,000k		\bigcirc		
	Multiple Cores, More RAM, More Disk Space	\odot			
	Single parts or less assembly parts		\bigcirc		
	Assembly with lots of contact set	\odot			
	Analysis with No Penetration contacts	\odot			
	Mixed-mesh models	\odot			
	Models of parts with widely different material properties	\bigcirc			
Burn-in&1	Applying FEA Simulation for Test Interface Unit				

Burn-in & Test Strategies Workshop

Session 7 Presentation 1

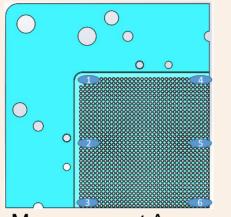
Teaming Up - Handler / Test Cell

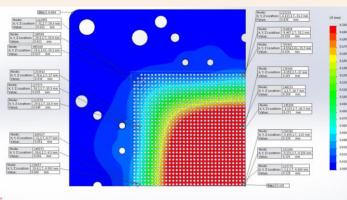


Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell

Physical & Virtual Correlation





Measurement Area

Probe Point from Simulation

	Measured	FEA Results	FEA vs Measured
Area	Y-Displacement	Y-Displacement	∆ Percentage, %
1	0.024	0.022	5.6
2	0.042	0.040	4.0
3	0.059	0.058	2.3
6	0.040	0.038	5.8
7	0.248	0.269	8.5
8	0.312	0.328	5.1

A good correlation between simulation and measured deformed of test socket.

Applying FEA Simulation for Test Interface Unit

in & Test Strategies

Teaming Up - Handler / Test Cell

Meet Requirement?

4352L-BGA	DOE1		
Pin Length, mm	3.00		
Total Pin Preload (kgf)	56.576		
Material (GP)	Aluminium		
Material (TP & BP)	Vespel		
Max Y-Displacement (TP) (mm)	0.328		
Max Von Mises Stress (TP) (MPa)	67.0		
Factor of Safety (TP)	2.31		

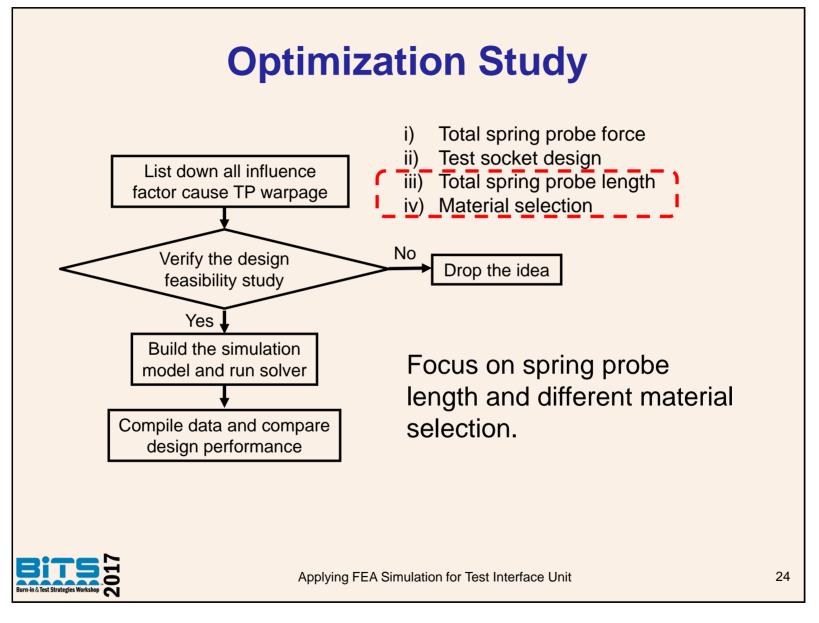
- Target 0.150mm for TP coplanarity
- Maximum displacement from simulation 0.328mm
- Unstable electrical spring probe performance cause by high warpage
- TP material stiffness is not enough
- Thin TP thickness cannot withstand high pin force
- Improvement study is required



Applying FEA Simulation for Test Interface Unit

BiTS 2017

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

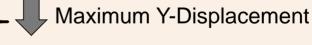
Teaming Up - Handler / Test Cell

Optimization Study

4352L-BGA	DOE1	DOE2	DOE3	DOE4	DOE5
Pin Length, mm	3.00	4.70	5.70	5.70	5.70
Total Pin Preload (kgf)	56.576	56.576	56.576	56.576	56.576
Material (GP) & Elastic Modulus	Aluminium, 72 GPa	Aluminium, 72 GPa	Aluminium, 72 GPa	Aluminium, <u>72</u> GPa	Stainless Steel, 190 GPa
Material (TP & BP) & Elastic Modulus	Vespel, 4 GPa	Vespel, 4 GPa	Vespel, 4 GPa	Torlon, 14.6 GPa	Torlon, 14.6 GPa
Max Y-Displacement (TP) (mm)	0.328	0.250	0.189	0.107	0,093
Max Von Mises Stress (TP) (MPa)	67.0	64.5	64.4	65.1	63.5
Factor of Safety (TP)	2.31	2.40	2.41	2.64	2.71

Pin length (DOE1 -> DOE 2 -> DOE3)

- High stiffness material applied on
- socket body (DOE 3 -> DOE4-> DOE5)



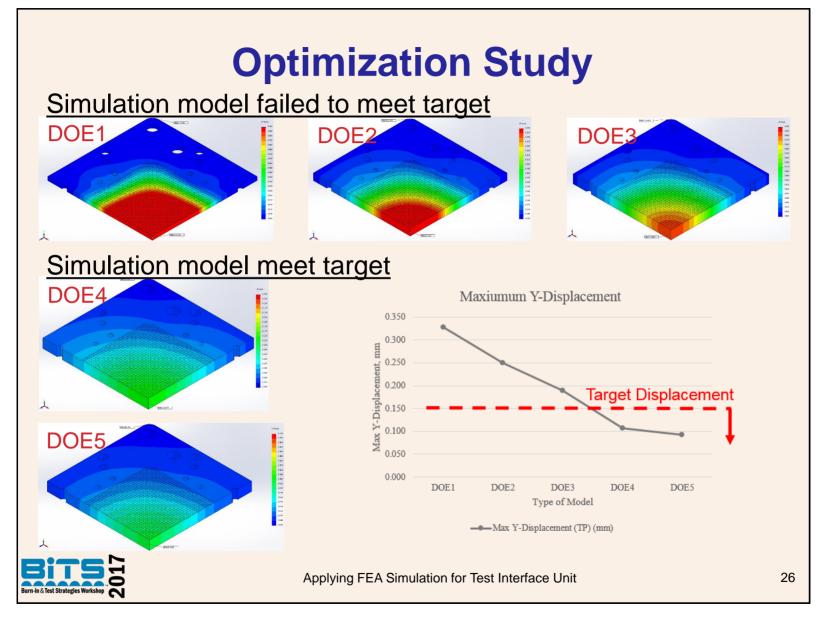


Applying FEA Simulation for Test Interface Unit

Burn-in & Test Strategies Workshop

BiTS 2017

Teaming Up - Handler / Test Cell



Burn-in & Test Strategies Workshop

Teaming Up - Handler / Test Cell

Conclusions

- FEA simulation help engineers filter out potential risk and gain a much broader picture for better decisions making.
- Training is required and the opportunity to practice extensively.
- Comparing simulation results with physical data if possible.
- Finite Element Analysis make a good engineer great, and make a bad engineer dangerous.
- "Garbage in = Garbage Out" magic box dilemma



Applying FEA Simulation for Test Interface Unit

Burn-in & Test Strategies Workshop