EIGHTEENTH ANNUAL
BiTS
TM
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 6
© 2017 BiTS Workshop – Image: tonda / iStock

Copyright Notice

Session 6
Jason Mroczkowski
Session Chair

BiTS Workshop 2017 Schedule

Frontier Day

Tuesday March 7 - 1:30 pm

Making Contact

"High Current Final Test Contactor Development"

Thiha Shwe, Hisashi Ata – Texas Instruments

Kenichi Sato – Yokowo

"Customers Are the New Team Member for Board to Board Connectors"

Derek Biggs – Plastronics

"WLCSP Contacting Technologies for 0.2 mm Pitch and Below"

Valts Treibergs - Xcerra Corporation

"Coming to terms with Burn-In sockets"

James Tong - Texas Instruments

Coming to Terms with Burn-In Sockets

James Tong
Texas Instruments

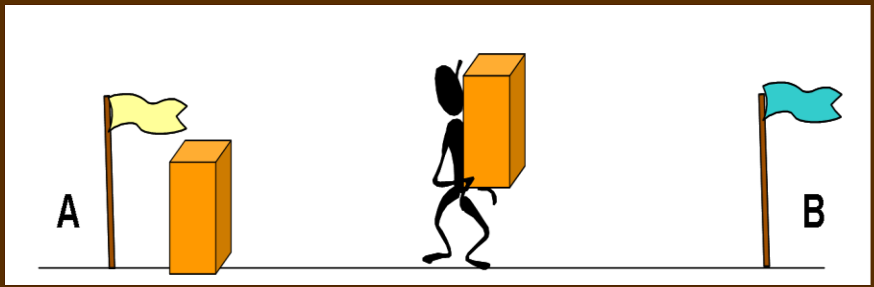
BiTS Workshop
March 5 - 8, 2017

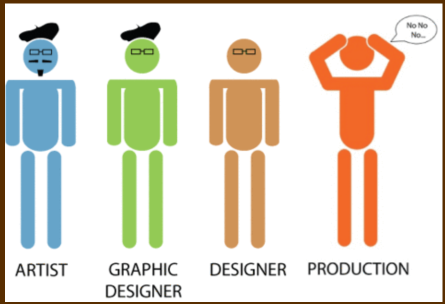
Contents

- Background
- Root cause review
- Solution selection
- Qualification process
- Result and data review
- Lesson learned
- Standardization
- Future plan

Background

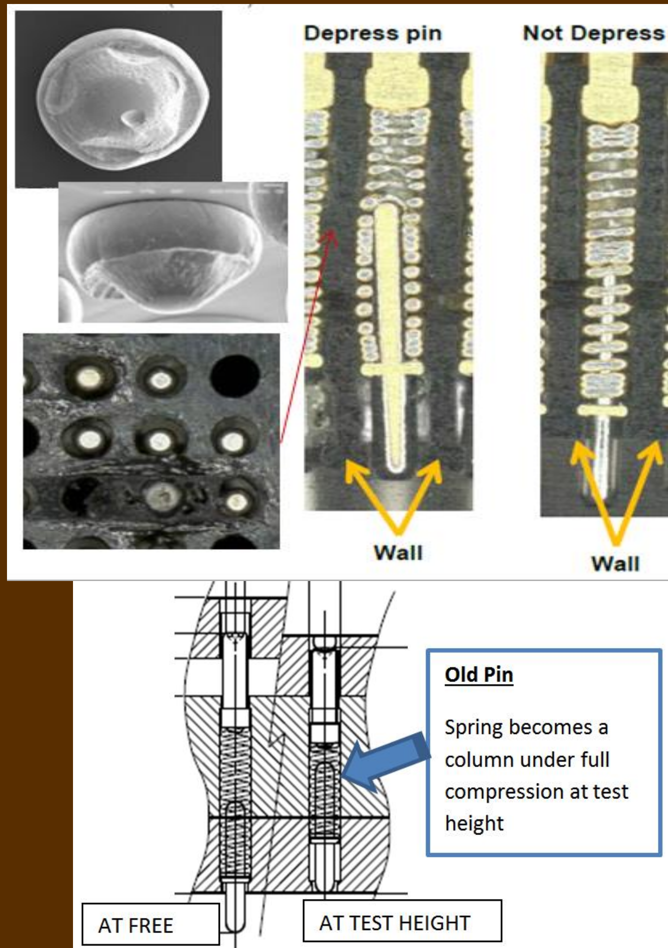
- Custom solution per device per supplier
- Solution selected base on
  - good faith and experience from last project
  - pricing is the main driver
- Engineering hardware for device checkout/qualification gets propagated to production burn in



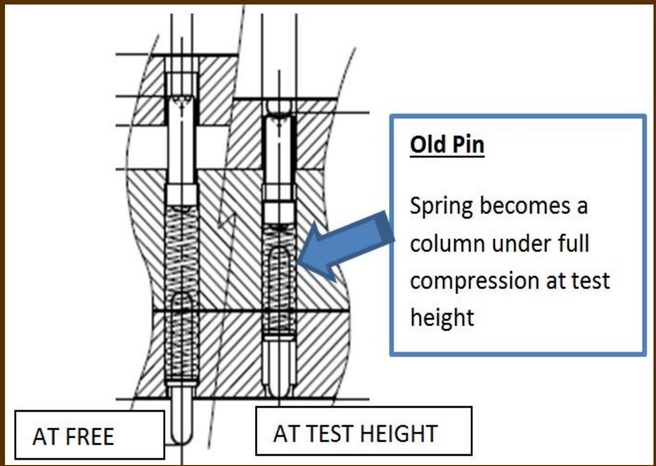


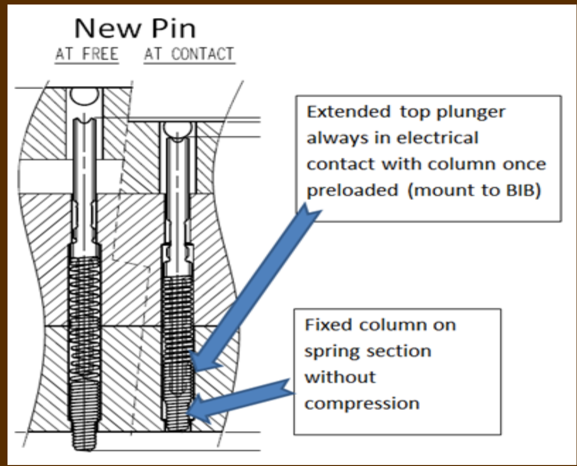
Root cause review

- Historically used solution was inferred to be the best solution
- Ball damaged due to stuck pin
- Plastic socket housing around the pin melted with Tj >200°C
  - High current
  - Contact resistance failure
  - Housing material
  - Defective device
- 5Ws => Ball deformation → stuck pin → melted housing → heated spring → current flows thru the spring



Solution selection – pick the right pin structure





- Considering the possible root causes of failure
- Plan checkout DOEs

Solution selection – decision matrix

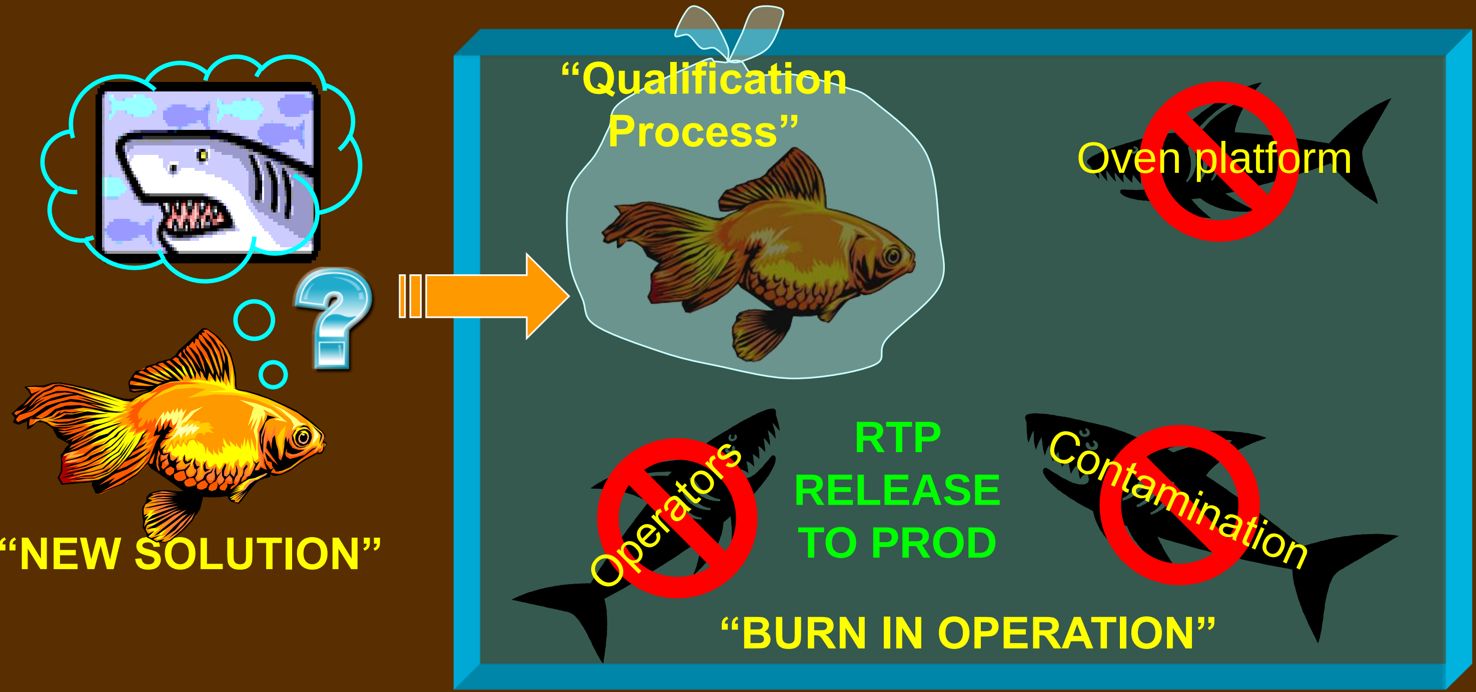
Selection Matrix					
Supplier	**Weightage**	**Vendor A**	**Vendor B**	**Vendor C**	**Vendor D**
Cost	3	4	5	3	4
Design Robustness	5	4	2	3	4
Responsiveness	3	2	4	3	4
A/T site Support	3	3	2	4	4
Dallas Dev. Support	3	4	3	4	4
Pin Design	5	3	4	3	4
Engineeering Support	4	4	3	3	4
Quality	3	2	3	3	4
Delivery	4	3	4	2	4
Unweigthed Average		3.22	3.33	3.11	4.00
Total		**102**	100	92	**120**

#		Parameter	Units
1	Class	Manufacture	
2	Class	Pin Model #	
3	Class	Package	
4	Class	Pin Use	
5	Class	Status	
6	Cost	Price/pin	US$
7	Mechanical	Pin Drawing#	
8	Mechanical	Working CPH	mm
9	Mechanical	Force @ cph	grams
10	Mechanical	Min Pitch	mm
11	Mechanical	PCB Pre-Load	mm
12	Mechanical	DUT Compression	mm
13	Mechanical	Tip Shape	(PCB Side)
14	Mechanical	Tip Shape	(Dut Side)
15	Mechanical	Temp	Deg C
16	Mechanical	Kelvin F/S Pin Gap	mm
17	Electrical	Cres	mOhm
18	Electrical	CCC	Amps
19	Electrical	Induct. - Self	nH
20	Electrical	Induct. - Mutual	nH
21	Electrical	Cap. - Gnd	pF
22	Electrical	Cap. - Mutual	pF
23	Electrical	Insertion Loss (S21)	GHz @ -1dB
24	Electrical	Return Loss (S11)	GHz @ -20dB
25	Chemical	DUT Tip Plating Material	
26	Chemical	DUT Tip Base Material	
27	Chemical	PCB Tip Plating Material	
28	Chemical	PCB Tip Base Material	
29	Chemical	Spring Matl	
30	Chemical	Housing Matl	
31	Prod	Life	Insertions
32	Prod	Cleaning Interval	Insertions
33		Comment	

- Pick supplier → matrix
- Specify pin → worst case test requirement
- Qualify selected solution → qualification plan to define roadmap solutions

Qualification process

- 3 steps process
- Best of the Cheapest vs. Cheapest of the Best



Qualification process – Step1

Step 1: Vendor Self Qual and to submit report	
1	Pin Spec on Force, Cres, Lifetime (>5k)
2	Reliability test report up to 1000hr for Cres, Package sticking, Contact Mark and contamination check
3	Pin drawing
4	Socket design showing Z-stack up at test
4a	Details on Z-stack up at test
4b	Light colored or white base (good contrast to DUT for easy manual loading)
5	Pin to ball alignment validation (Positional analysis using RSS value or cross sectioning method)
6	Package wrapage simulation and other potential concern
7	Ra spec and report on nickle plated mirror finish Boss sample
8	Footprint compatability to TI std
9	Cabless connection for heater/thermistor if Dynamic temperatue control is applicable
10	CMT open top socket

- Max 2 pins designs to support all pitch in package family (BGA, QFN, QFP)
- CCC of 2 A or greater, Pin force of 15g/pin or less
- Vendor factory data on proposed pin solution
- Engineering data to support design robustness

Qualification process – Step2

Step 2: FAI checkout	
1	1 to 3 BIBs FAI checkout with BU
2	Full functionality
3	Die and package crack eval as needed
4	Run 5 to 10 consecutive insertions using production test program (100% electrical yield) and visual mechanical check on ball damage, tool marks, bottom and top side marring, substrate damage and no damage to PCB pad on BIB
5	Full BIS test in A/T site on sample units used

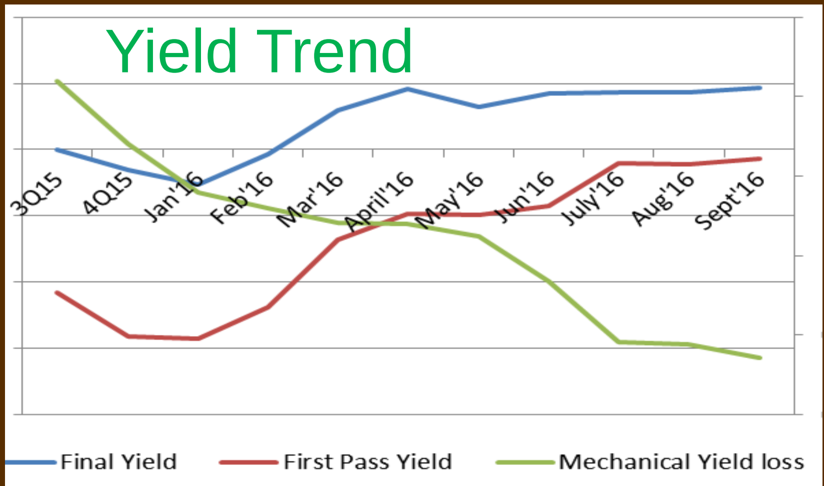
- Small sample functionality engineering checkout
  - ✓ Electrical performance
  - ✓ Mechanical performance
  - ✓ Operation friendliness

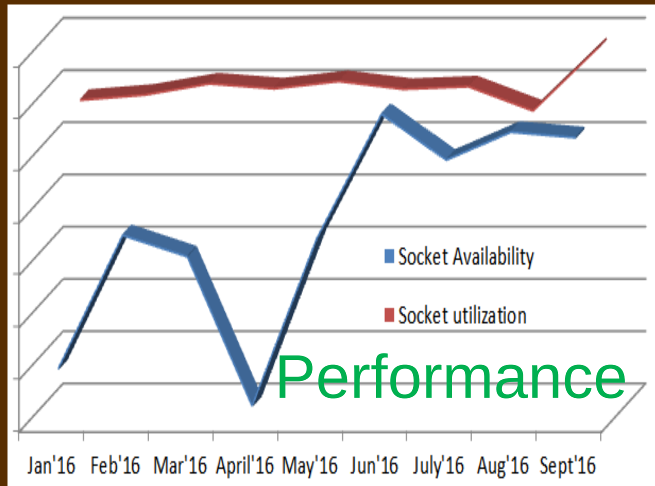
Qualification process – Step3

Step 3: Production Qualfication	
1	Repeat DOE (5 insertions) in step 2 at production site for repeatability
2	Identify lots to begin qual in production site
3	Pass ALU operation with no issue if applicable
4	Run 100 insertions under normal production conditions
4a	No or comparable production VM failure from inspections logpoints and BIS
4b	No physical damage to PCB pad on the BIB
4c	Comparable or better Frist Pass Yield
4d	Comparable or better Final Yield

- Production correlation
- High volume production qualification of solution
- Expose to typical production variables

Result and data review





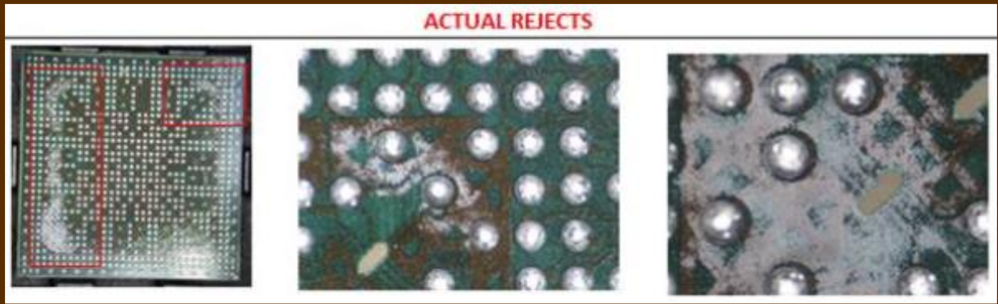
- ✓ First Pass to Final Yield Gap improved
- ✓ Final Yield improved

- ✓ Mechanical Yield loss drops (less scraps)

- ✓ More functional socket per BIB
- ✓ Better utilization / thru' put

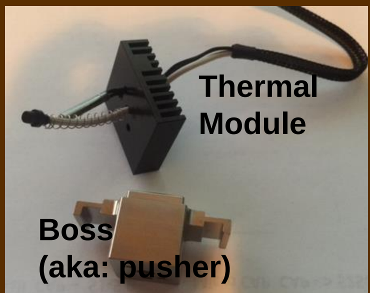
- Significant burn in test cost saving

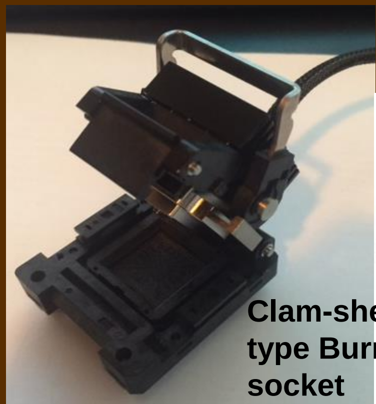
Lesson learned – Device surface marring

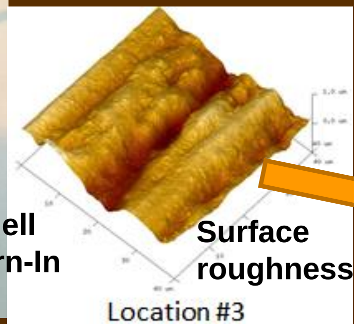


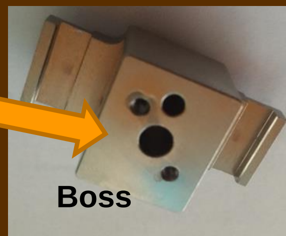
Bottom BGA substrate surface marring

Top side BGA substrate marring => illegible symbols



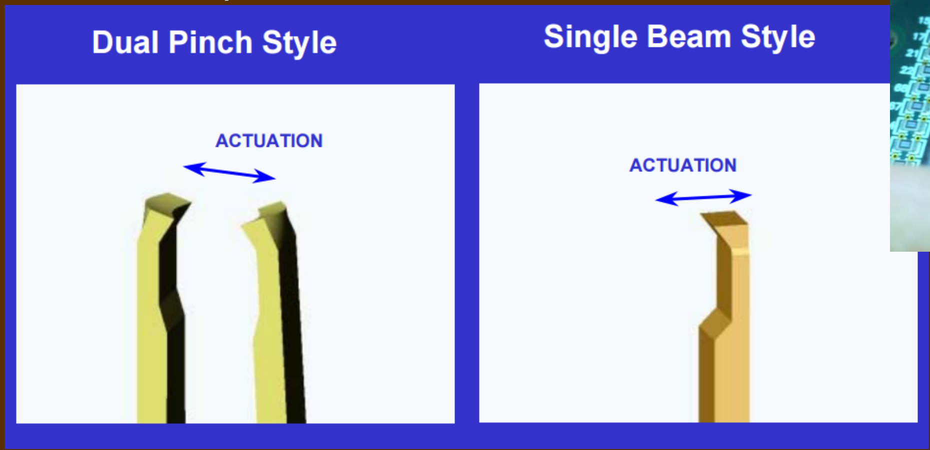


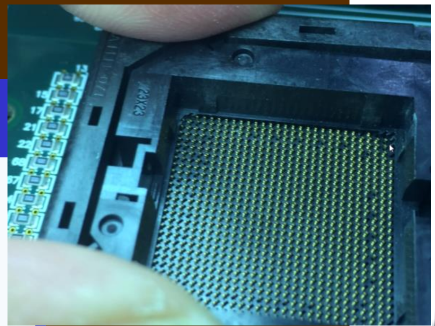




Lesson learned – Pin structure

Reproduced from BiTS workshop 2003 (Prasanth Ambady, James Forster & Jason Cullen – Texas Instruments)





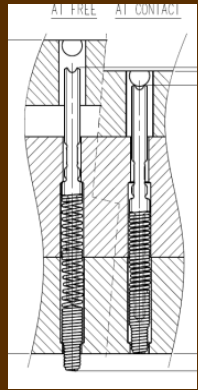
- **<u>Through hole</u>** pinch contact pin is problematic for BGA
- Impossible to replace worn off or damage socket

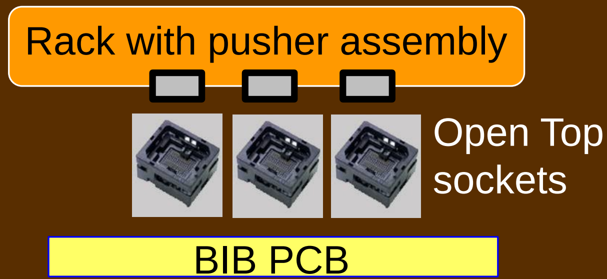
Standardization

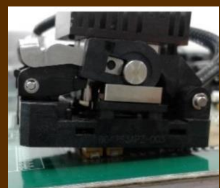
- Adopt proven qualification process
- Socket base sizes → Burn In Board (BIB) density
- Use compression mount technology (CMT) pins only
- Lock in socket mechanical design
- Minimize pin type/geometry for all device pitch
- Lower cost with best solution and volume

Future plan

- Use only roadmap CMT pin solution
- Open top sockets design
- Use rack style solution for active temperature control requirement
- Ability to use multiple socket suppliers on same device
- **Collaboration to define industry standard**







Clam-shell socket style

Acknowledgement

- TI operations team
- TI management team
- Suppliers
- BiTS2017 committee and attendees

Sensata Technologies

PLASTRONICS SOCKETS & CONNECTORS

enplas

YAMAICHI ELECTRONICS ENGINEERED TO CONNECT